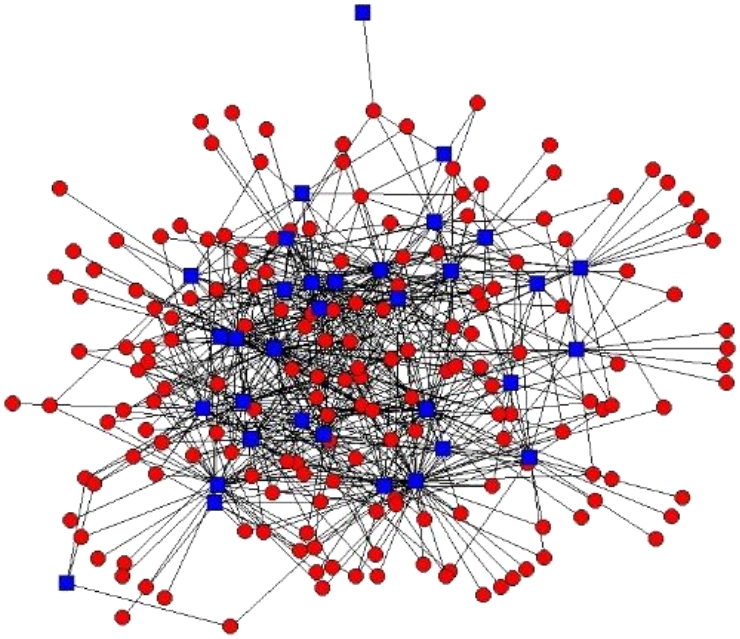
High-Performance Distributed RMA Locks

PATRICK SCHMID, MACIEJ BESTA, TORSTEN HOEFLER

Need for Efficient large-Scale Synchronization



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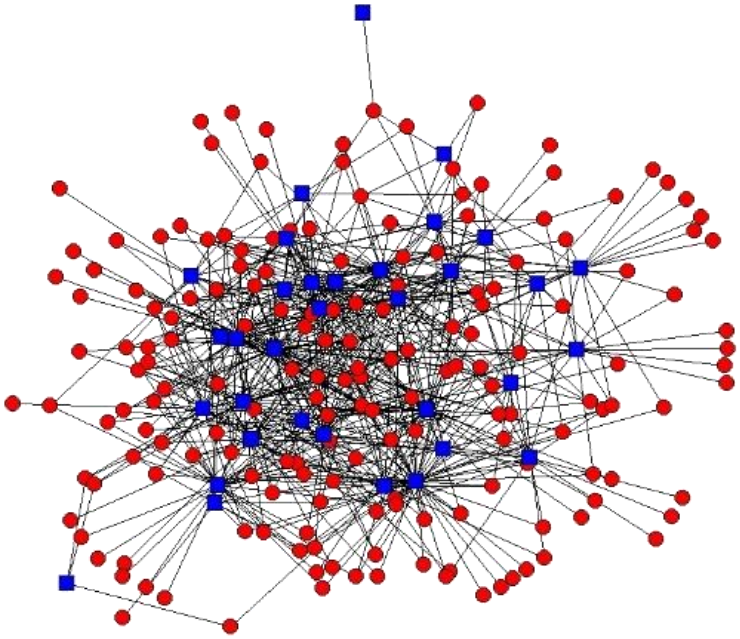

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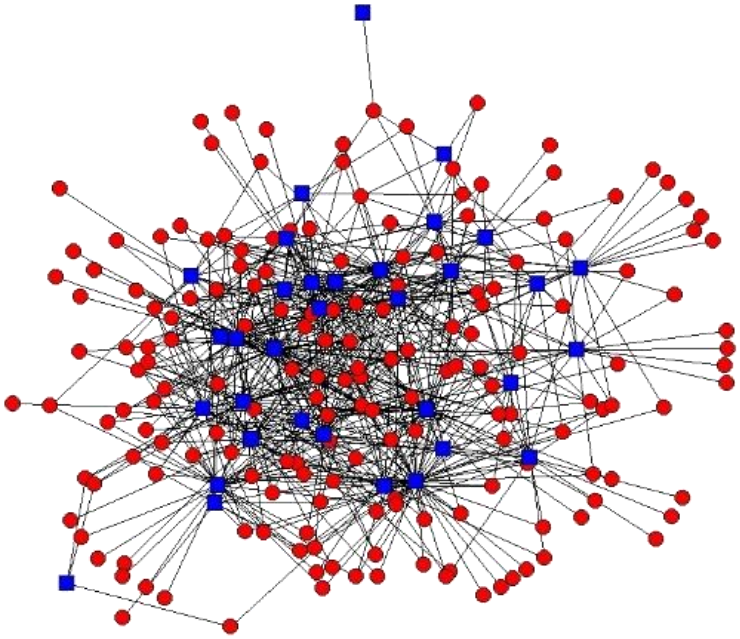

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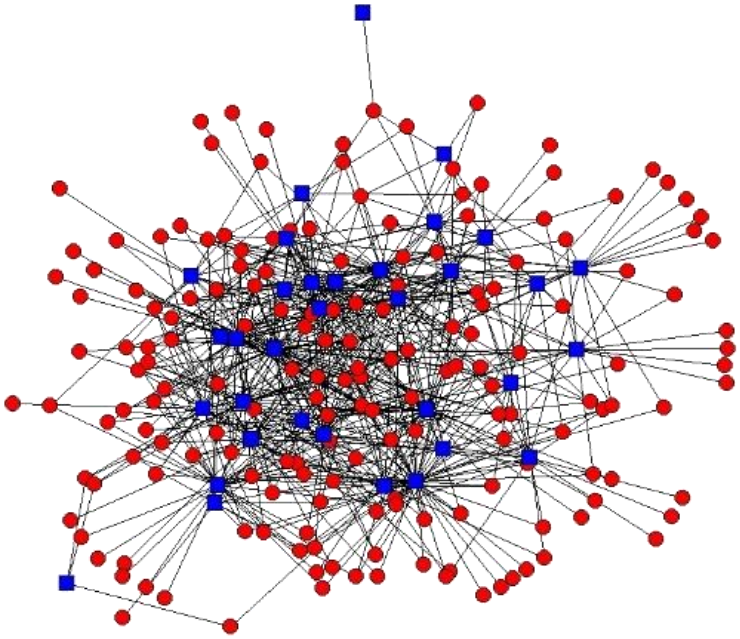
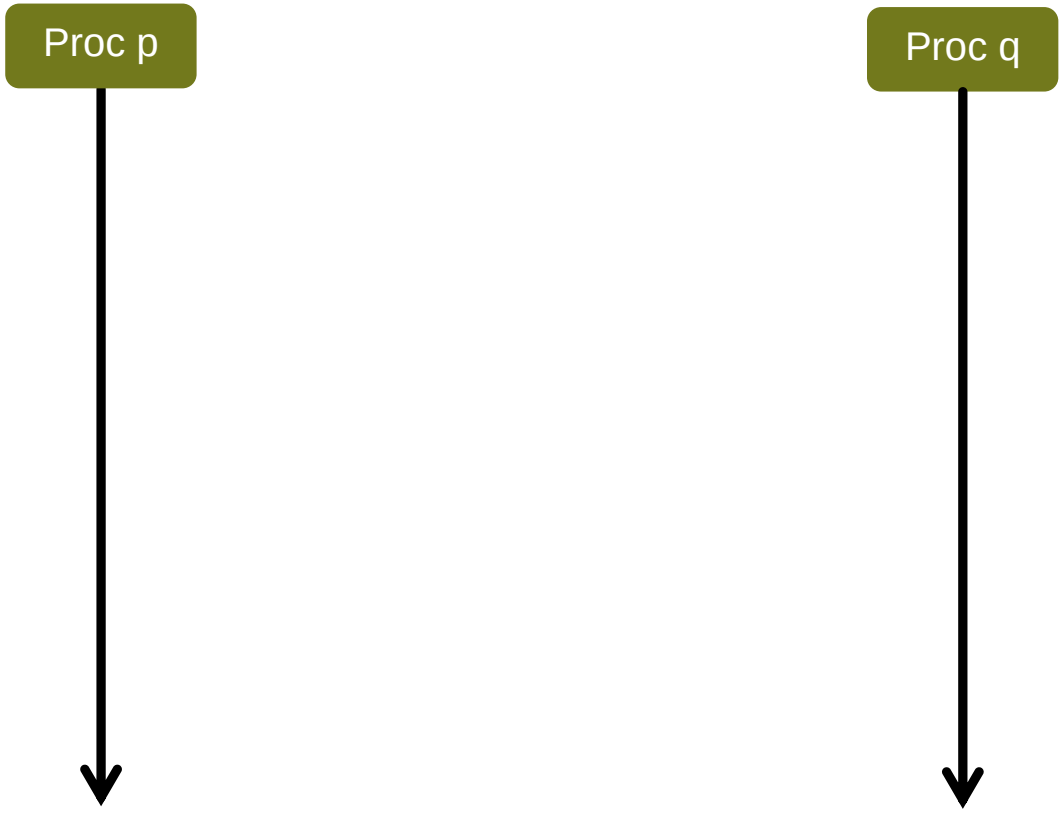


LOCKS

Locks



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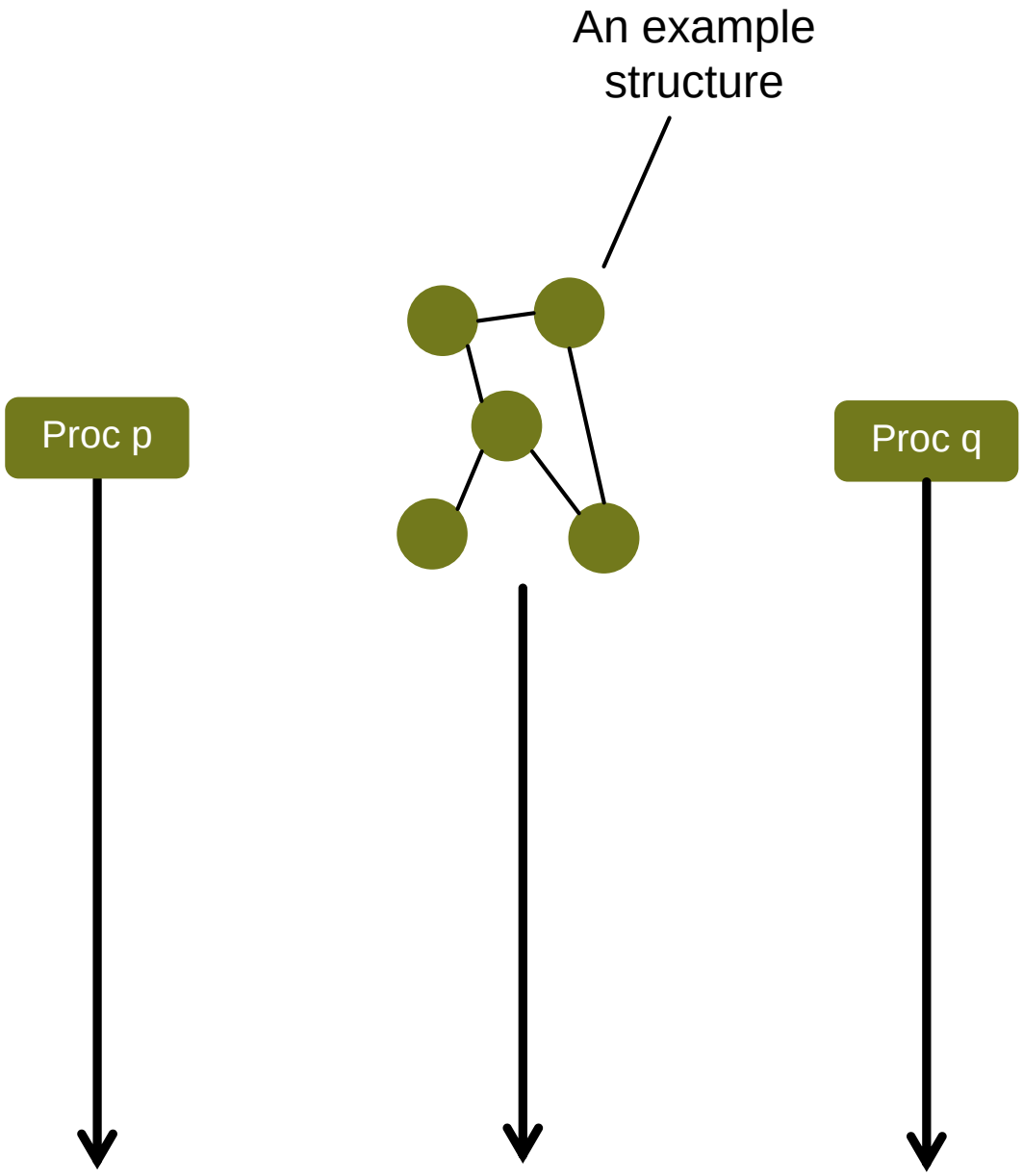

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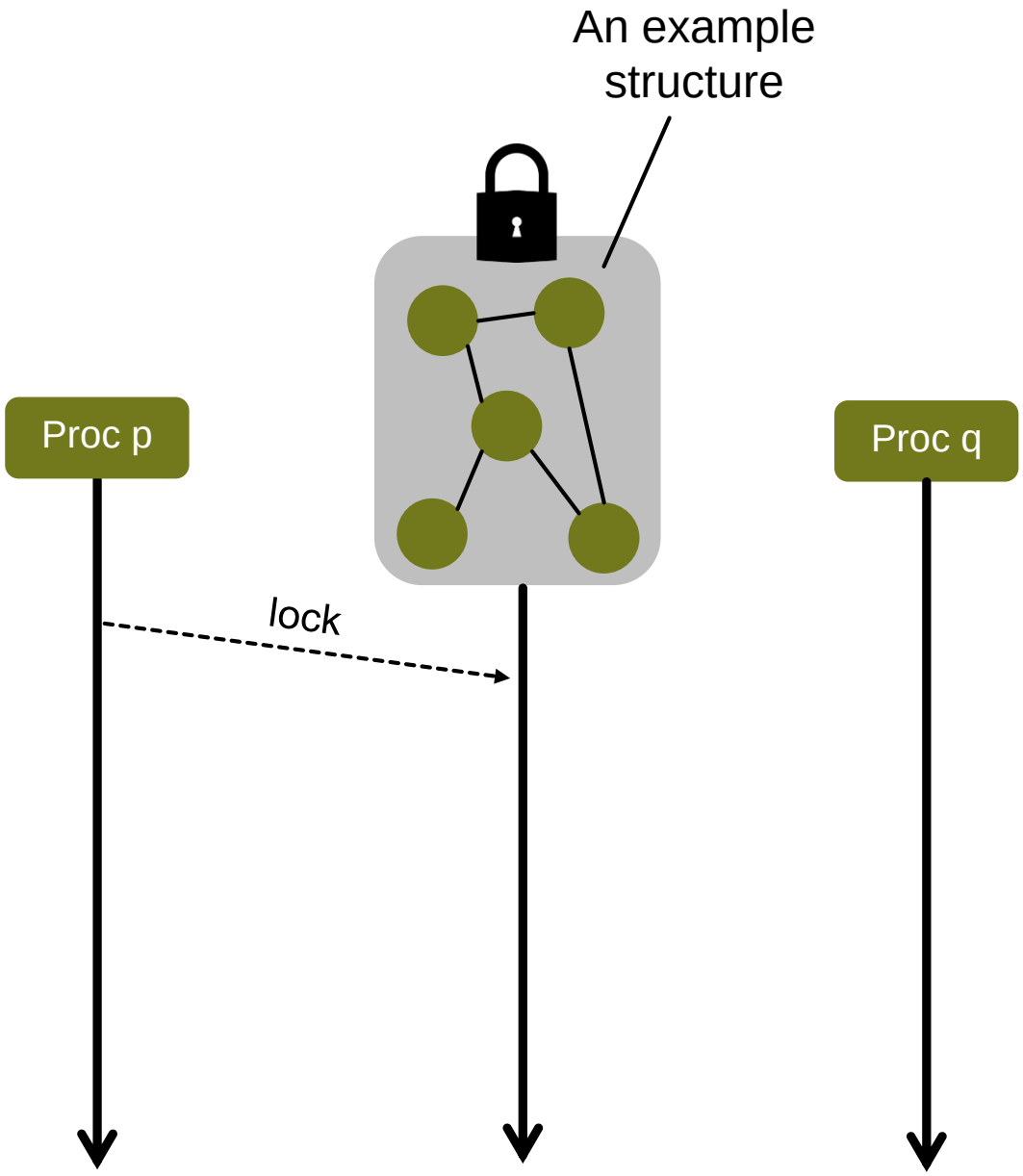

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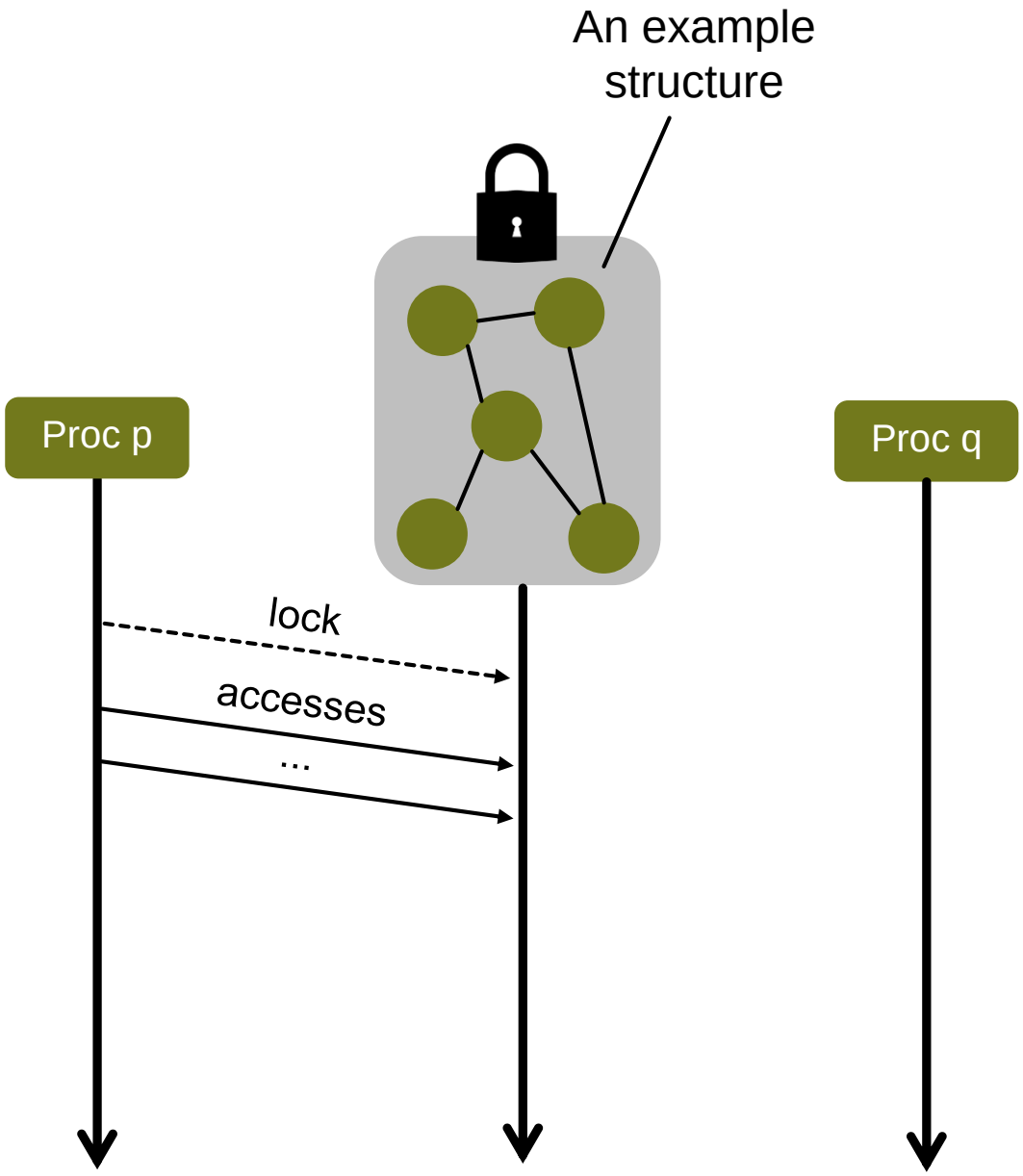

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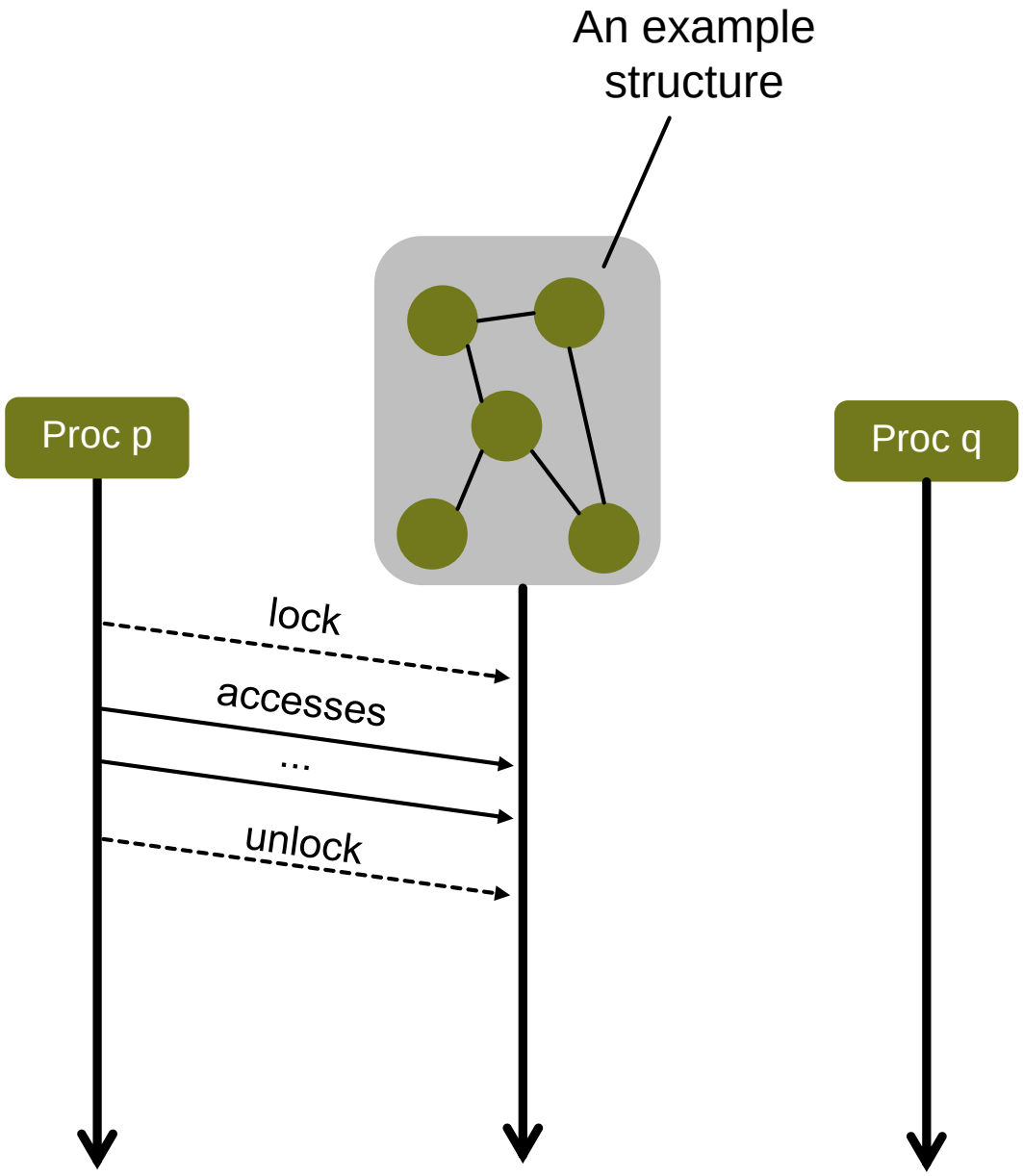

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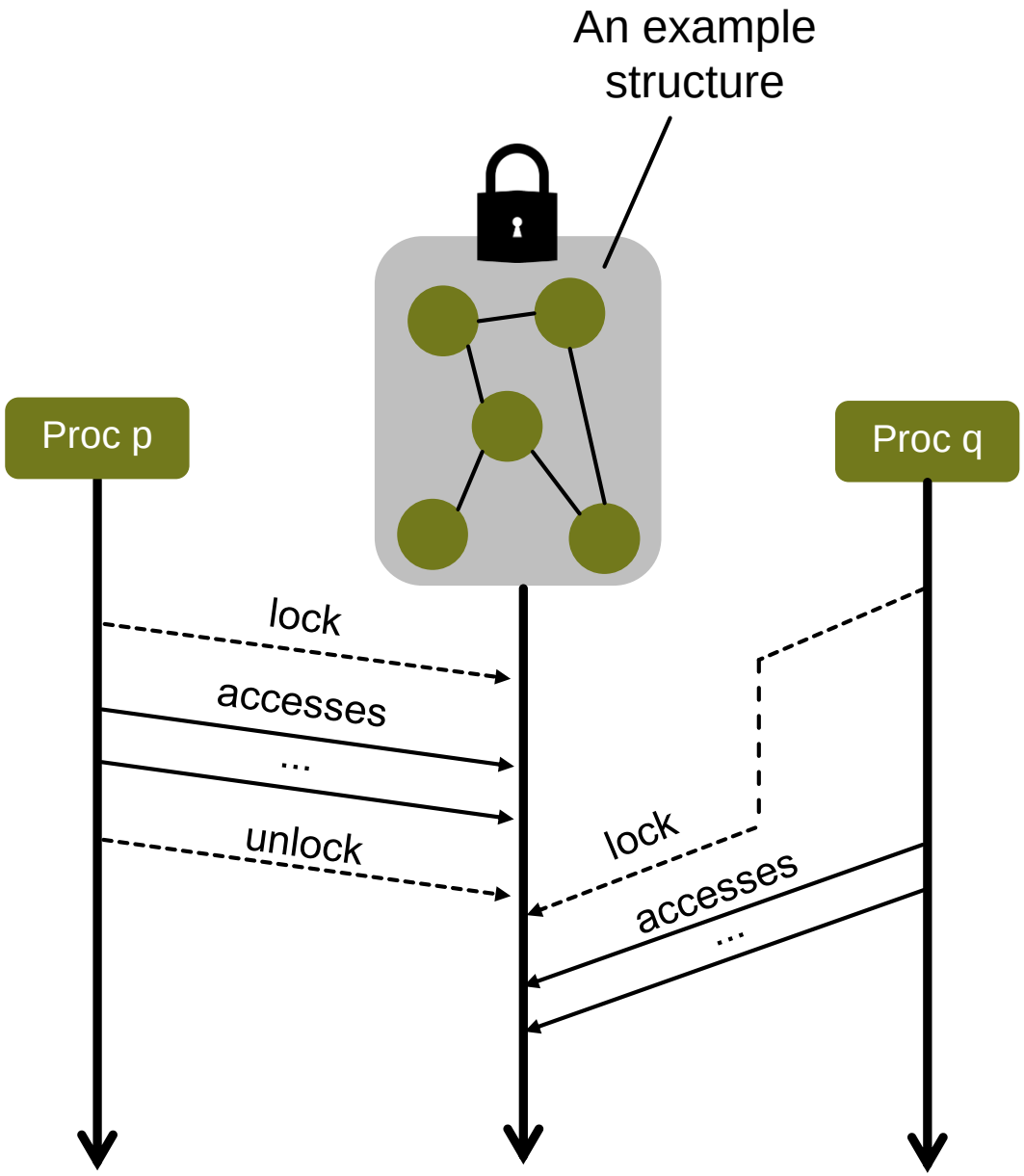
An example structure
Proc p
Proc q
lock
accesses
...
unlock
lock
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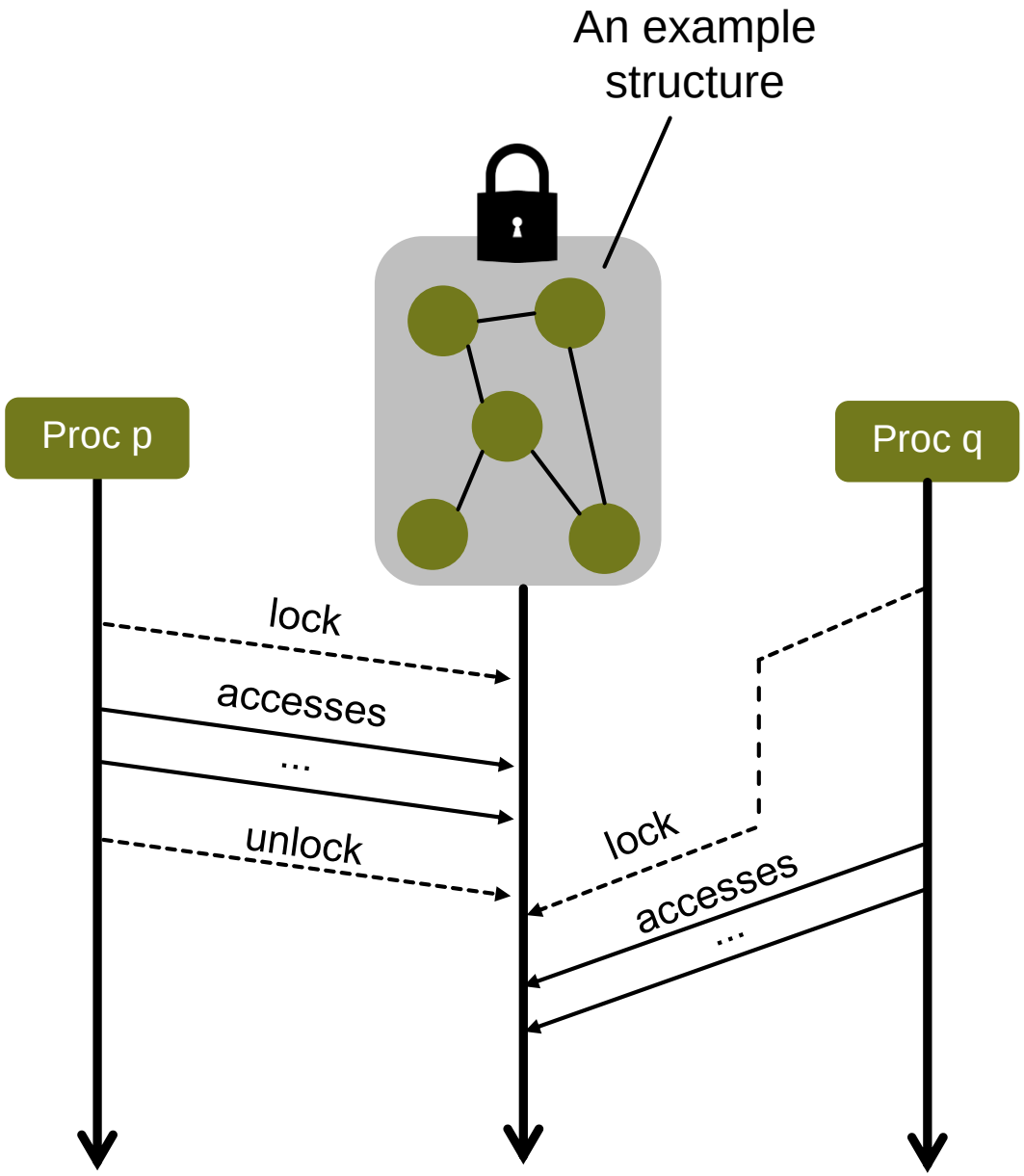
Locks


Inuitive
semantics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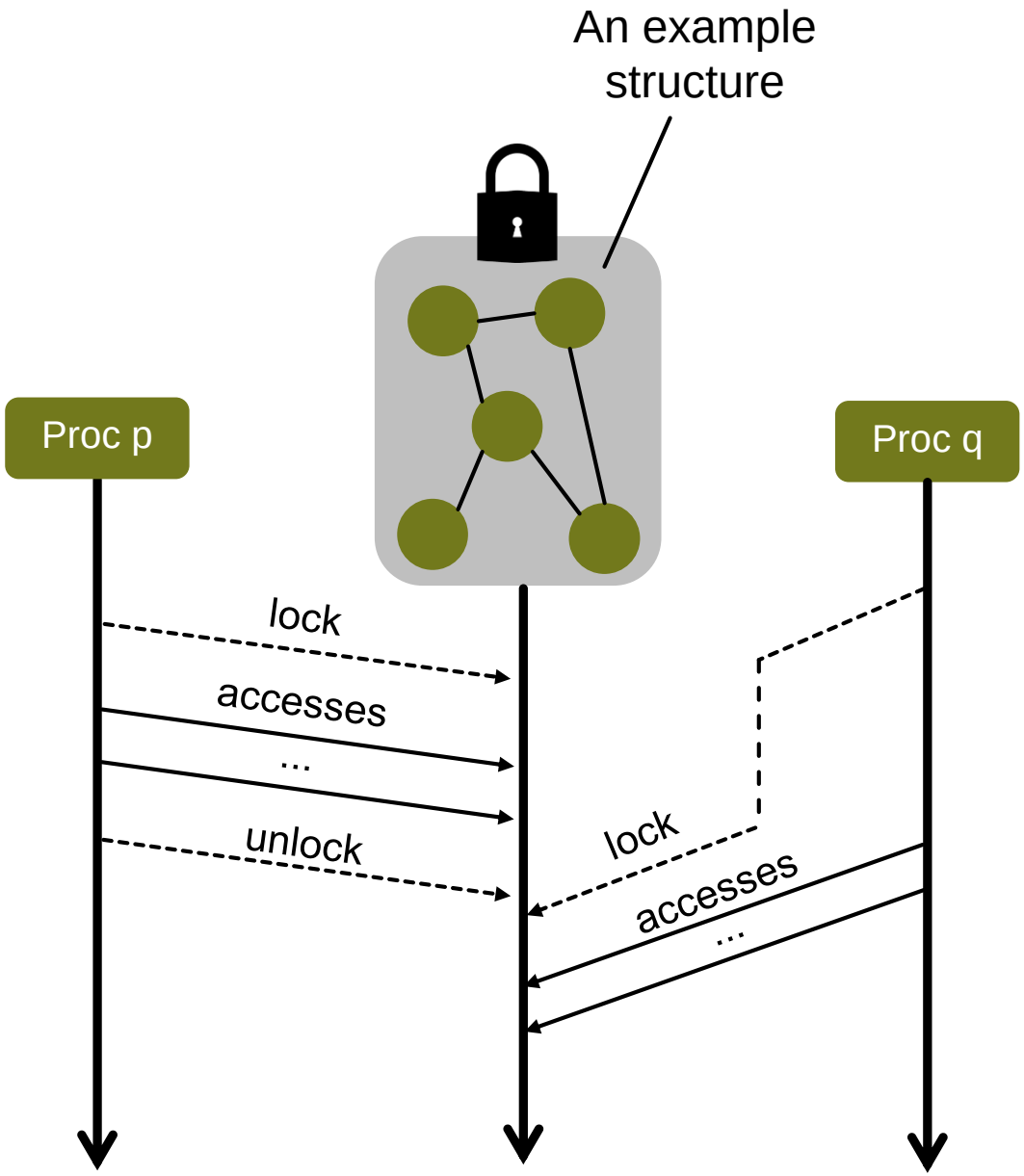
Inuitive semantics

Various performance penalties



LOCKS: CHALLENGES

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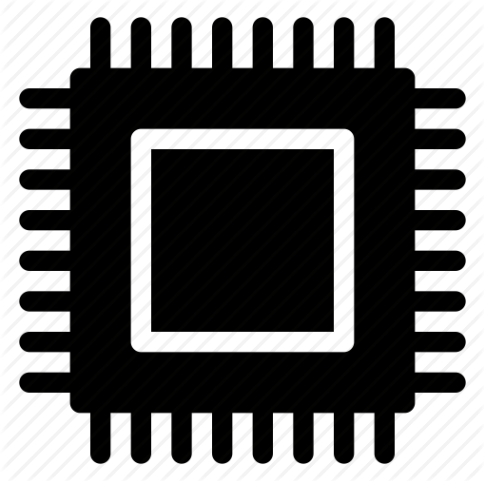

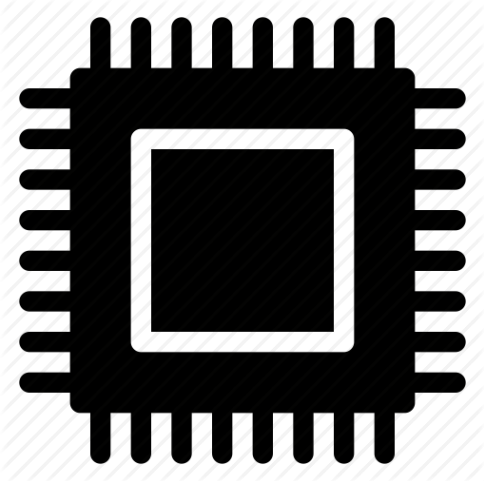

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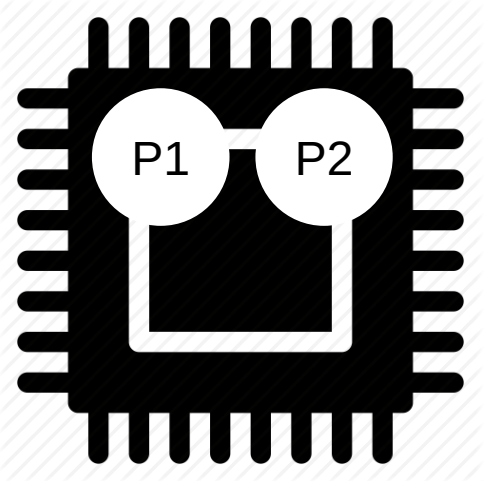

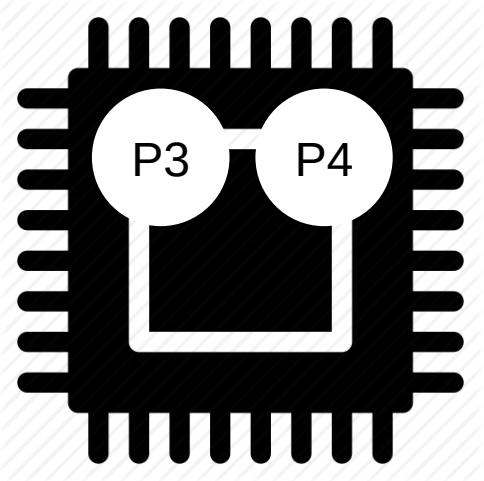

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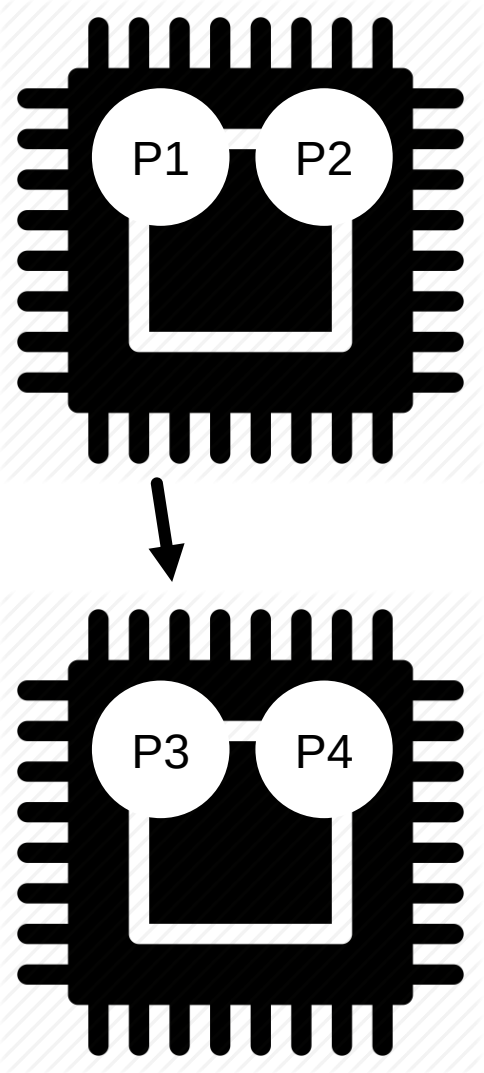

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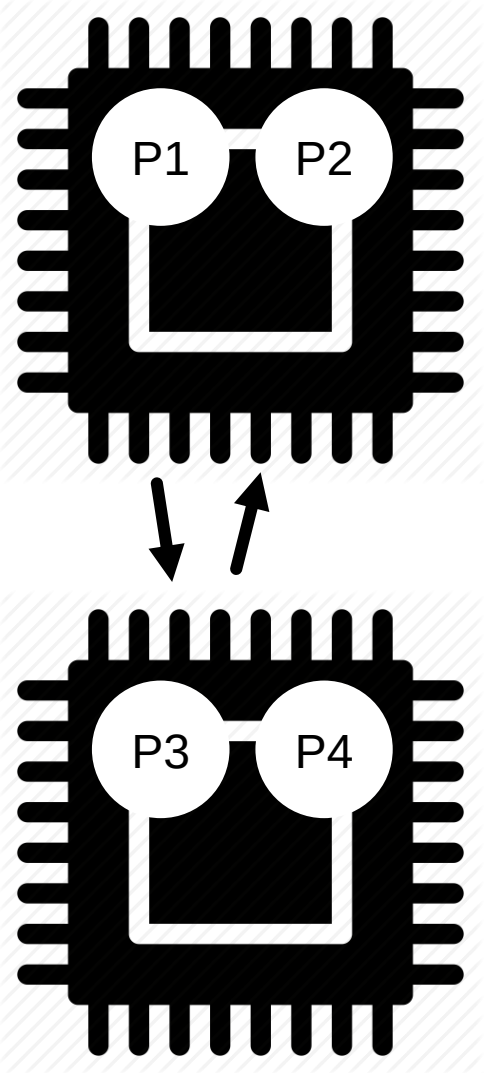

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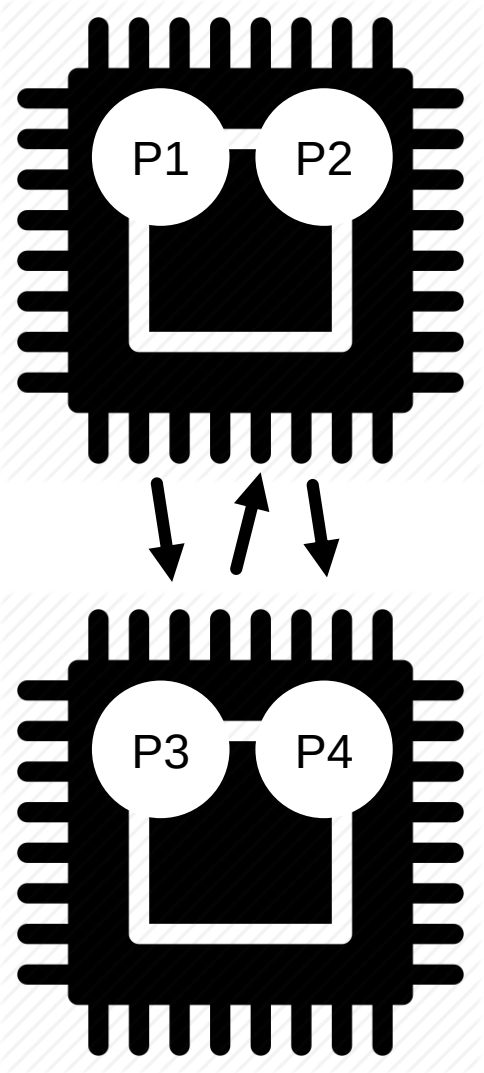

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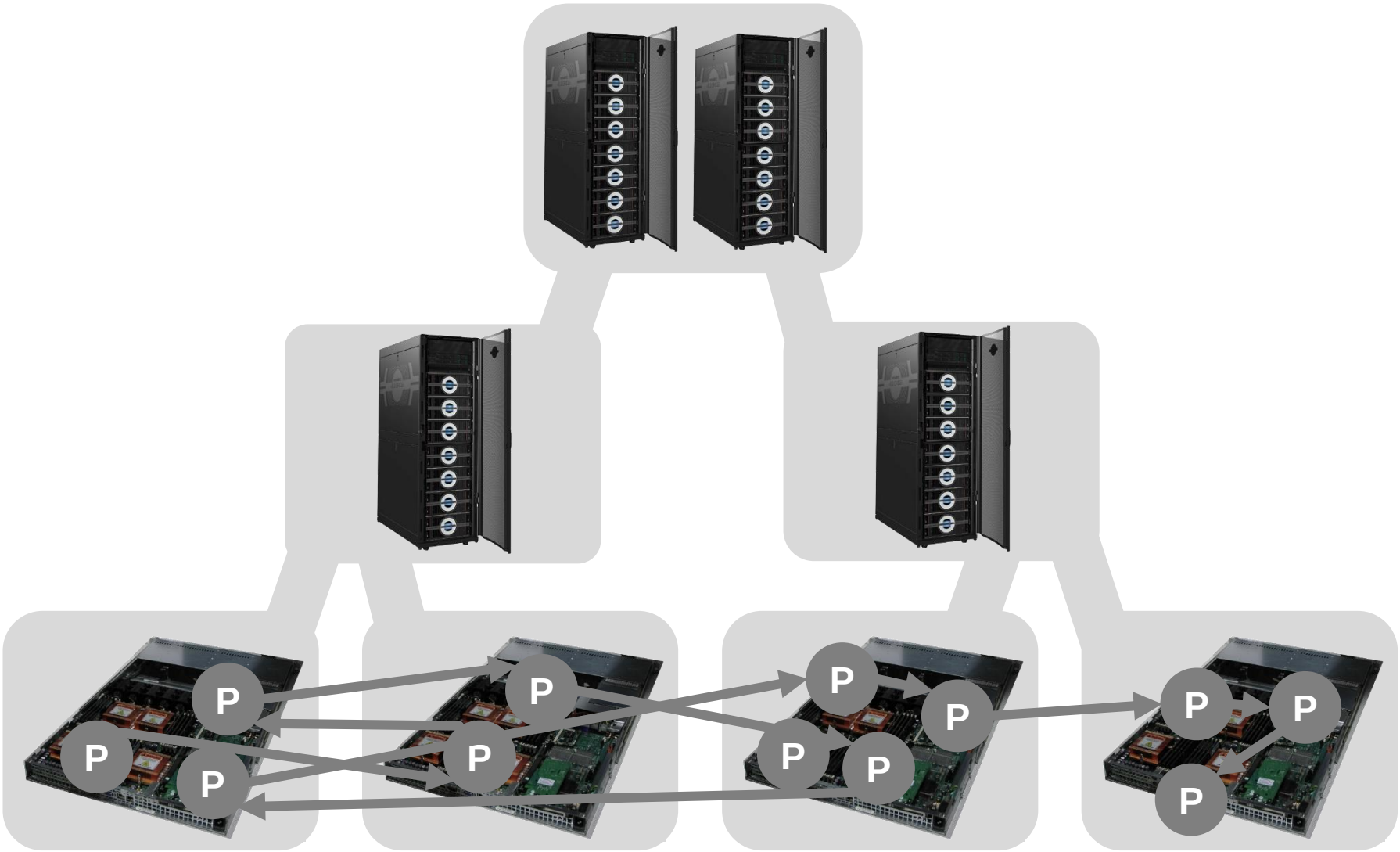

LOCKS: CHALLENGES

We need intra- and inter-node topology-awareness

We need to cover arbitrary topologies

LOCKS: CHALLENGES

LOCKS: CHALLENGES

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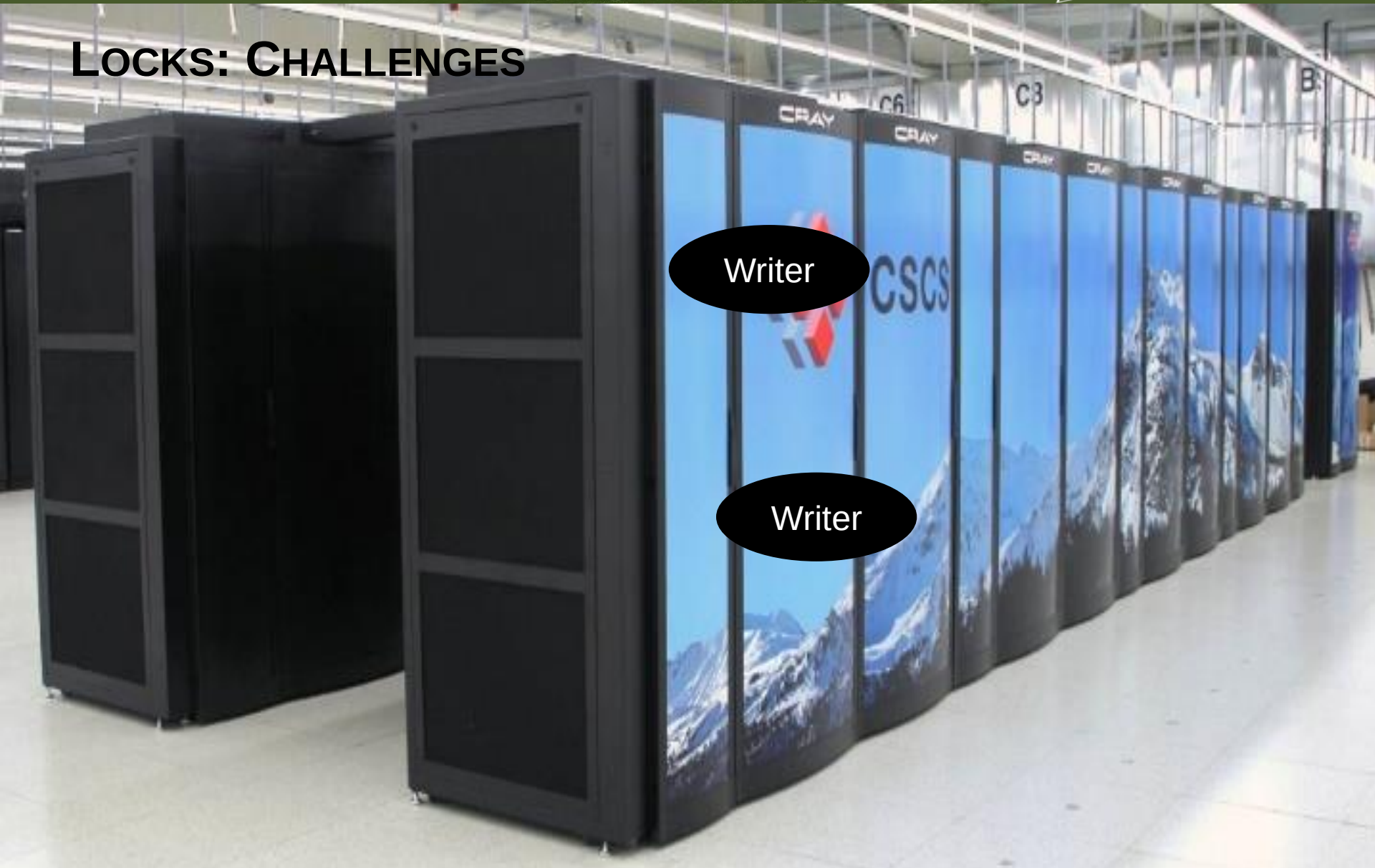
[1] V. Venkataramani et al. Tao: How facebook serves the social graph. SIGMOD'12.

LOCKS: CHALLENGES



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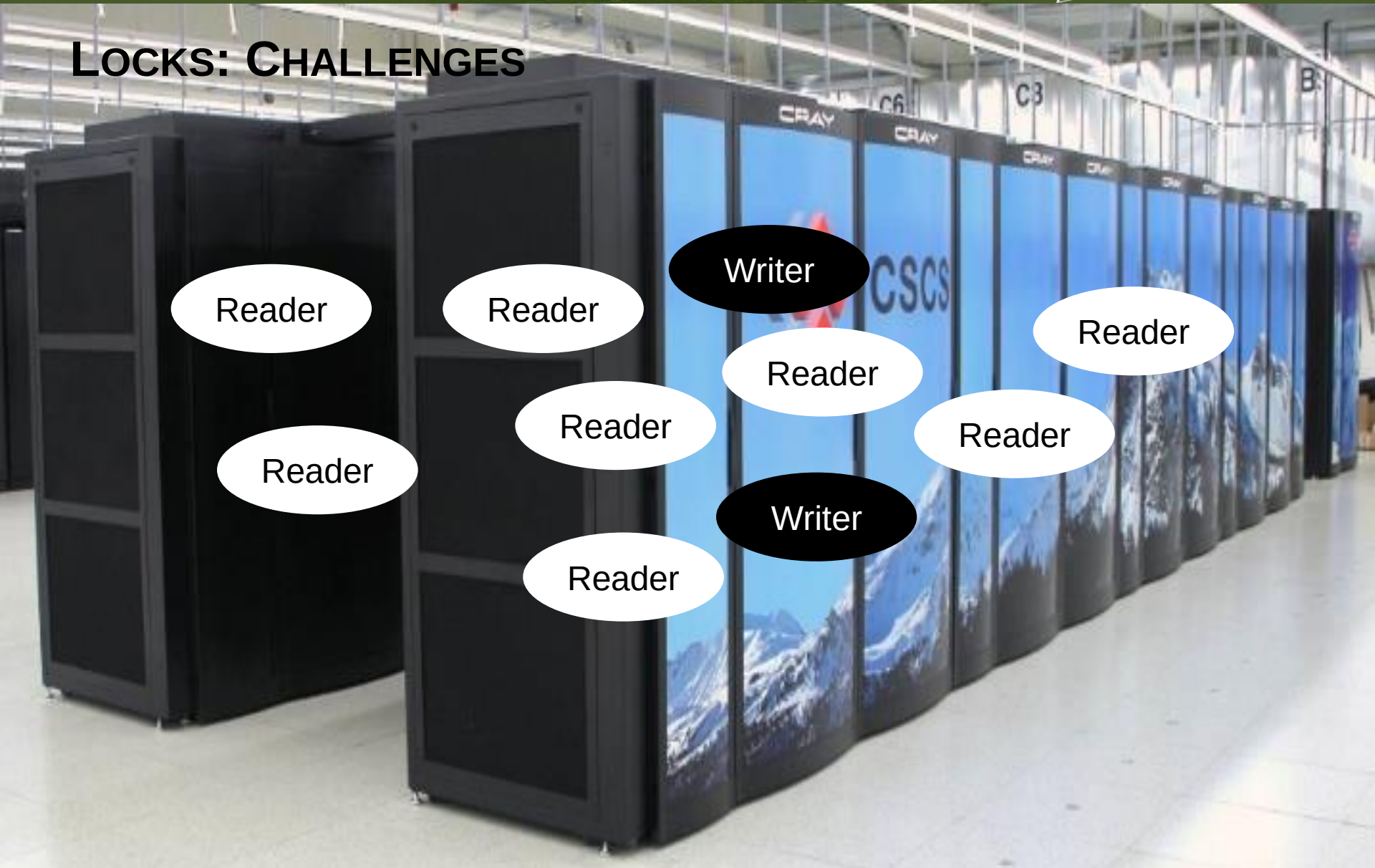

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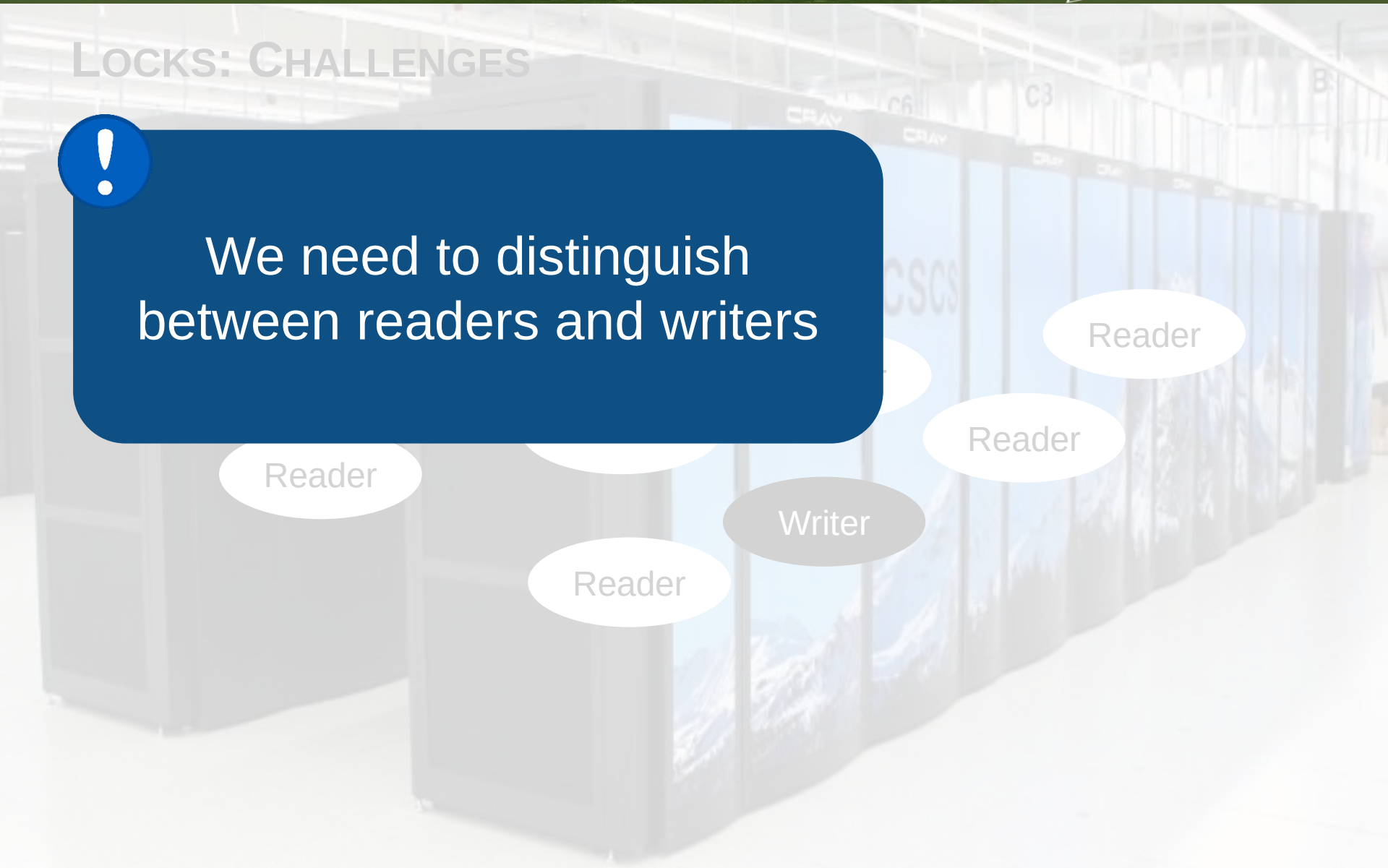
LOCKS: CHALLENGES

We need to distinguish between readers and writers



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Locks: Challenges

We need to distinguish between readers and writers

Reader

Reader

Reader

Writer

We need flexible performance for both types of processes

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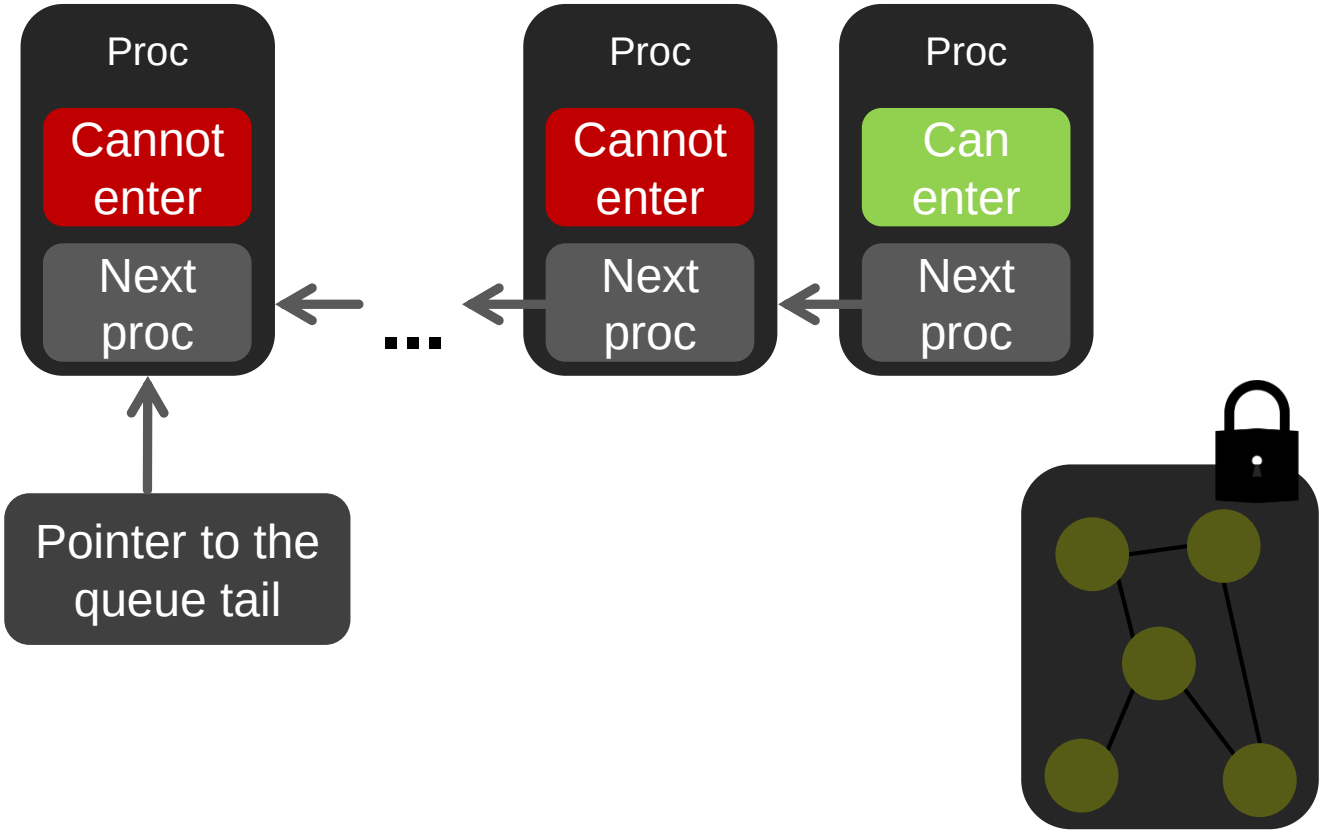
What will we use in the design?

What we will use
MCS Locks



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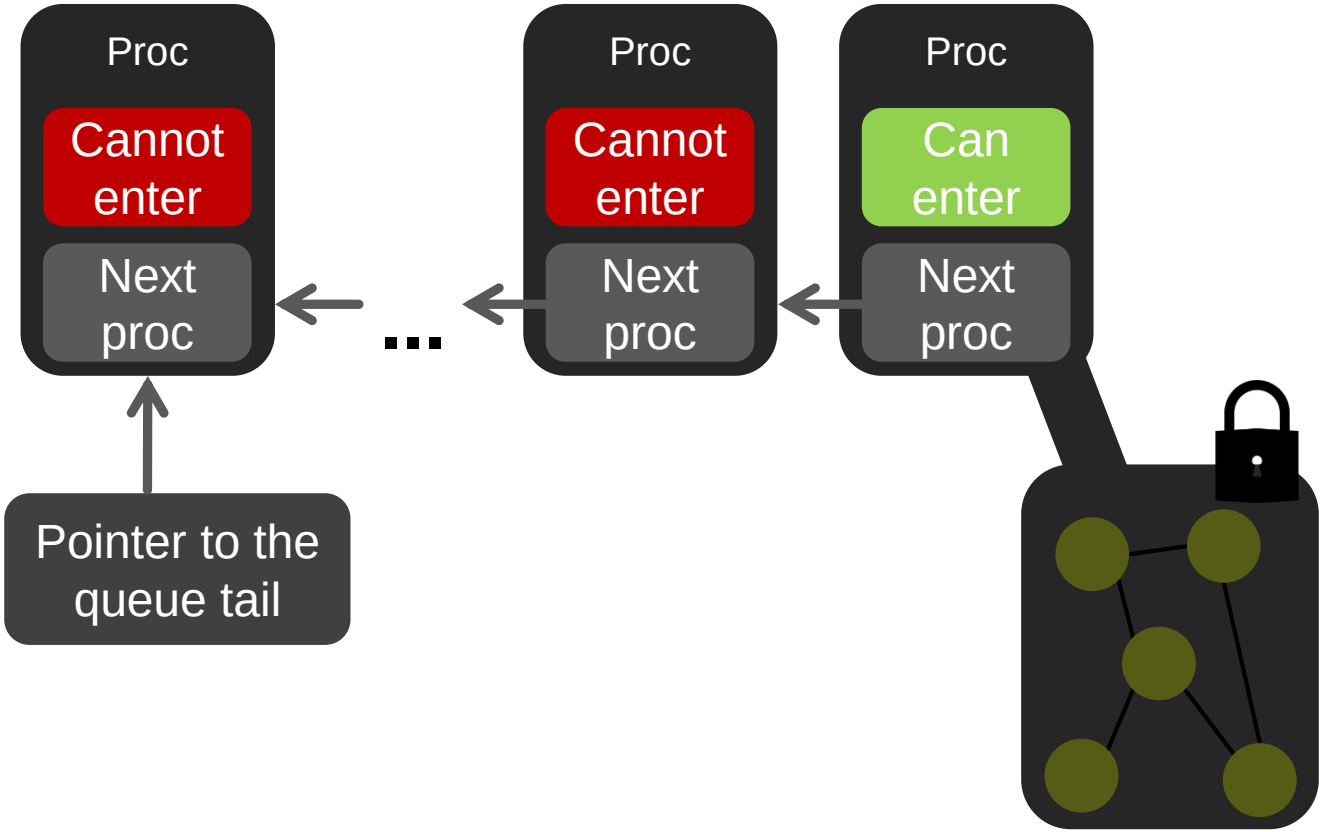

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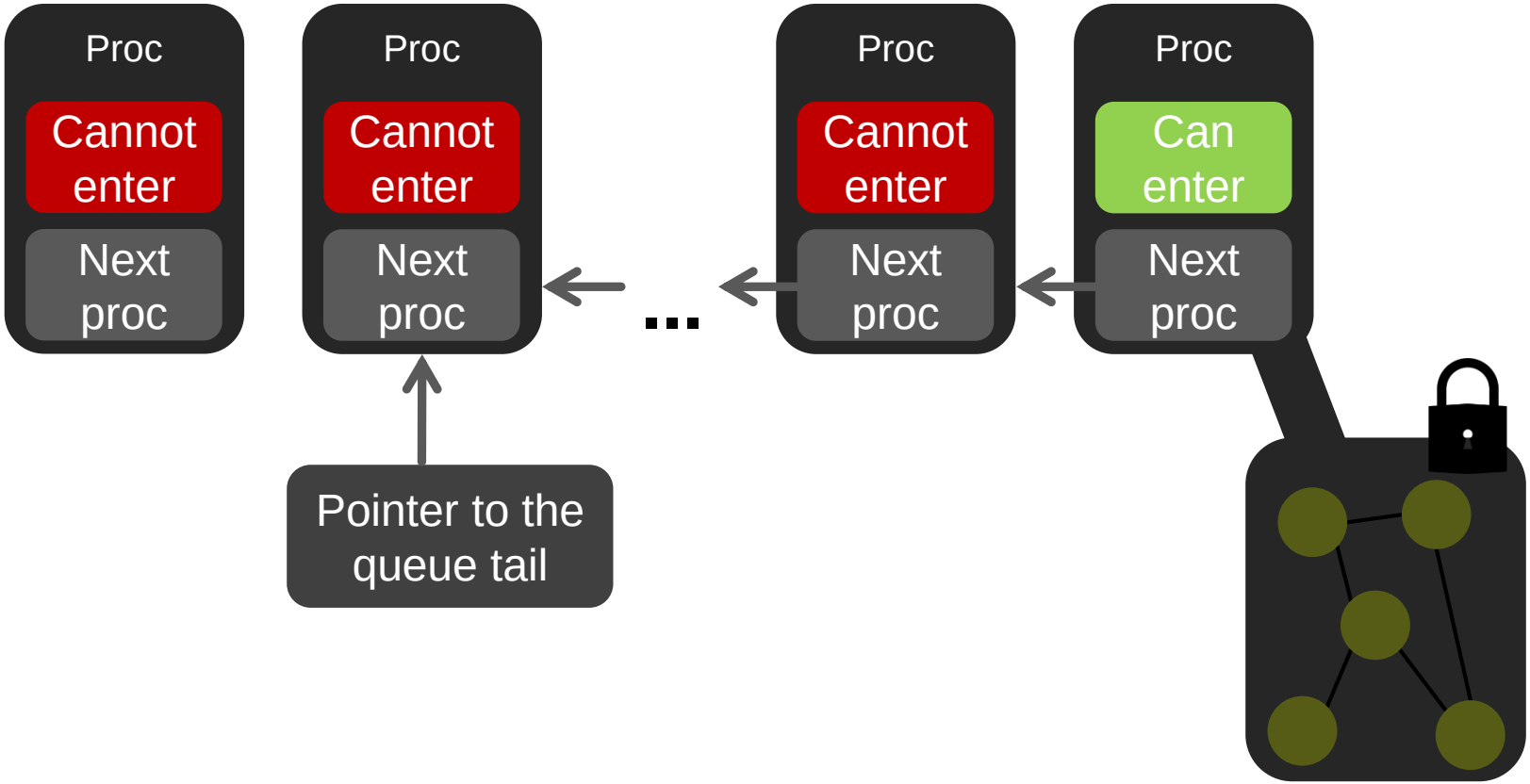

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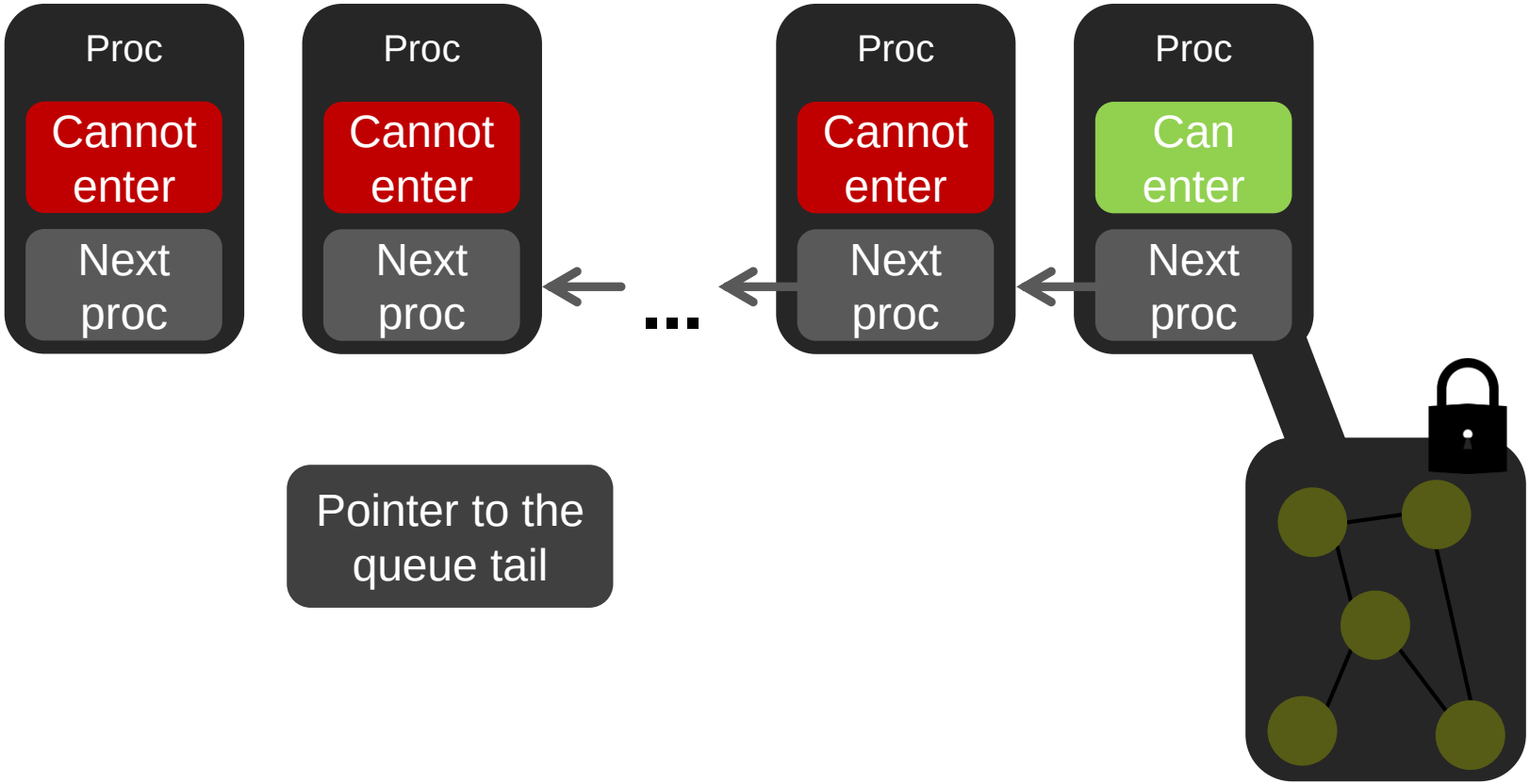

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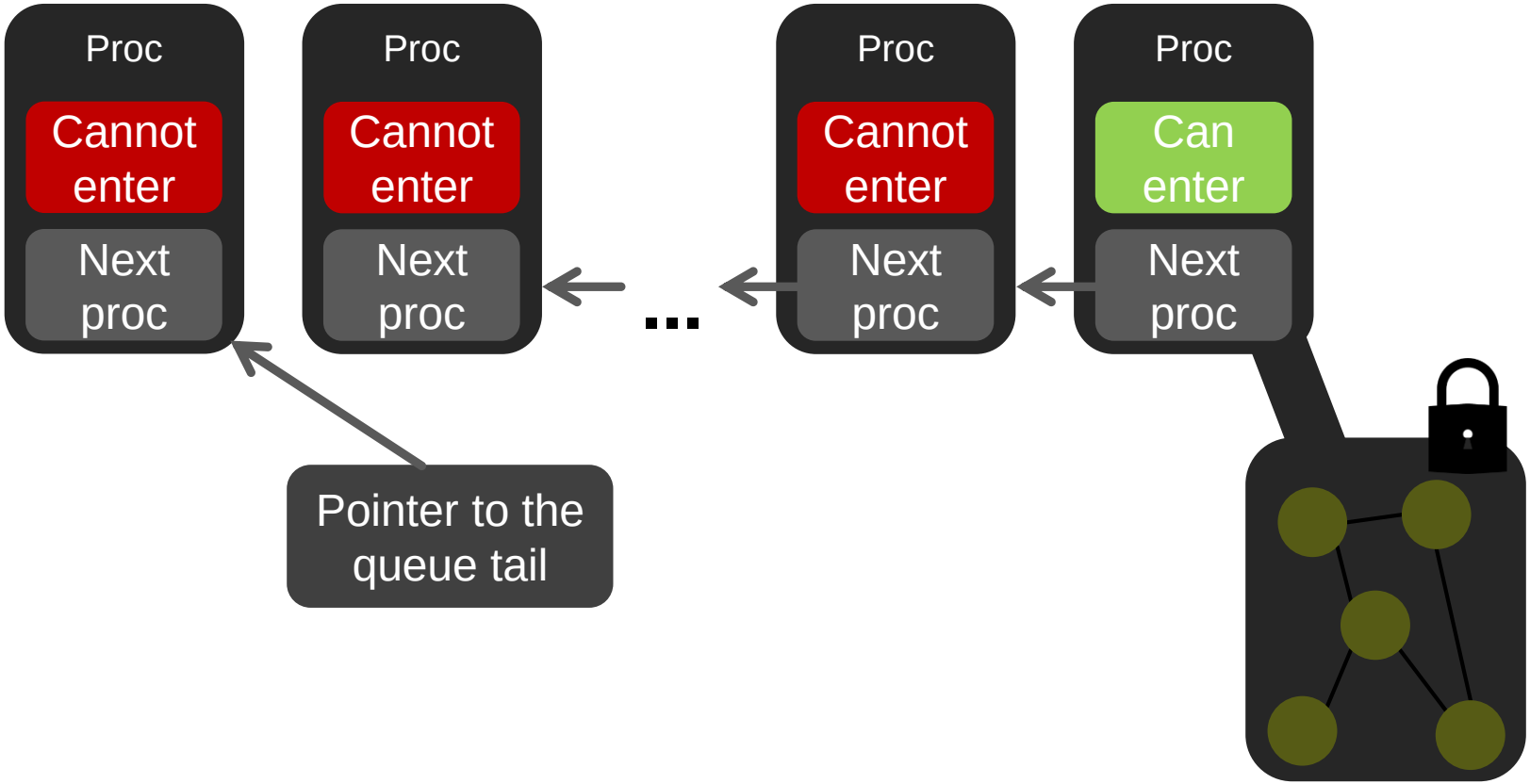

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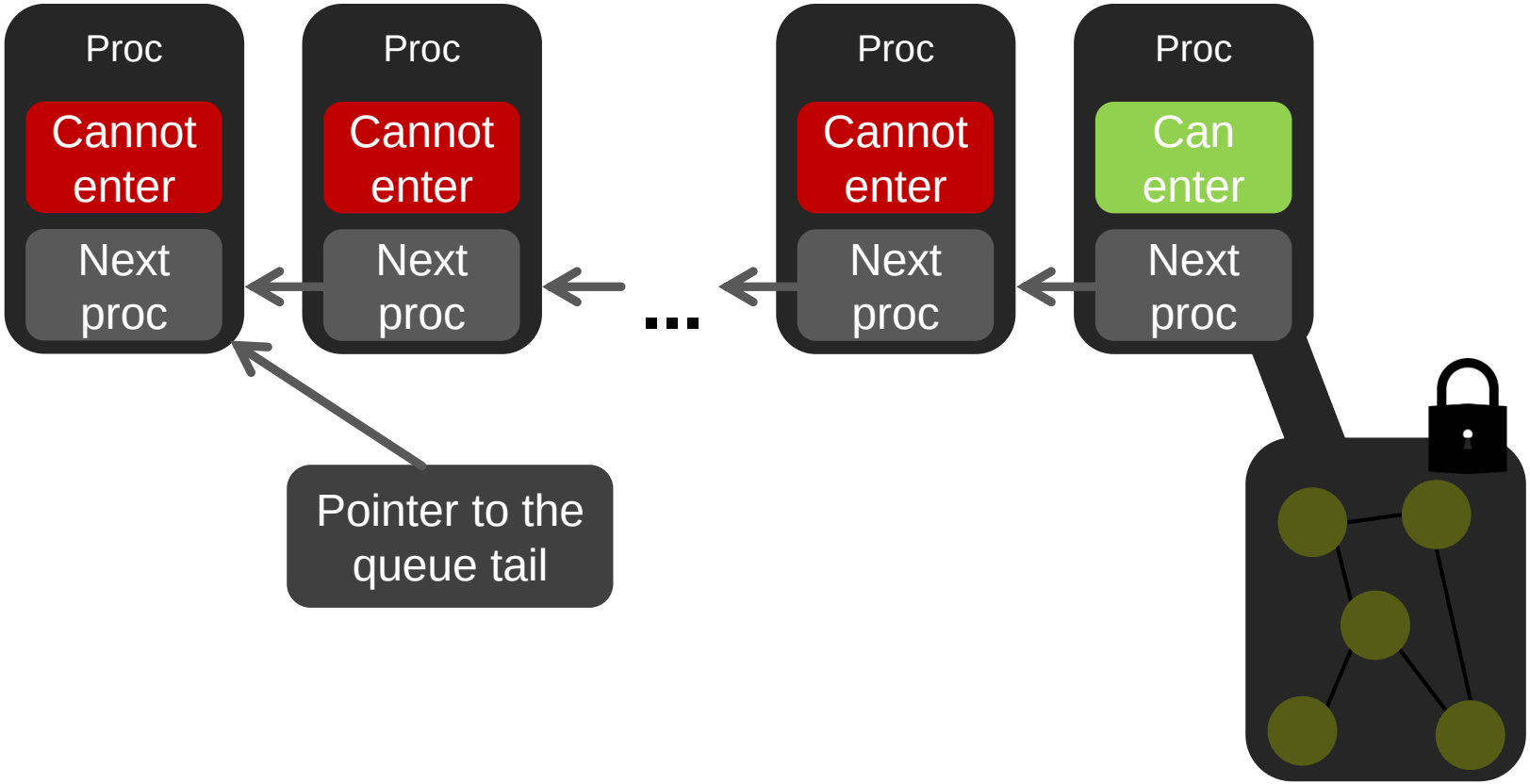

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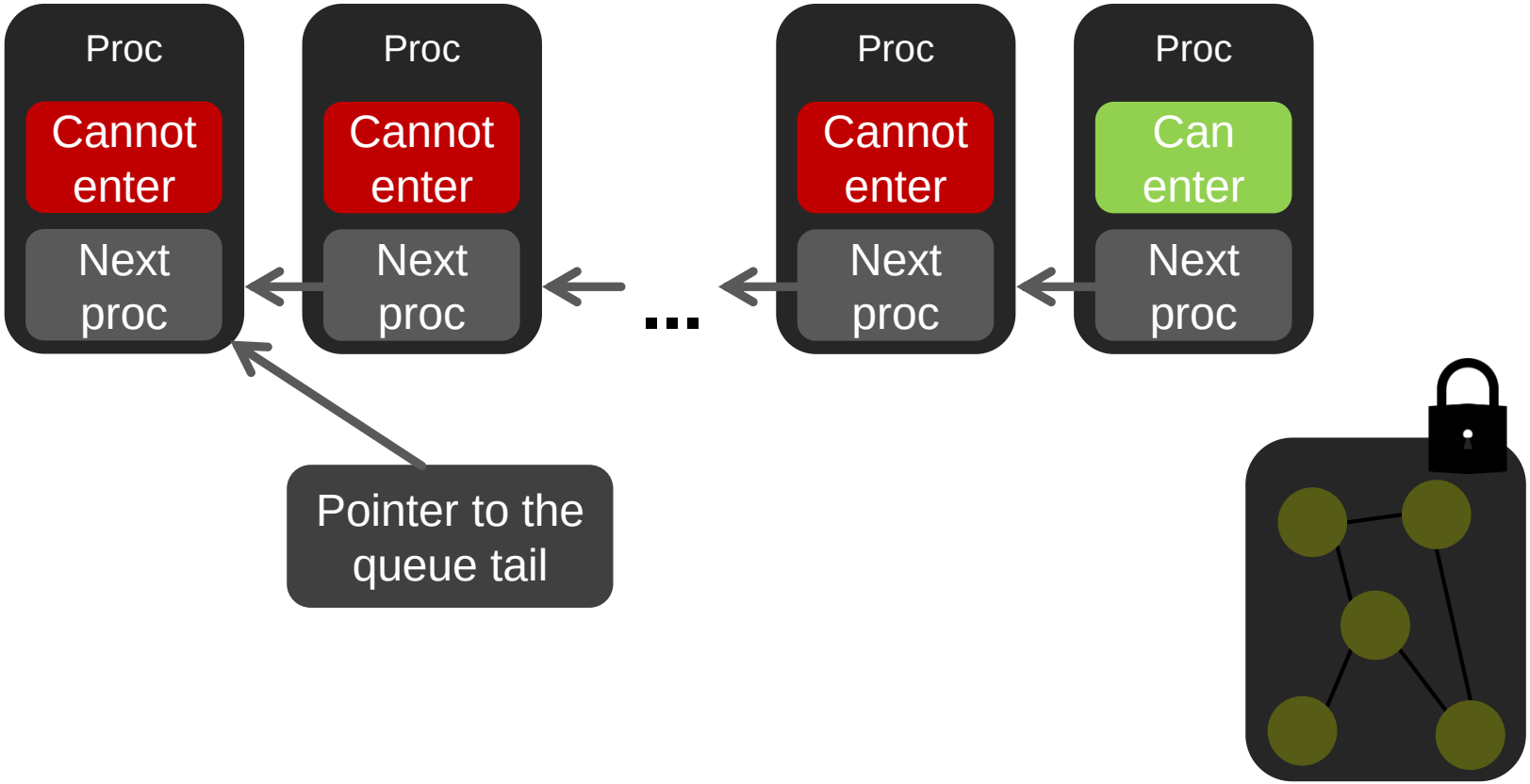

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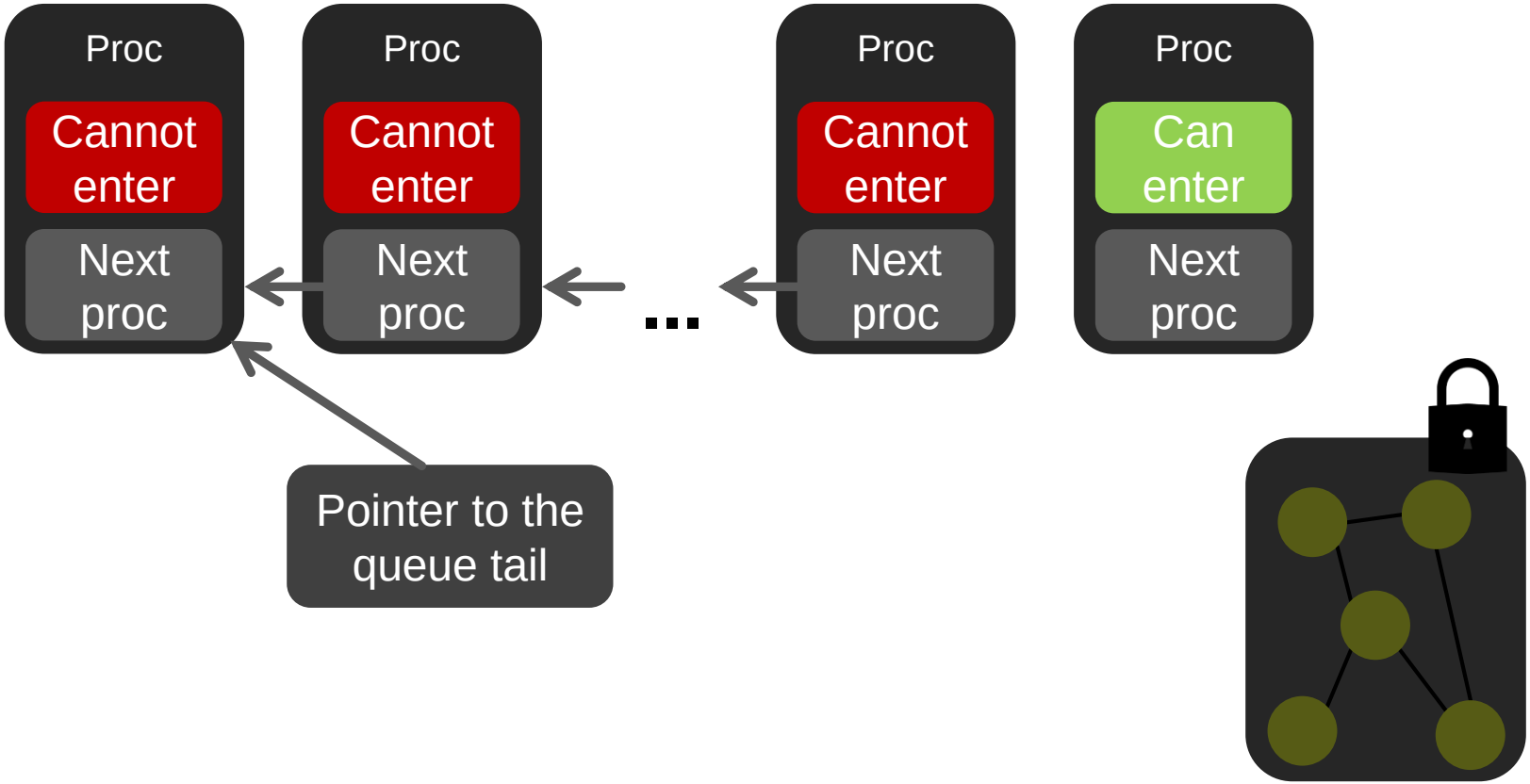

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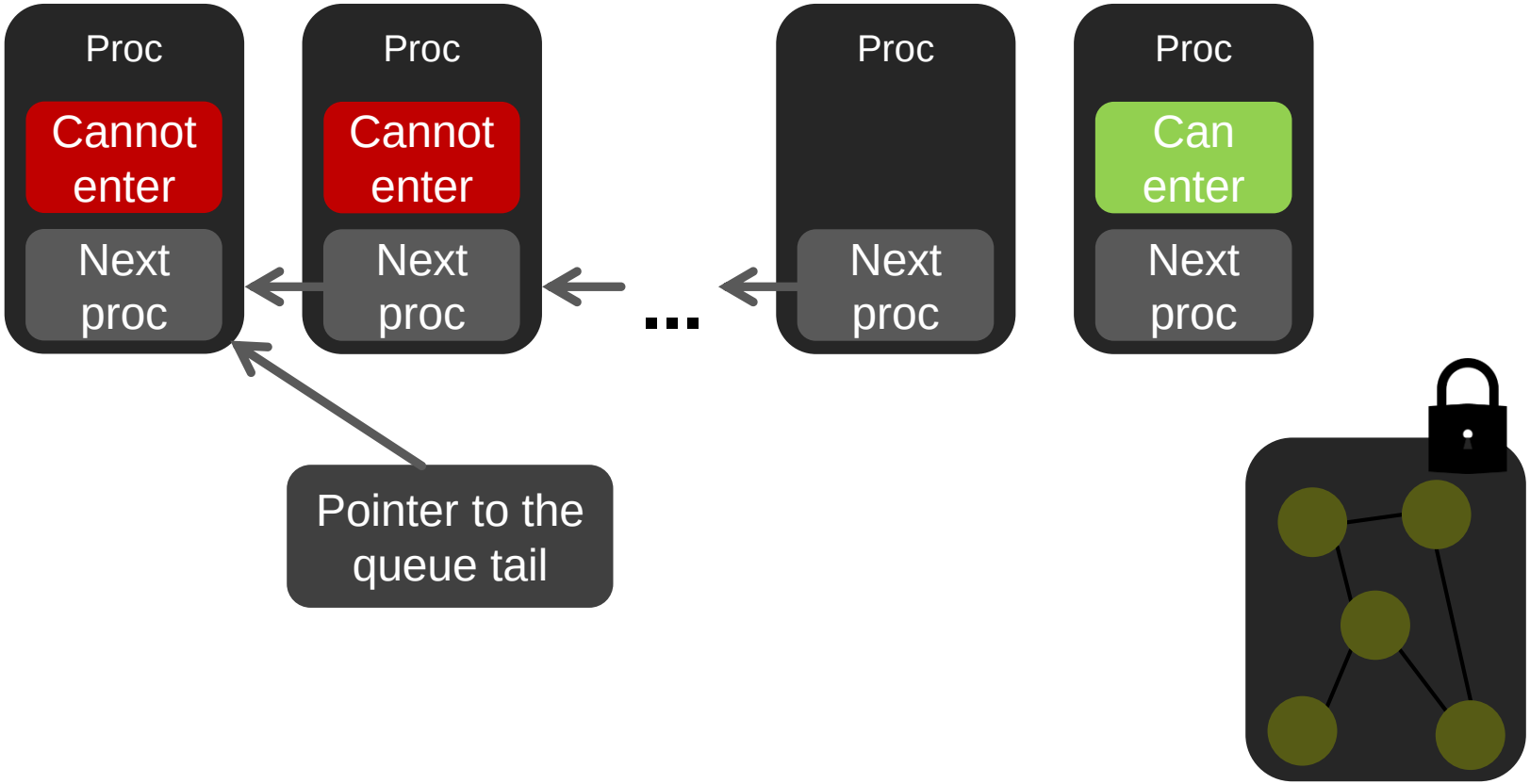

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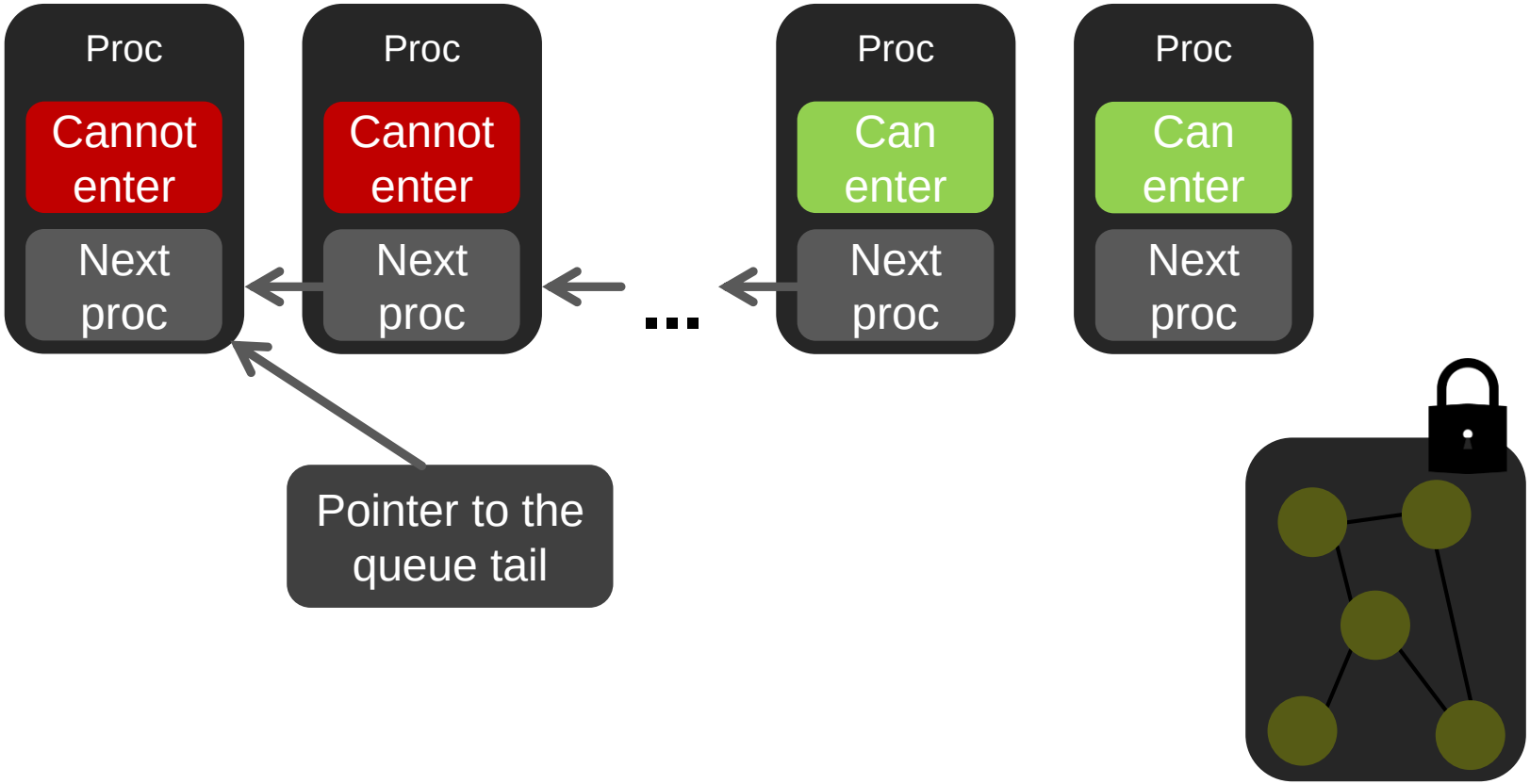

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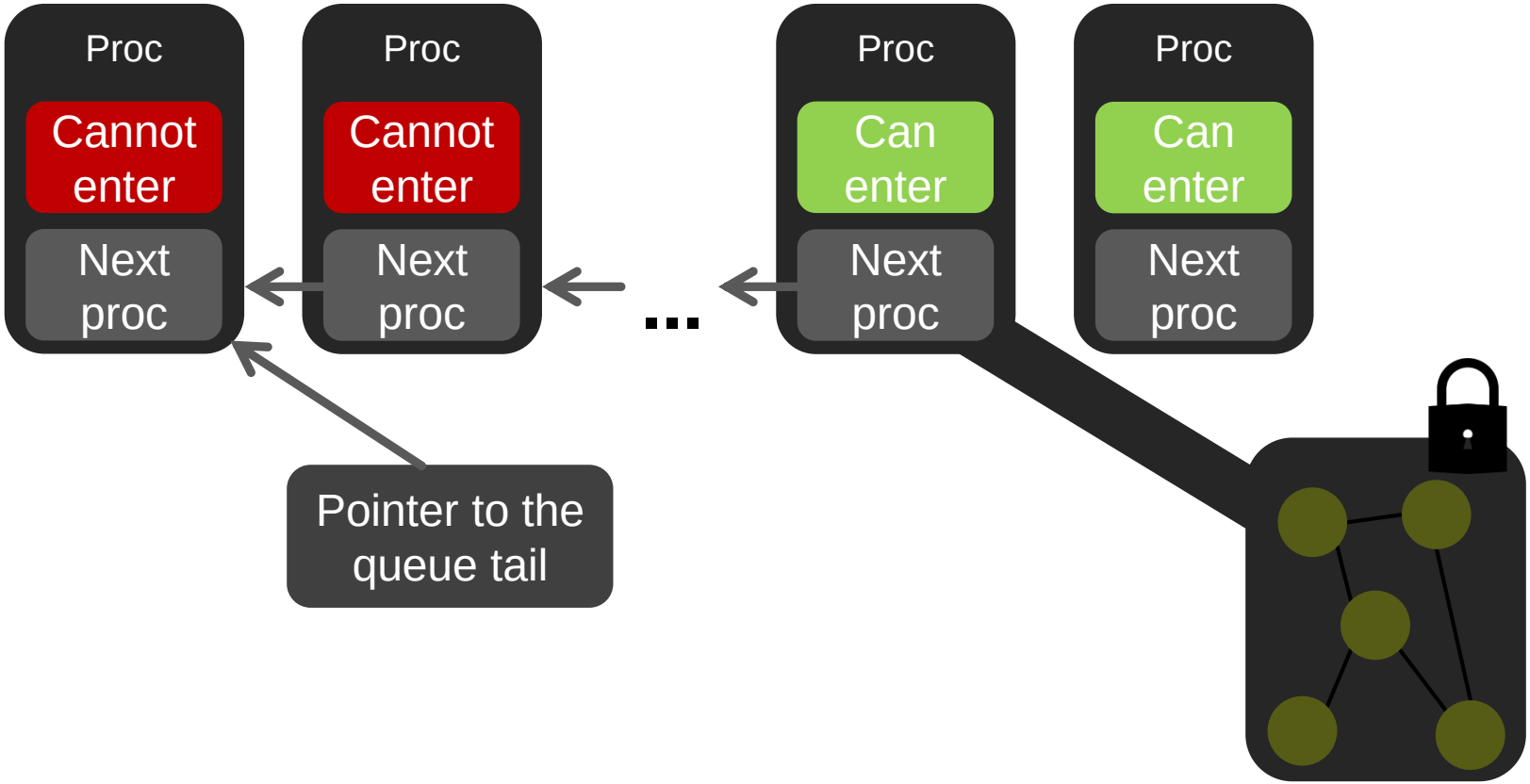

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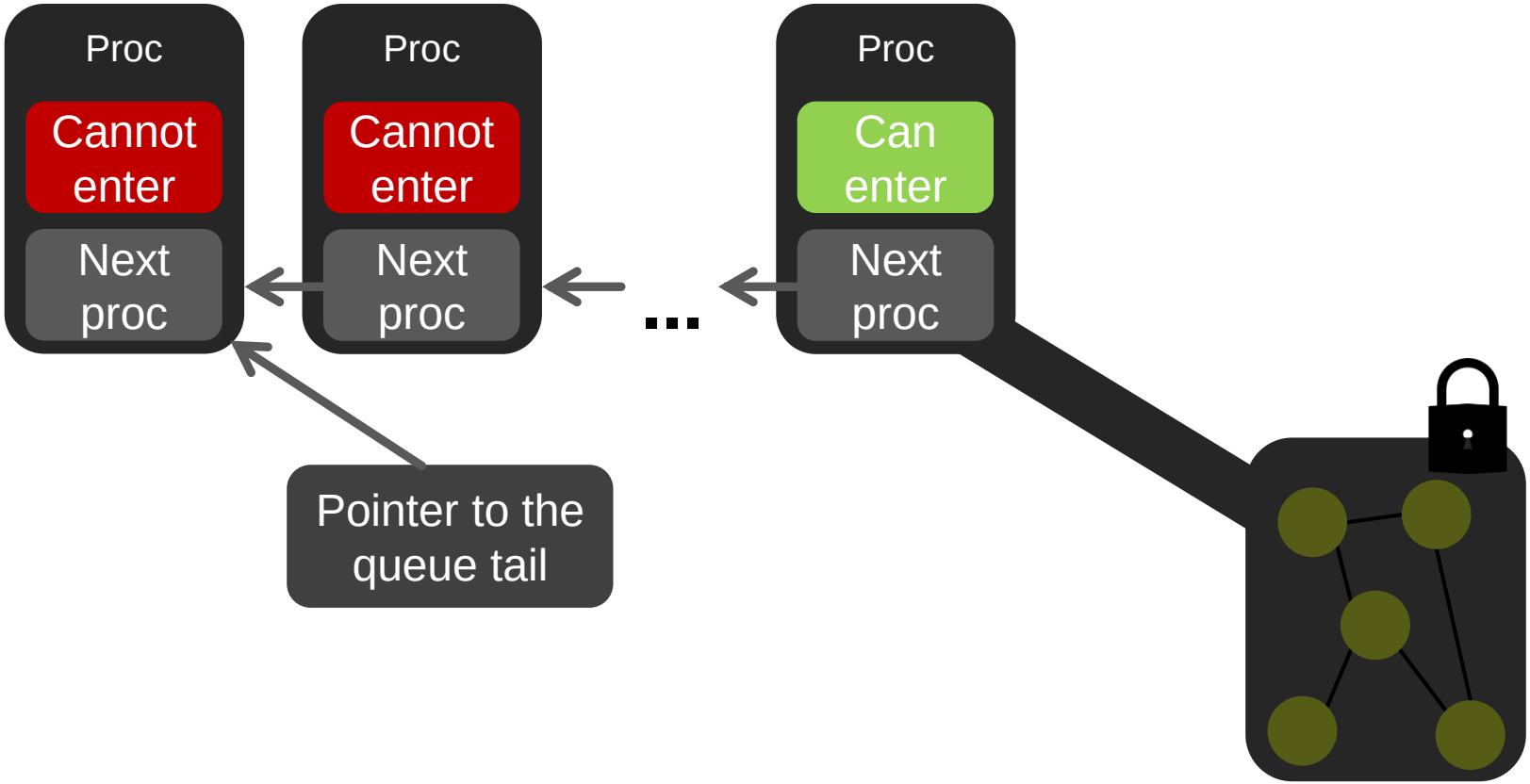
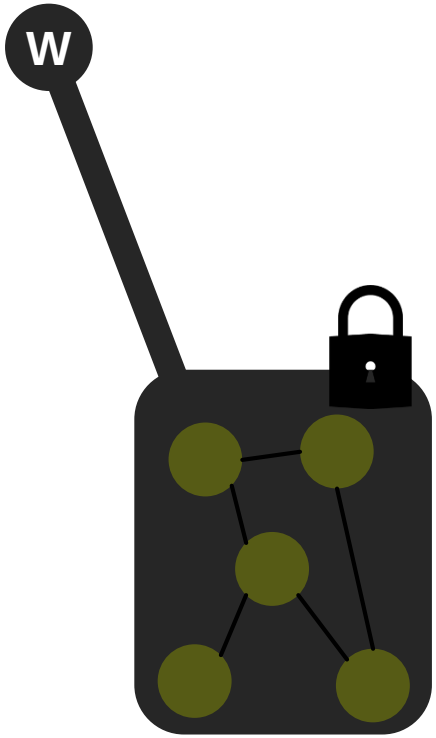


What we will use
Reader-Writer Locks



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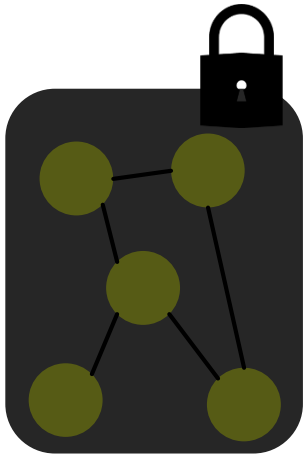

WHAT WE WILL USE
Reader-Writer Locks

R

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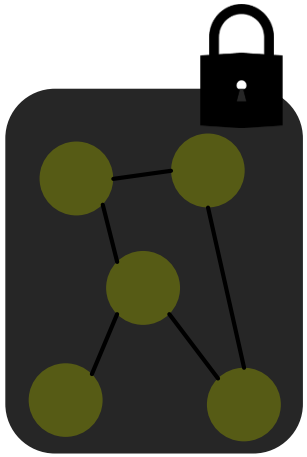

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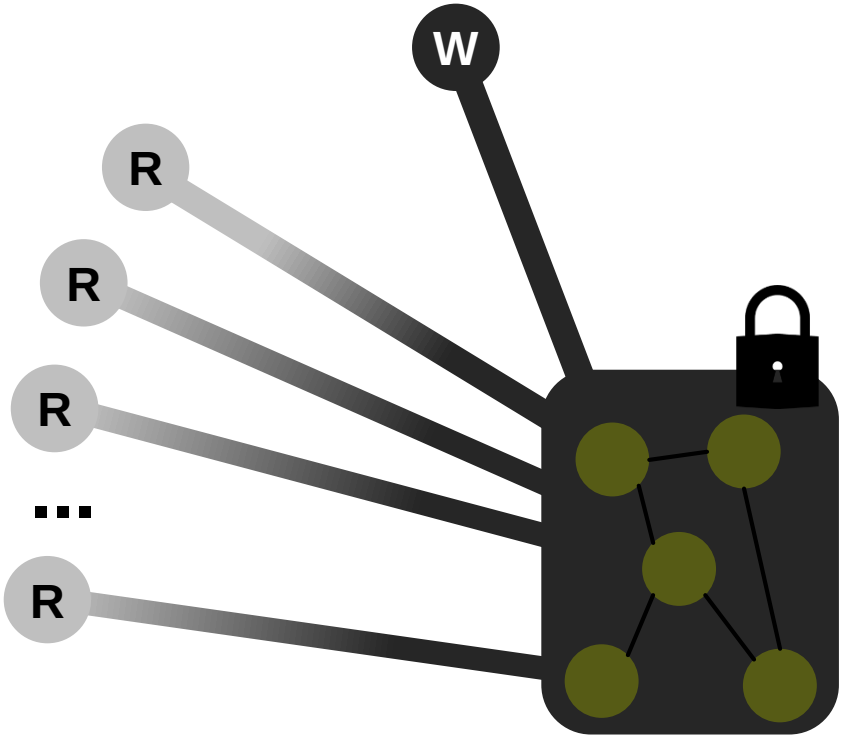

How to manage the design complexity?

How to manage the design complexity?

What mechanism to use for efficient implementation?

How to manage the design complexity?

How to ensure tunable performance?

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Remote Memory Access (RMA) Programming

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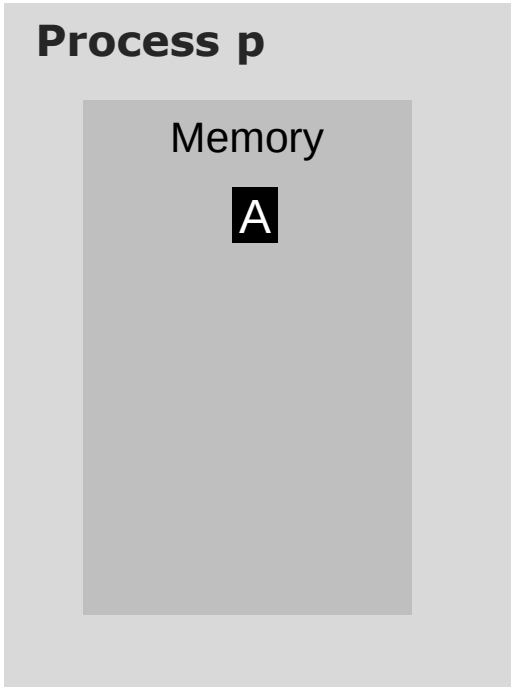

Remote Memory Access (RMA) Programming

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Process p

Memory

A

Process q

Memory

B

Cray BlueWaters

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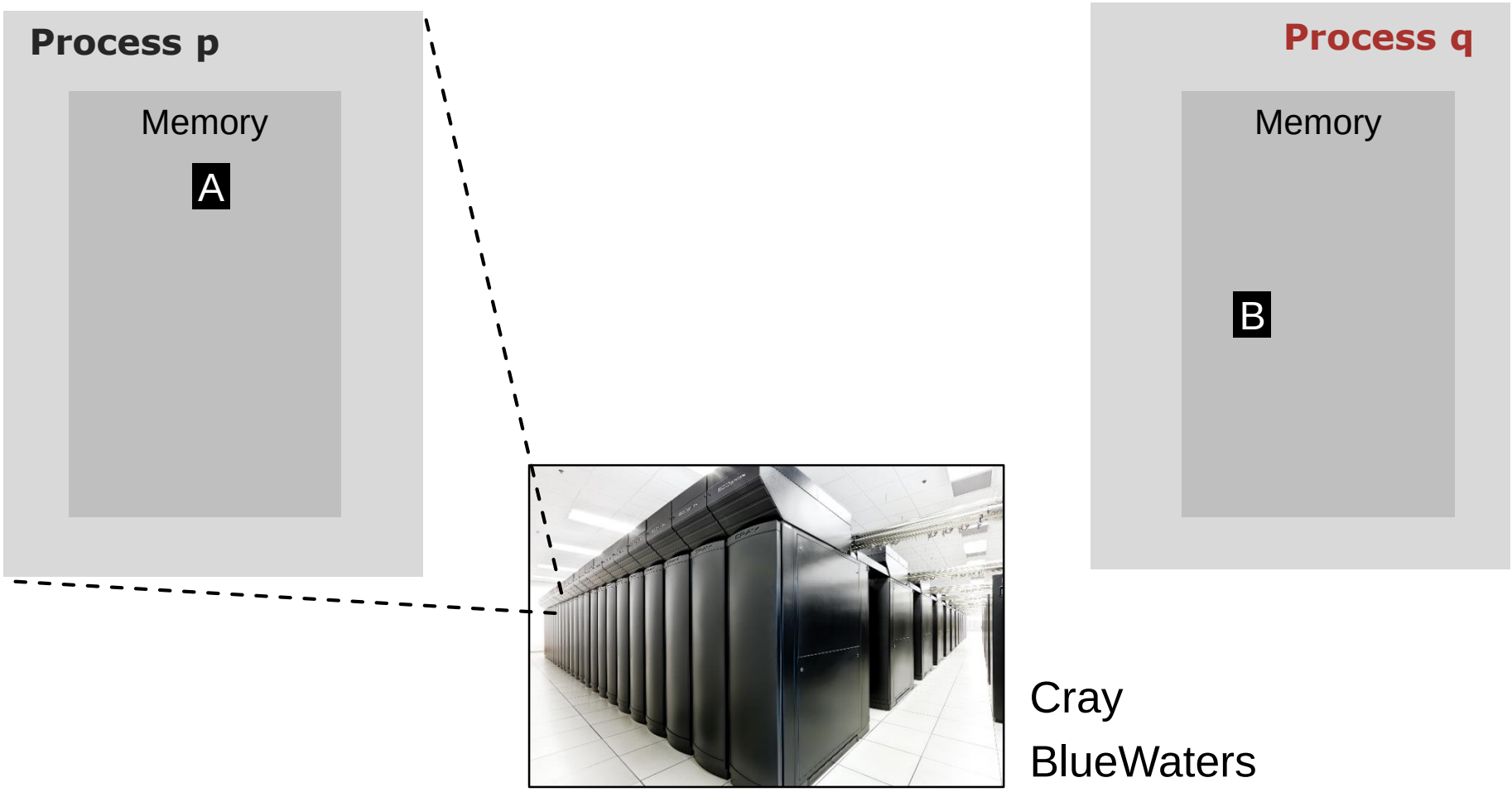

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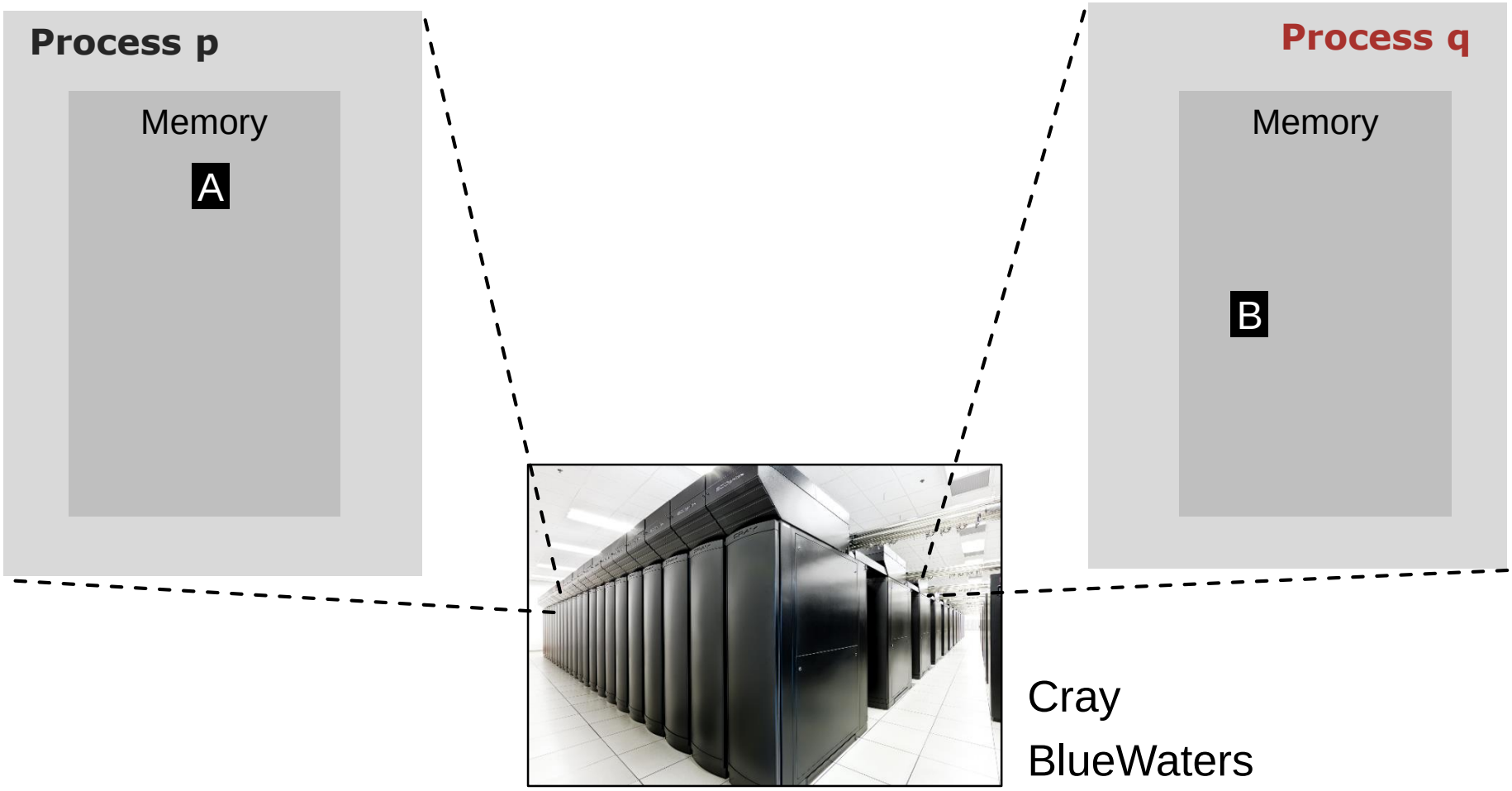

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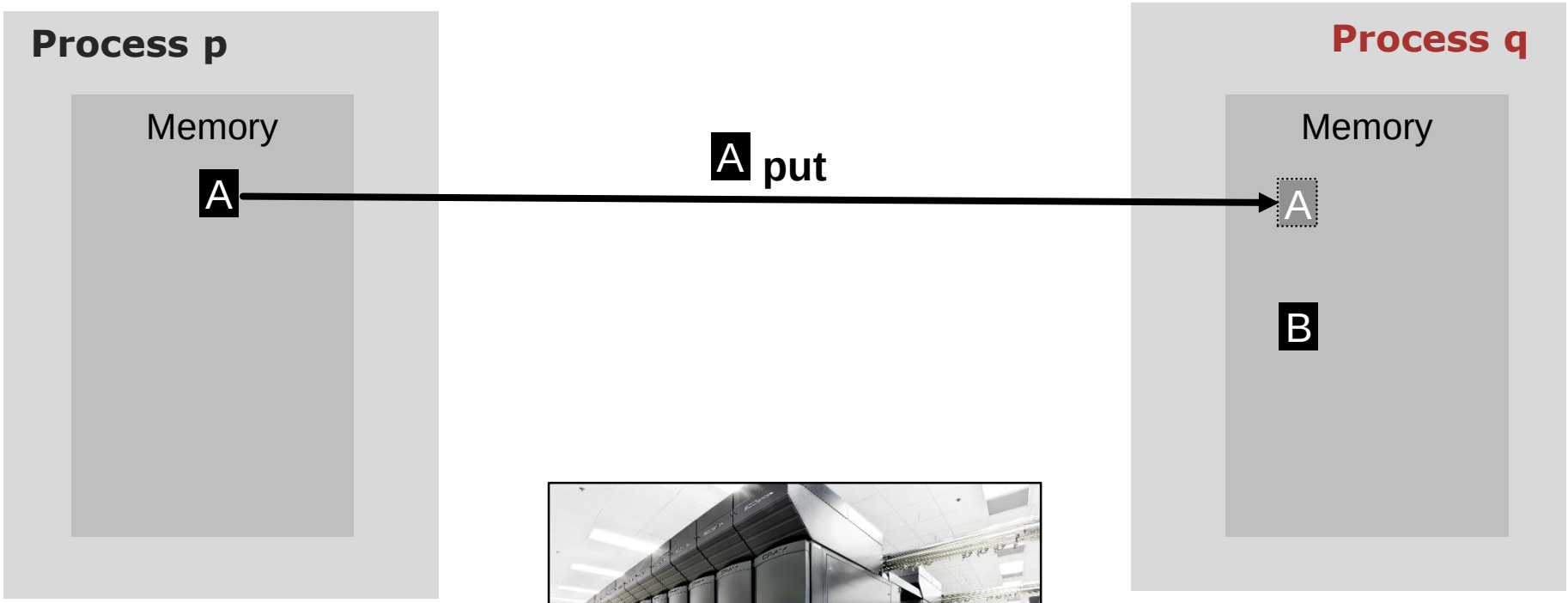

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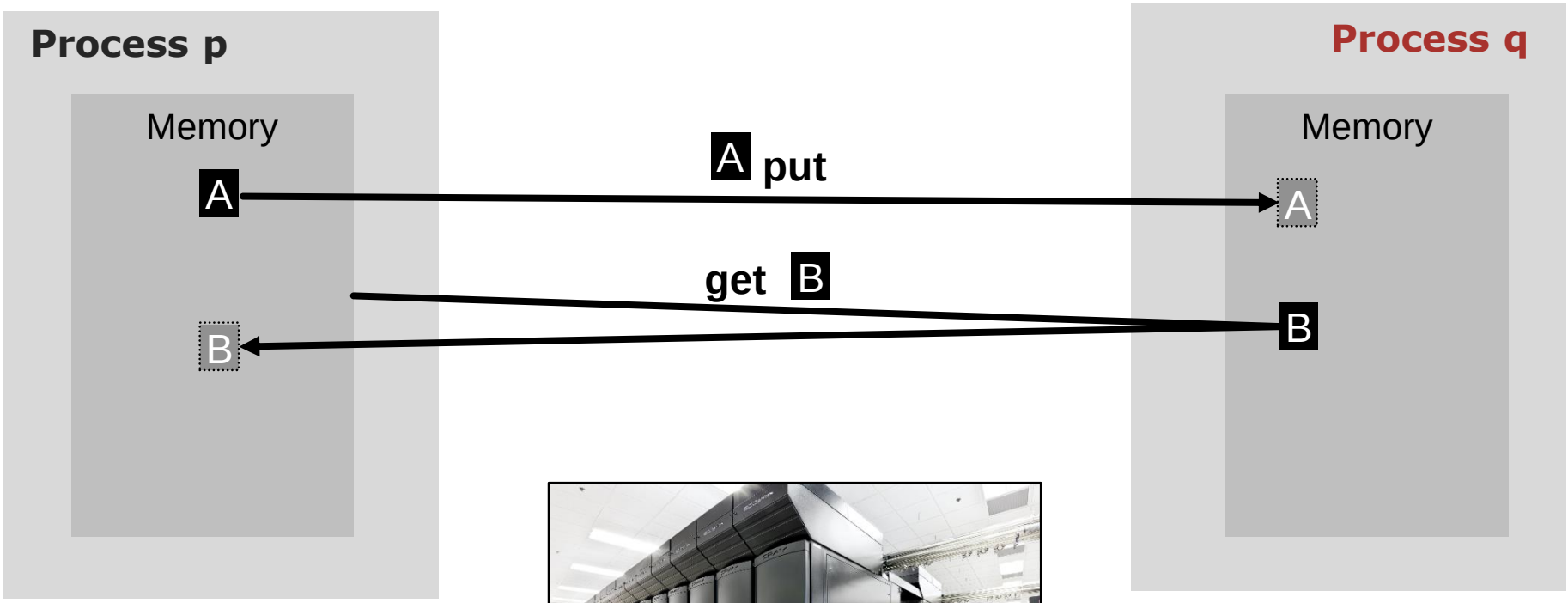

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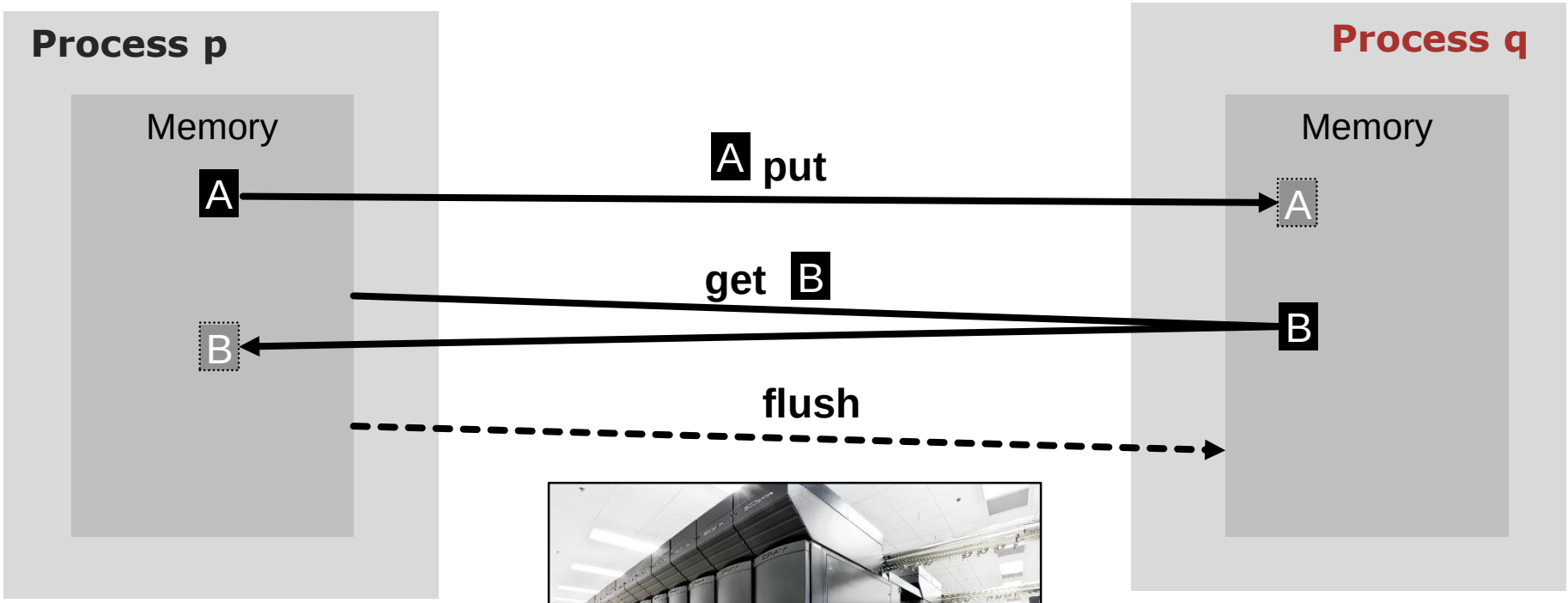

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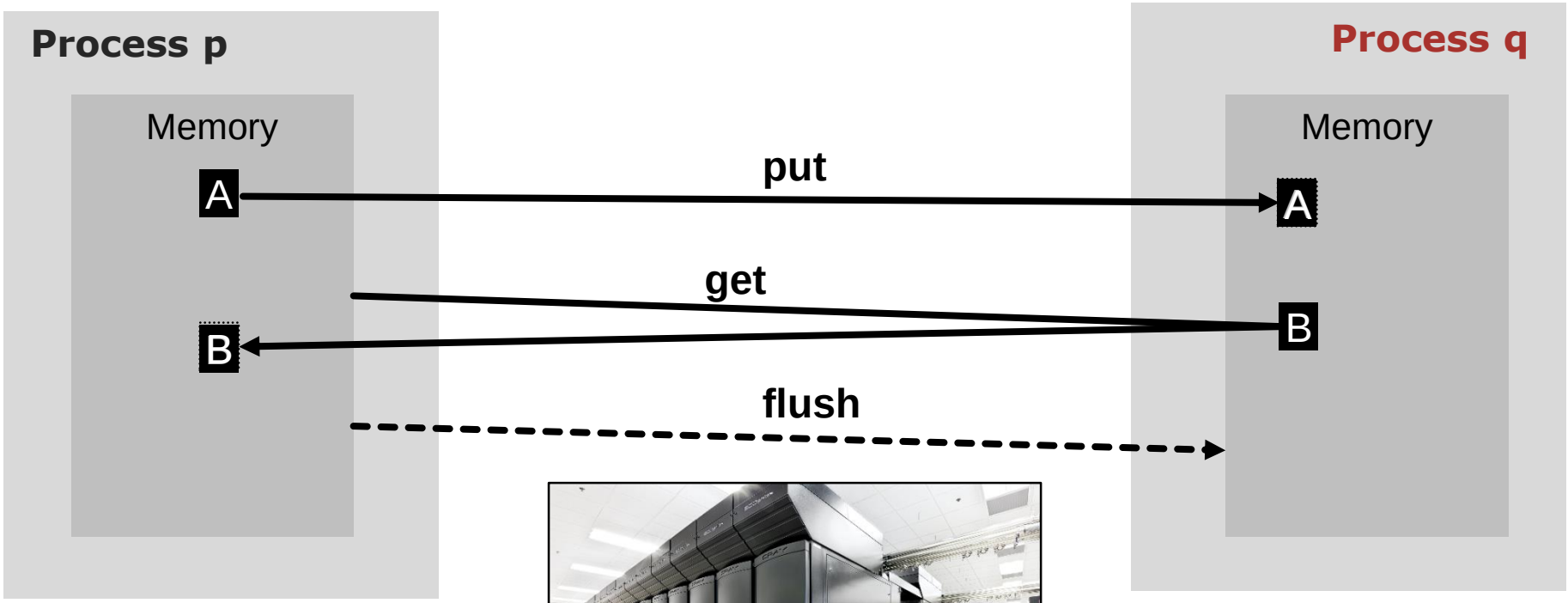
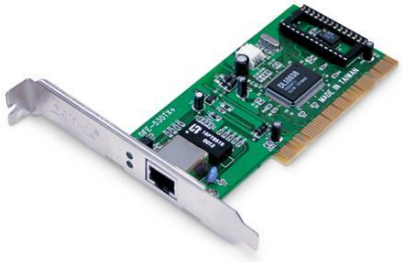


Cray BlueWaters

Remote Memory Access Programming

- Implemented in hardware in NICs in the majority of HPC networks (RDMA support).



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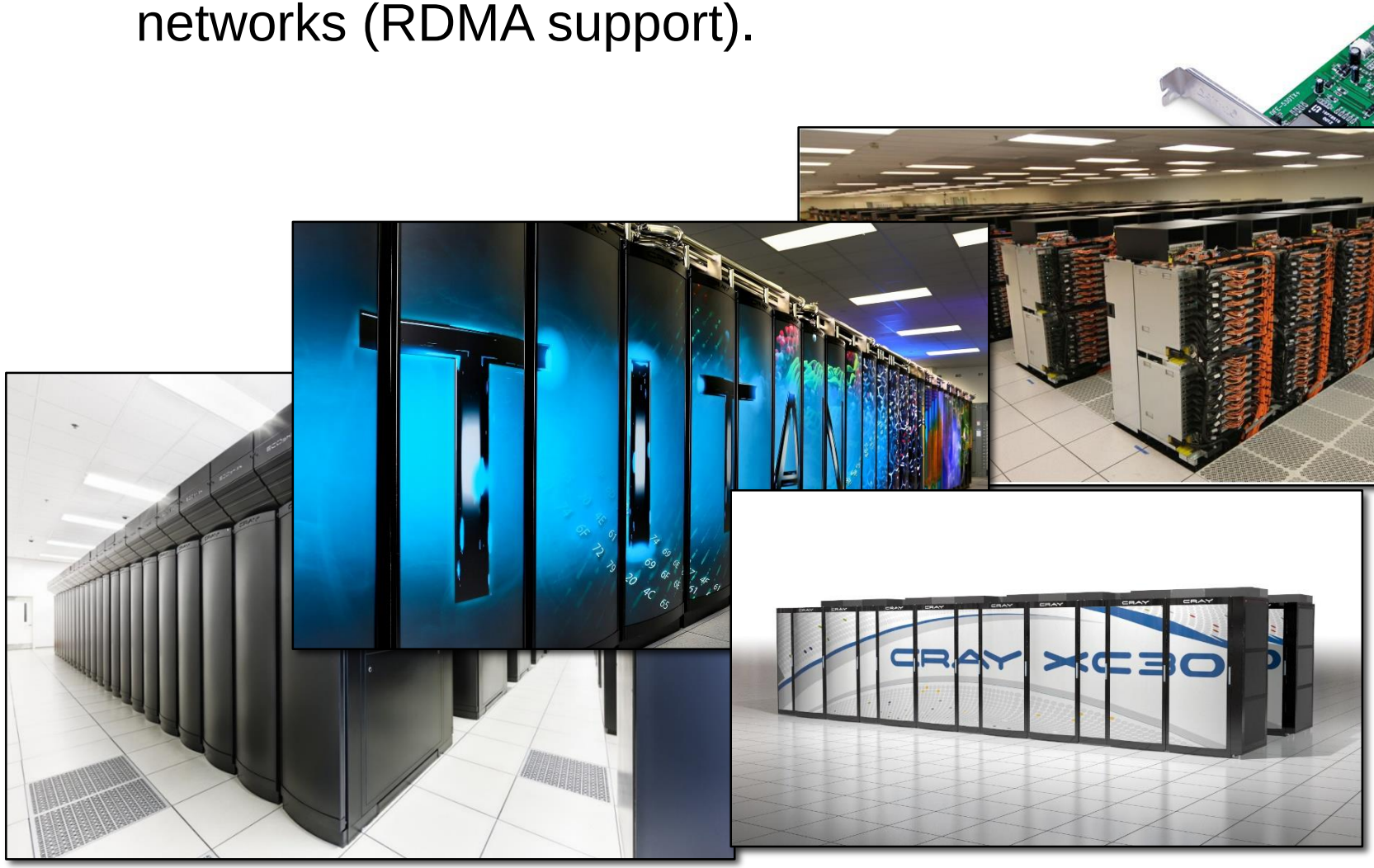

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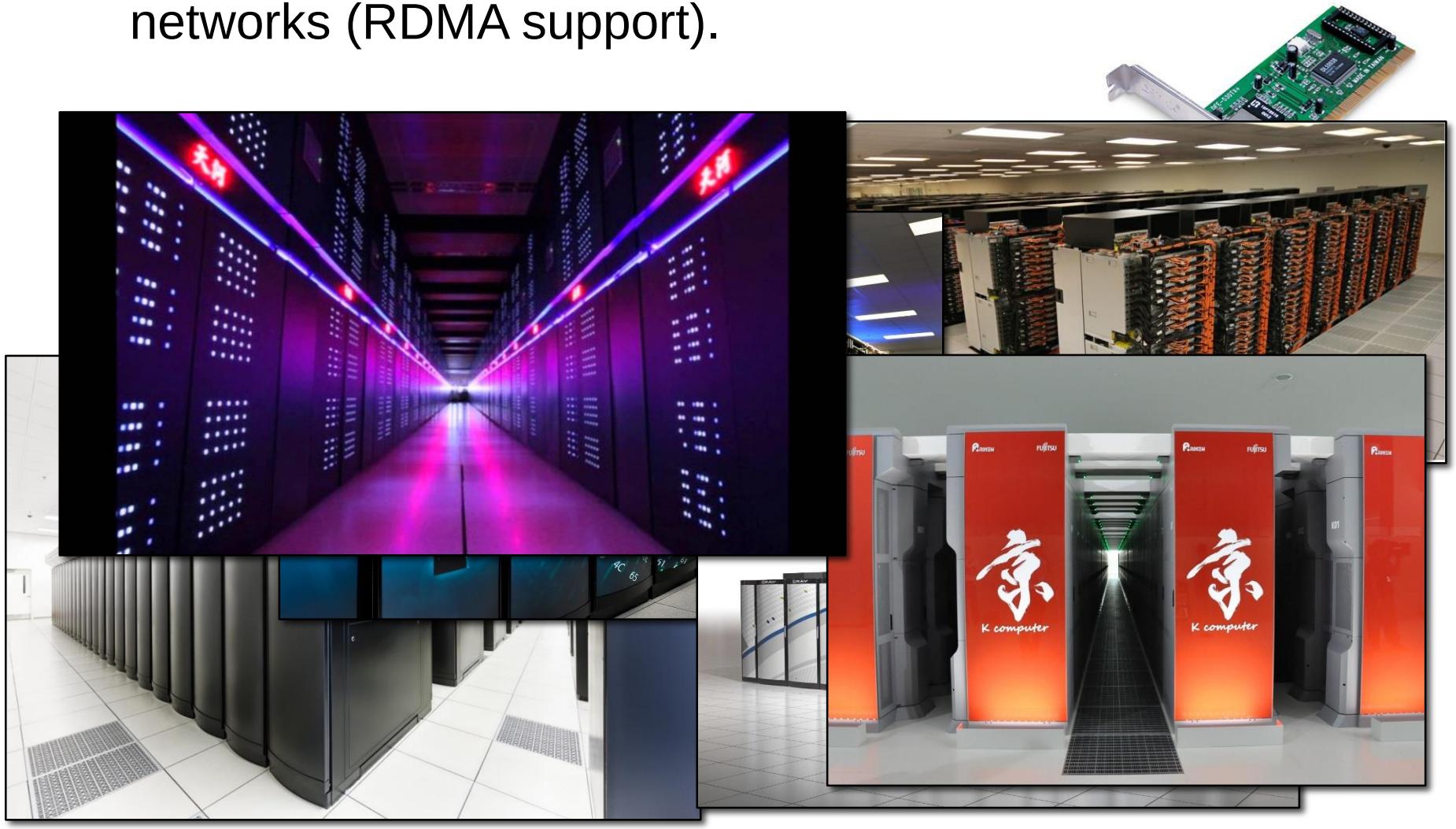

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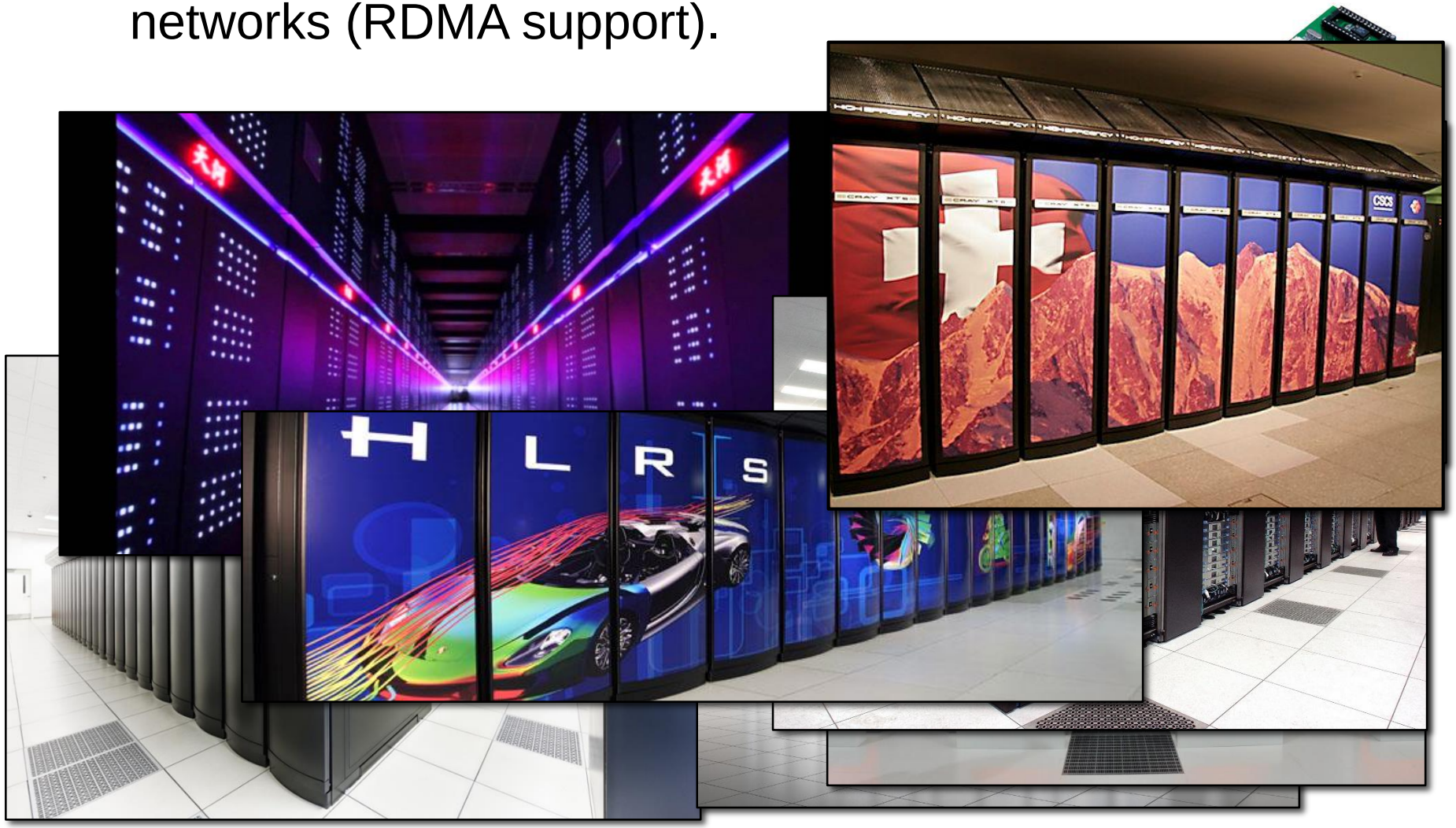

Remote Memory Access Programming

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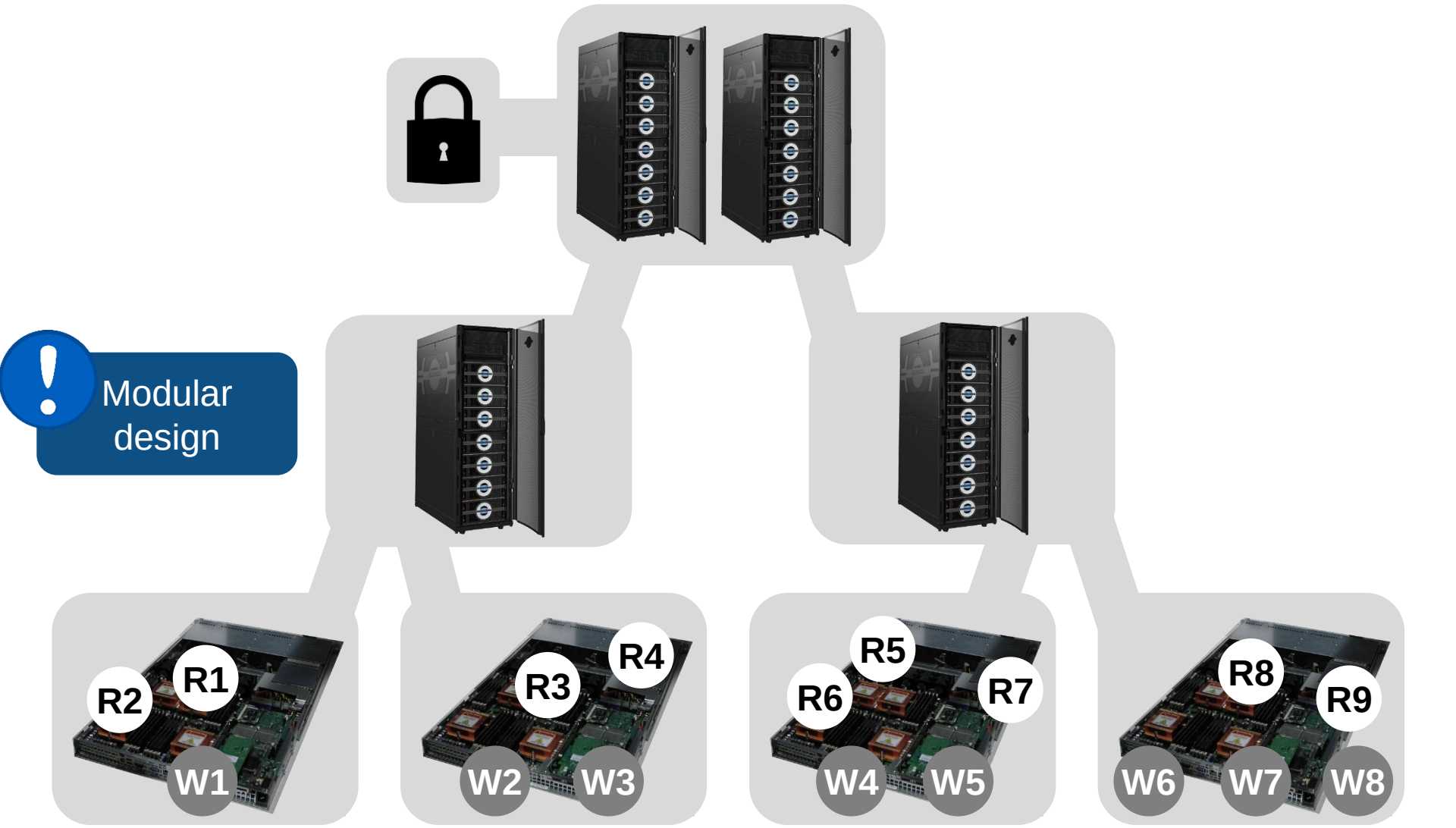
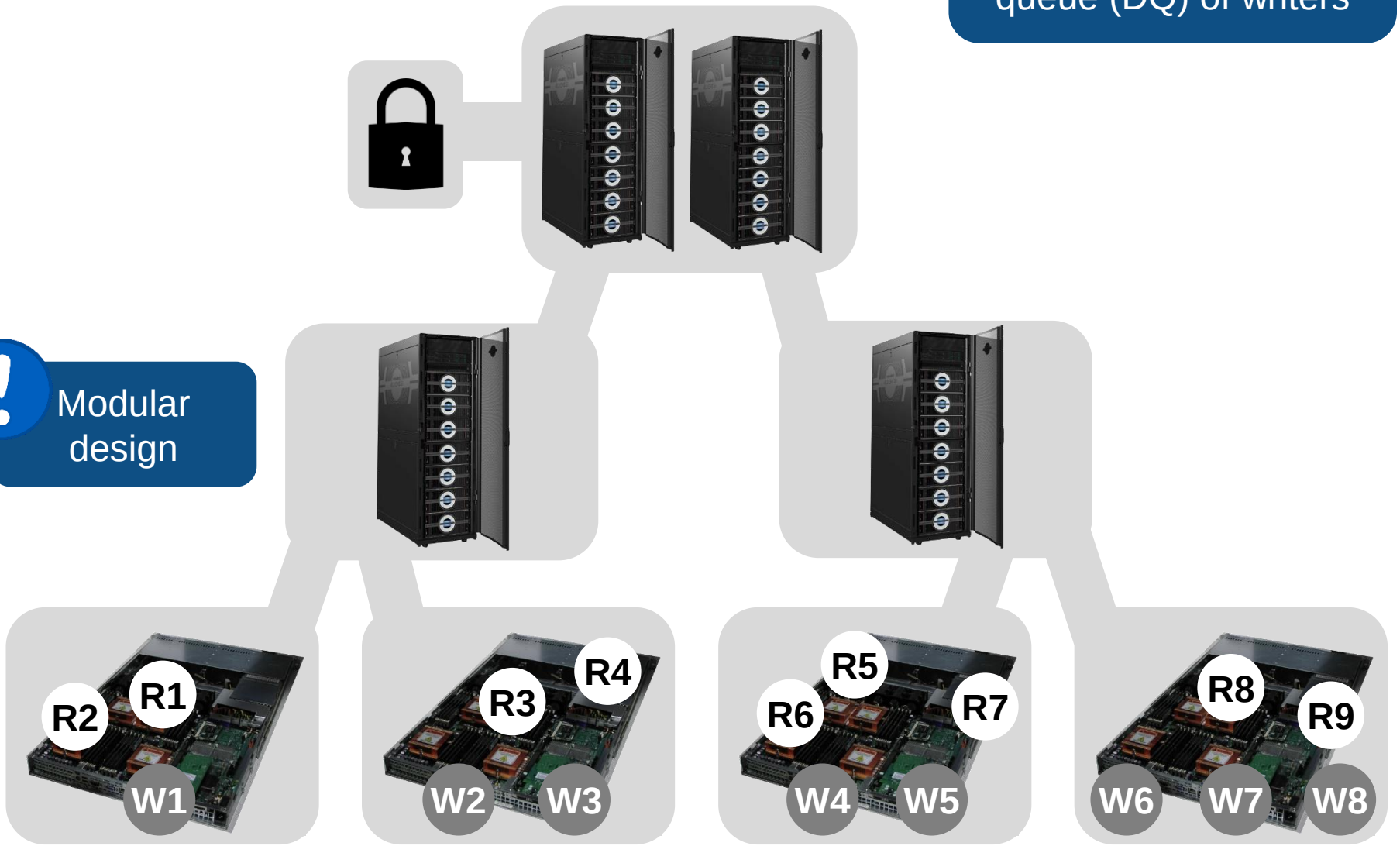


How to manage the design complexity?

Each element has its own distributed MCS queue (DQ) of writers

Modular design



How to manage the design complexity?

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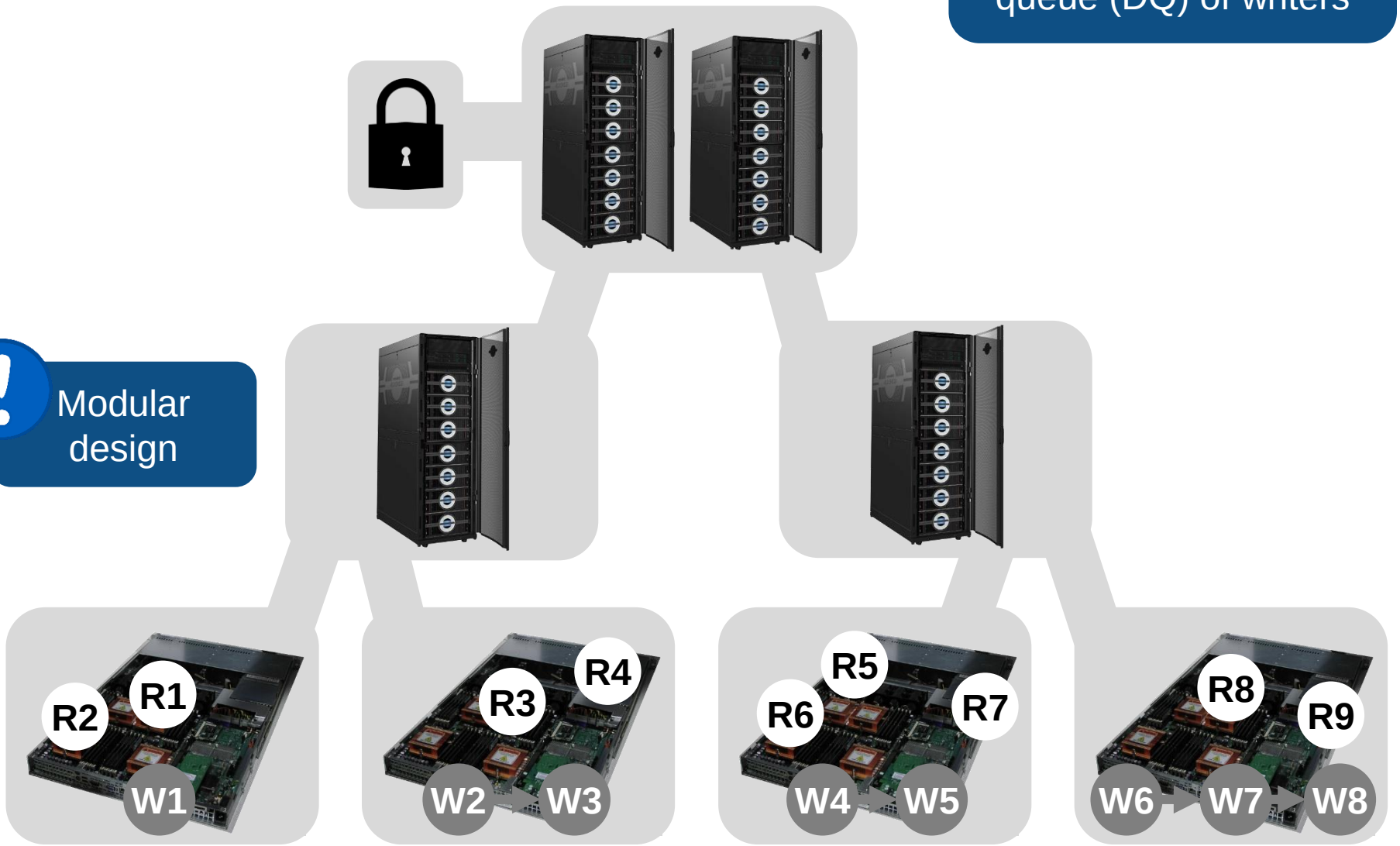

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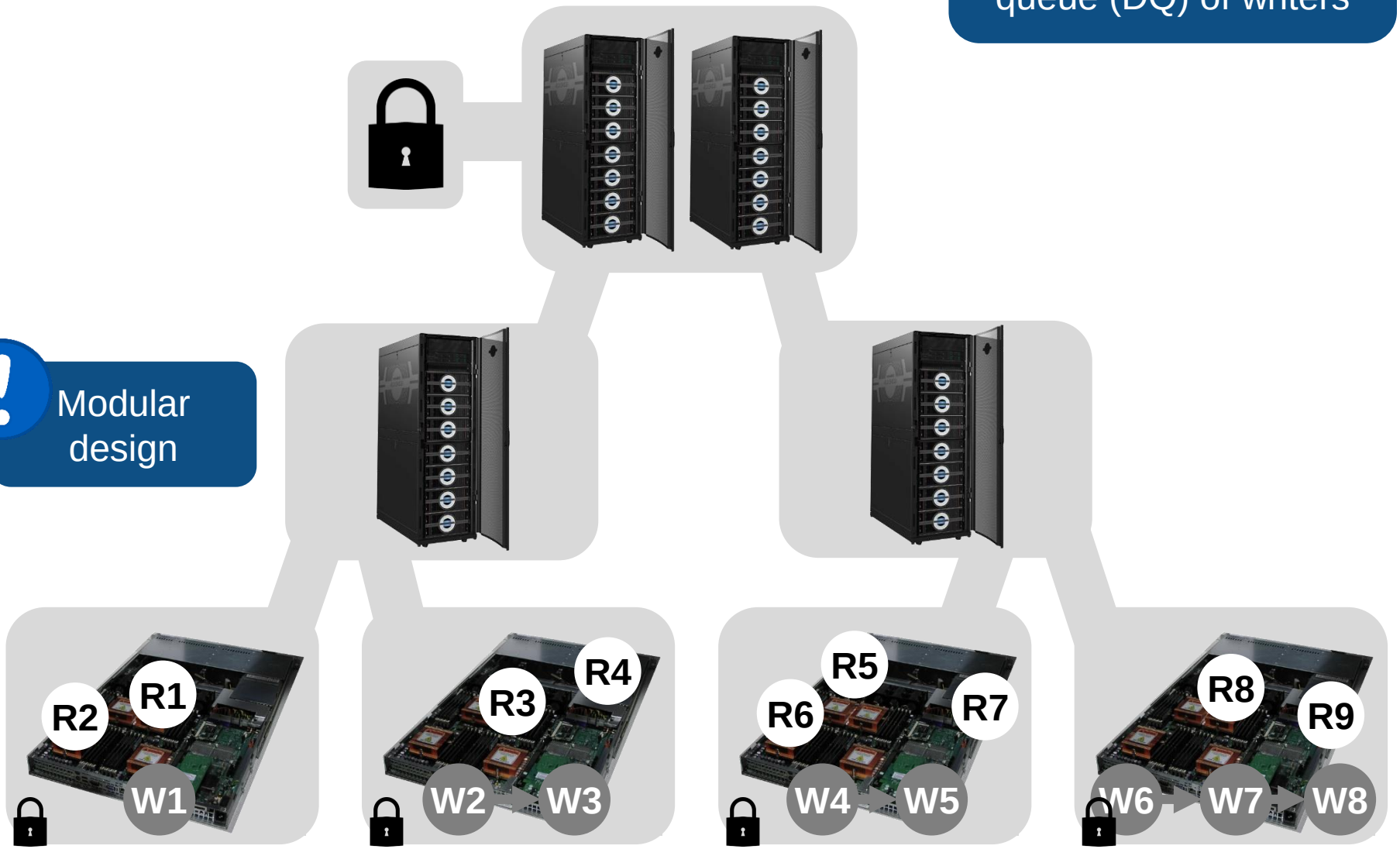

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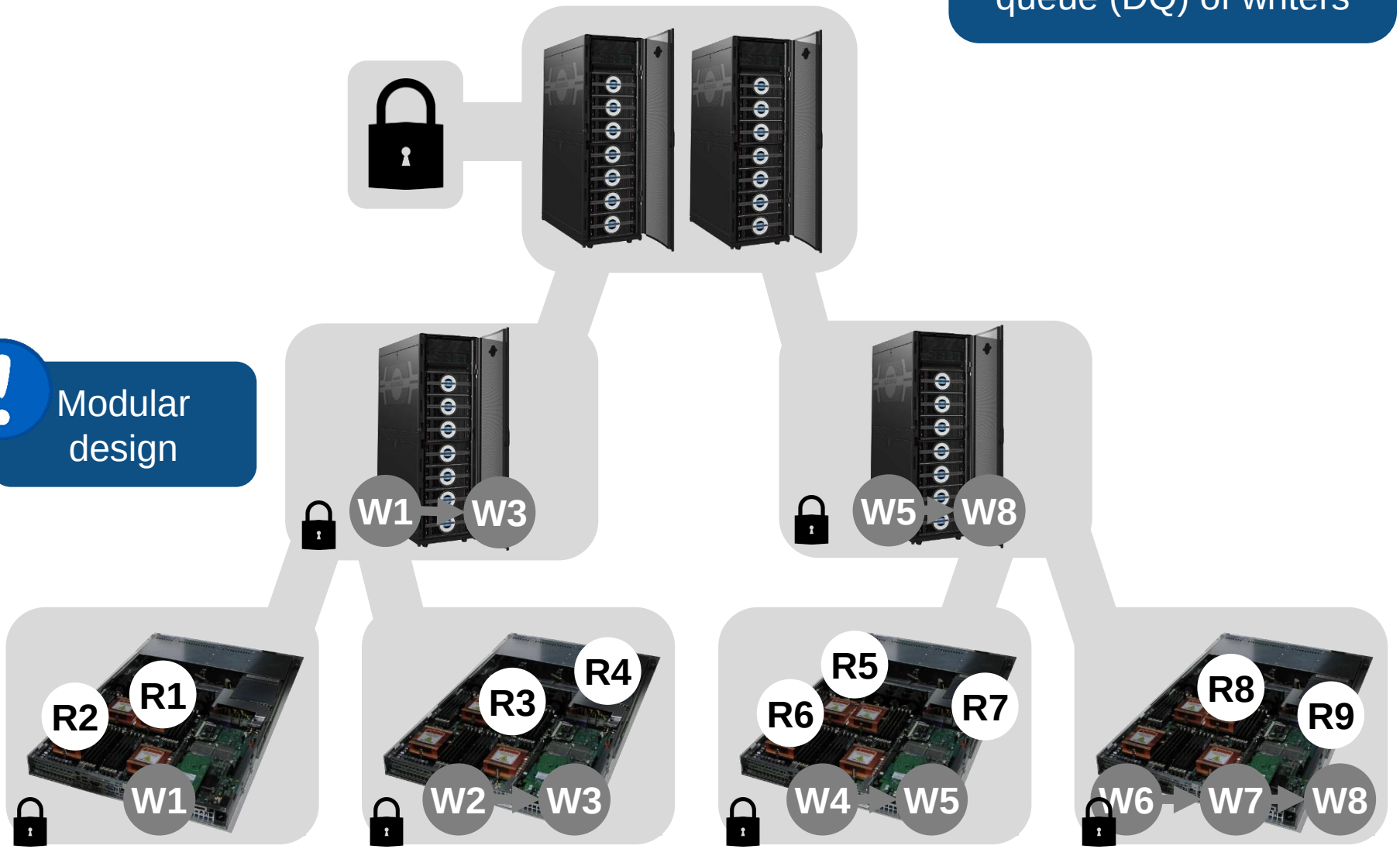

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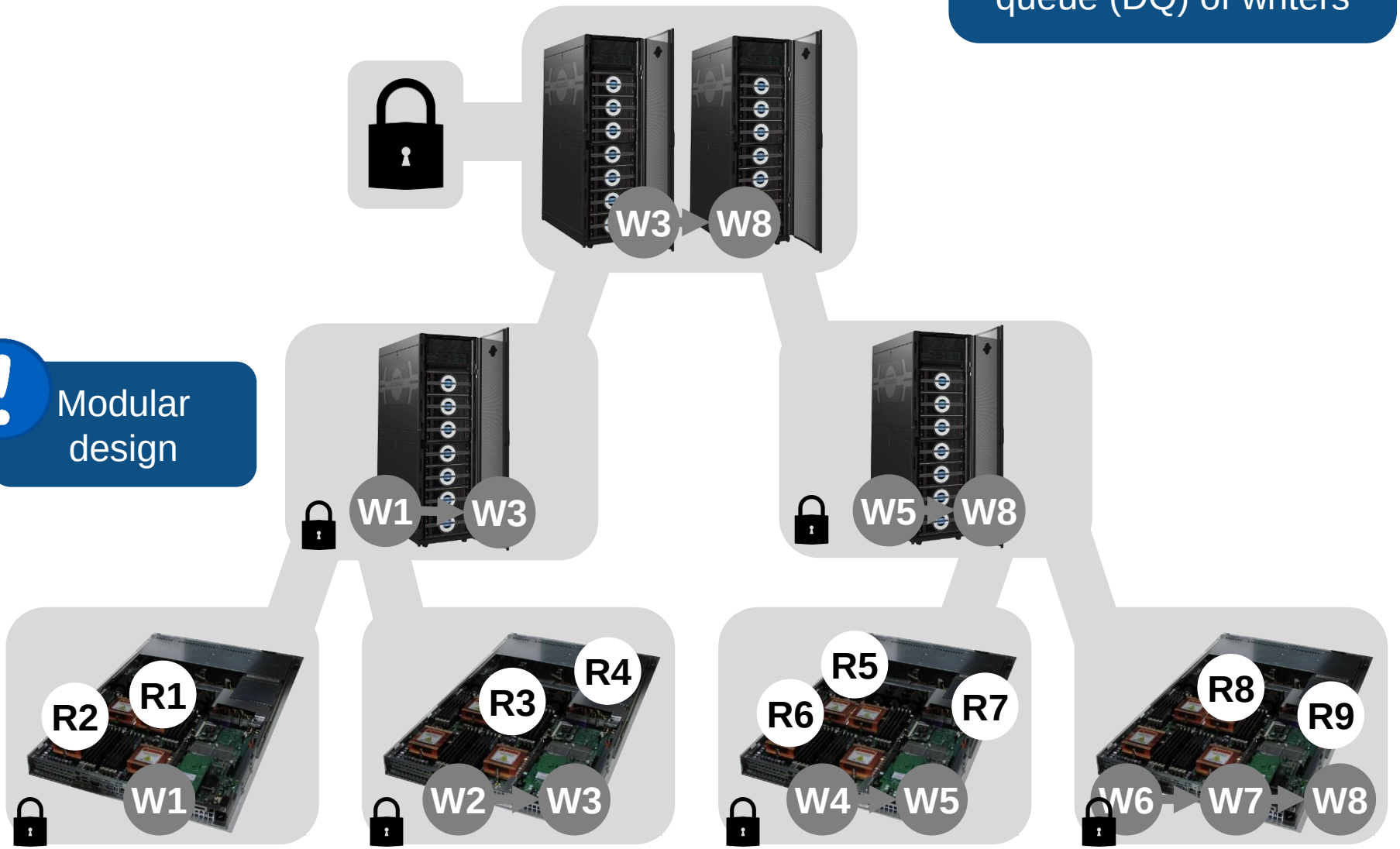

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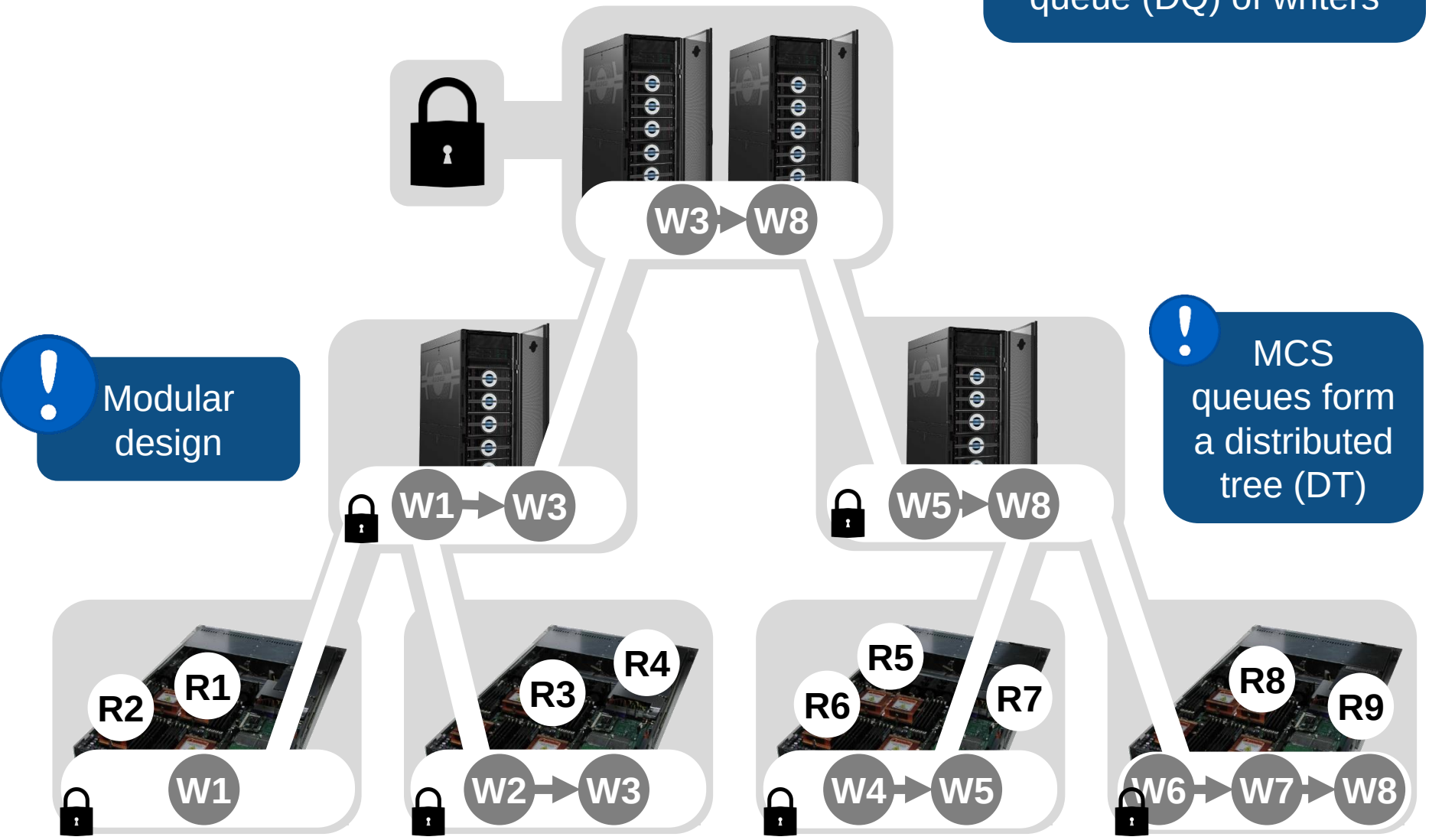
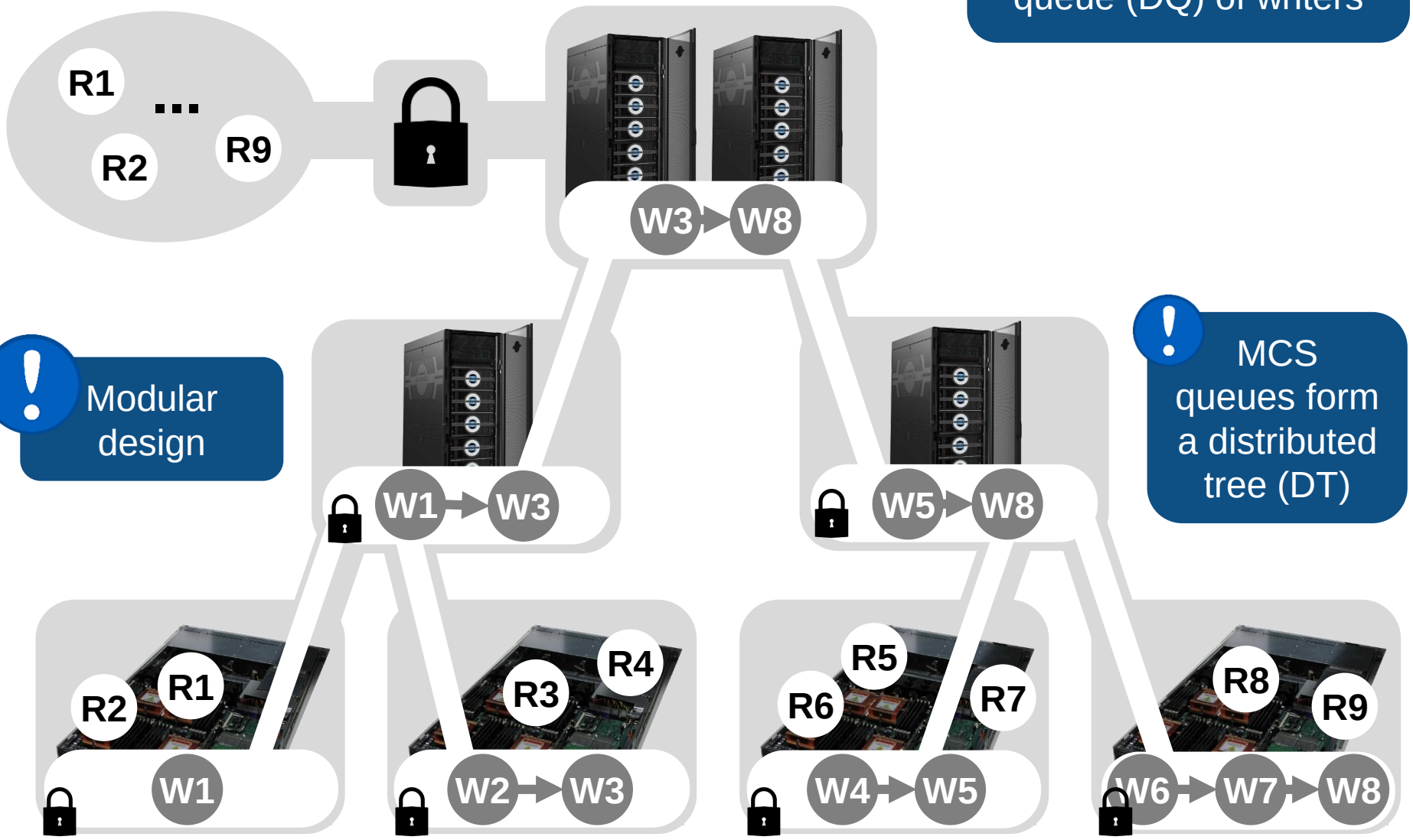


Modular design

MCS queues form a distributed tree (DT)

How to manage the design complexity?

Each element has its own distributed MCS queue (DQ) of writers



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Readers and writers synchronize with a distributed counter (DC)

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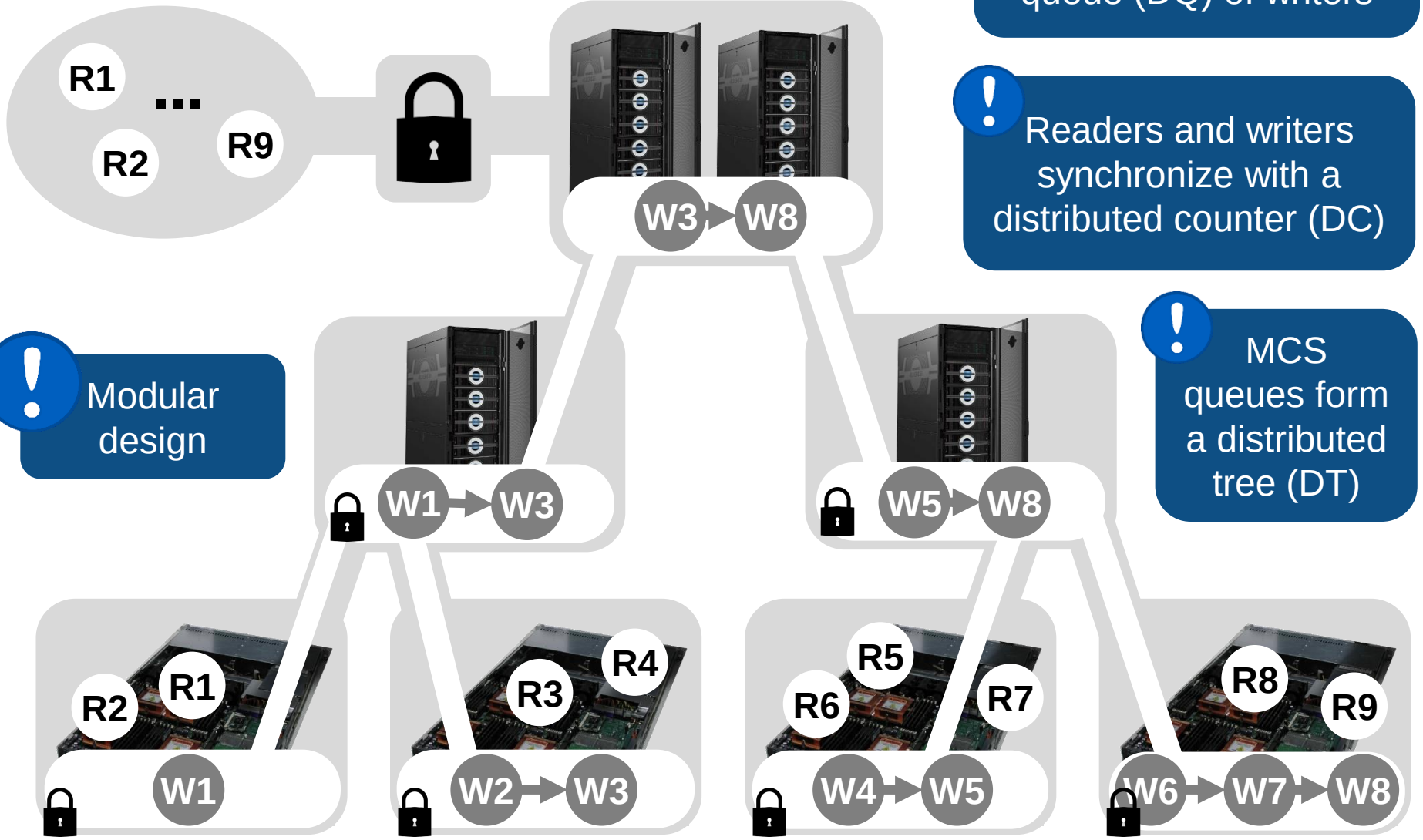
Modular design



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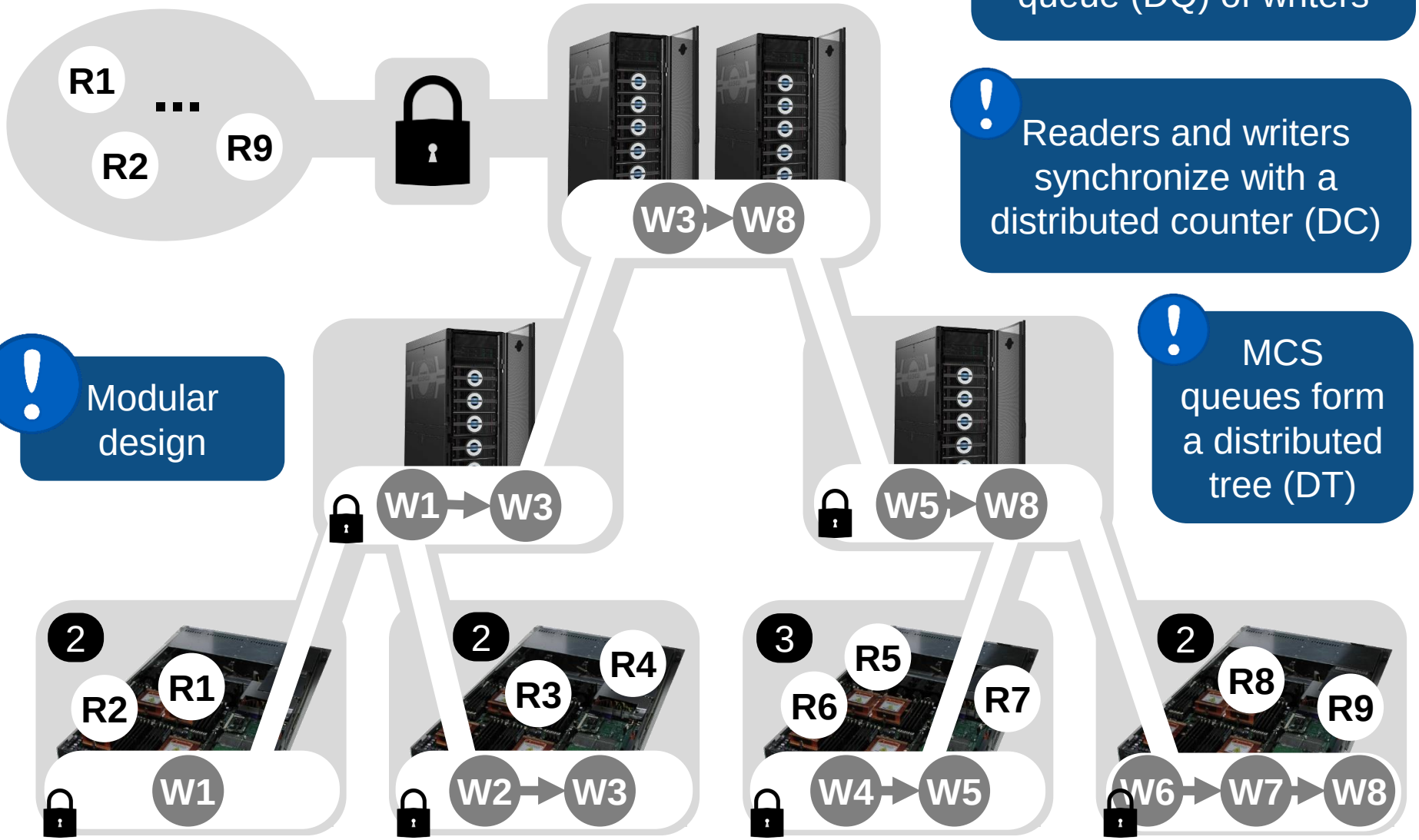
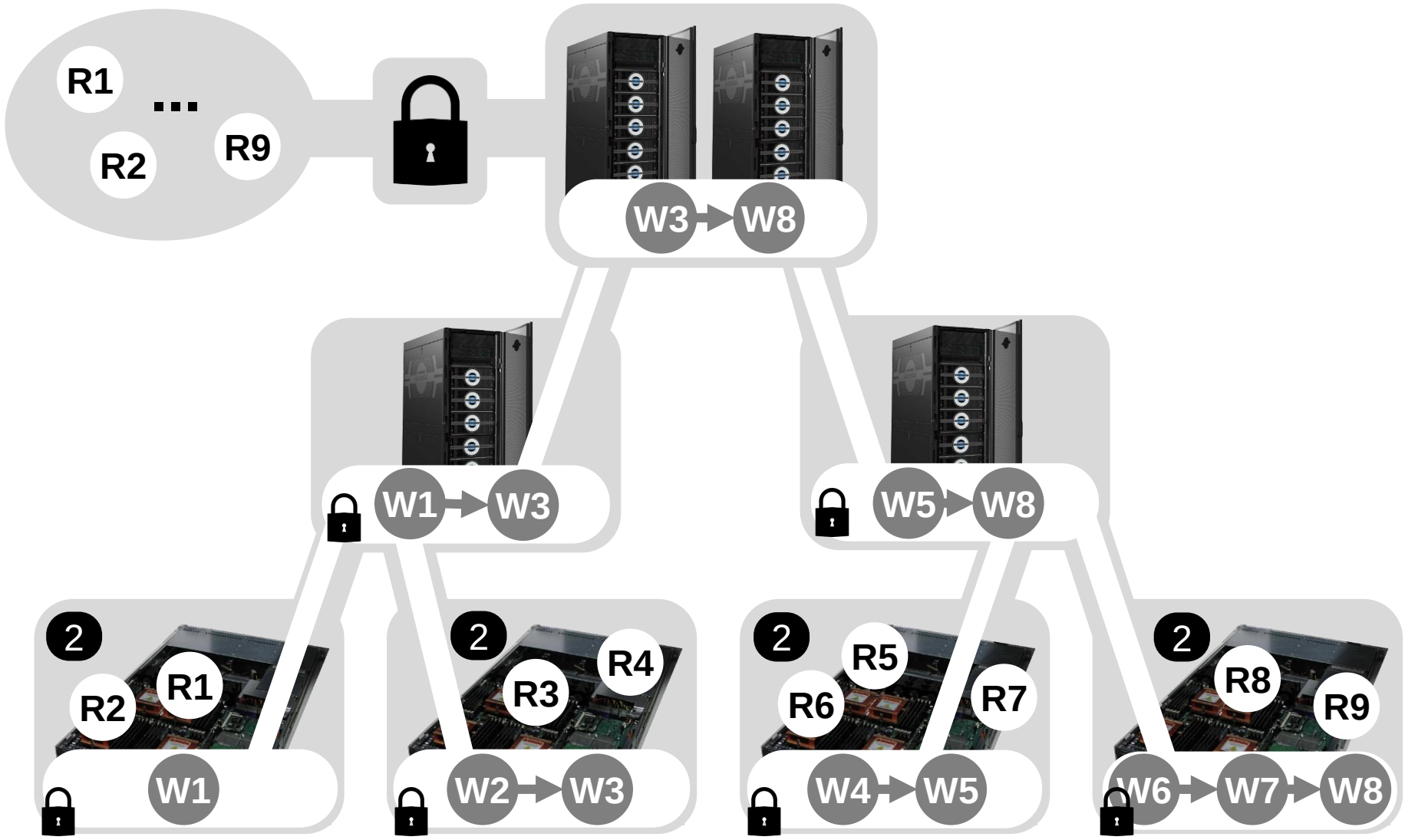


How to ensure tunable performance?



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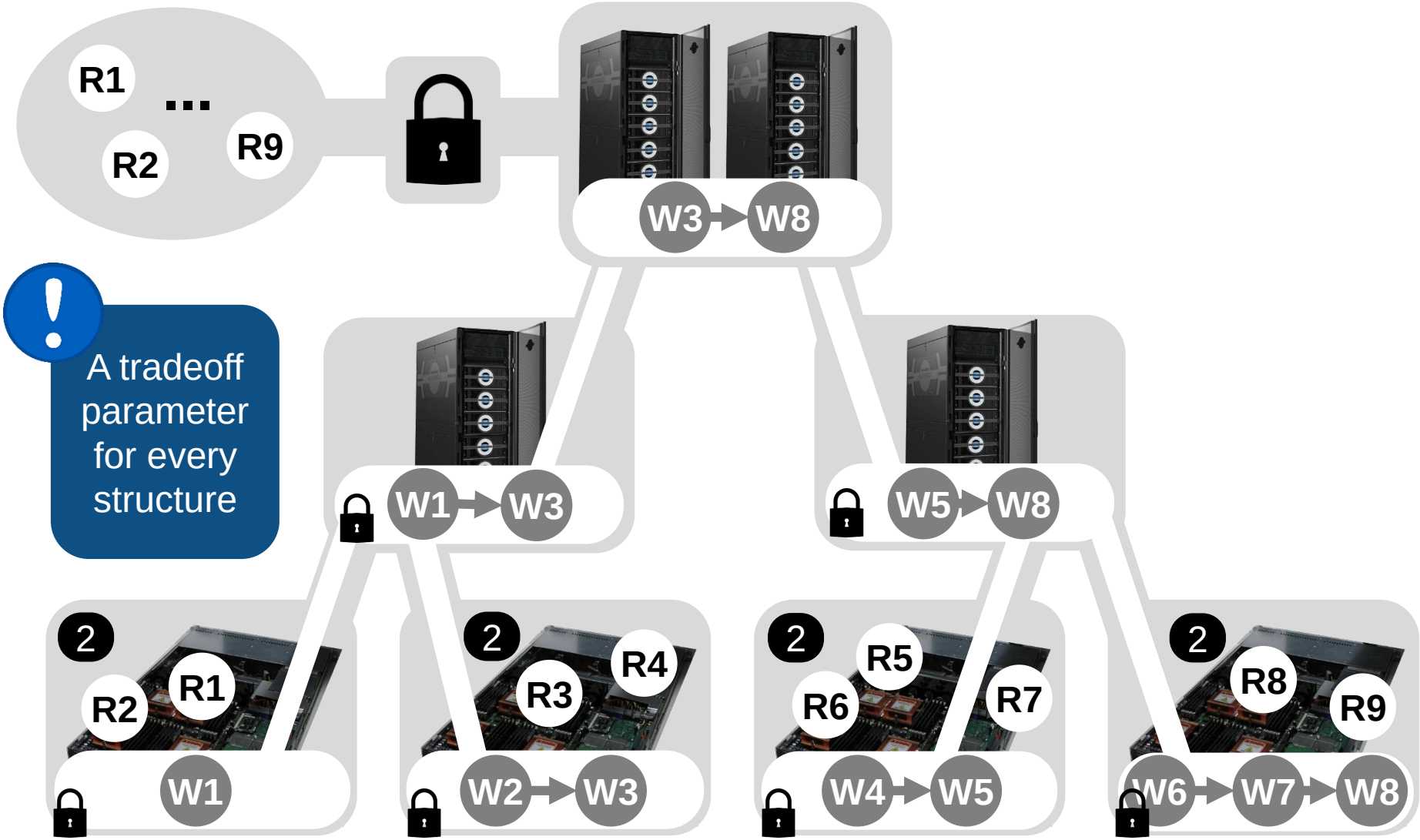

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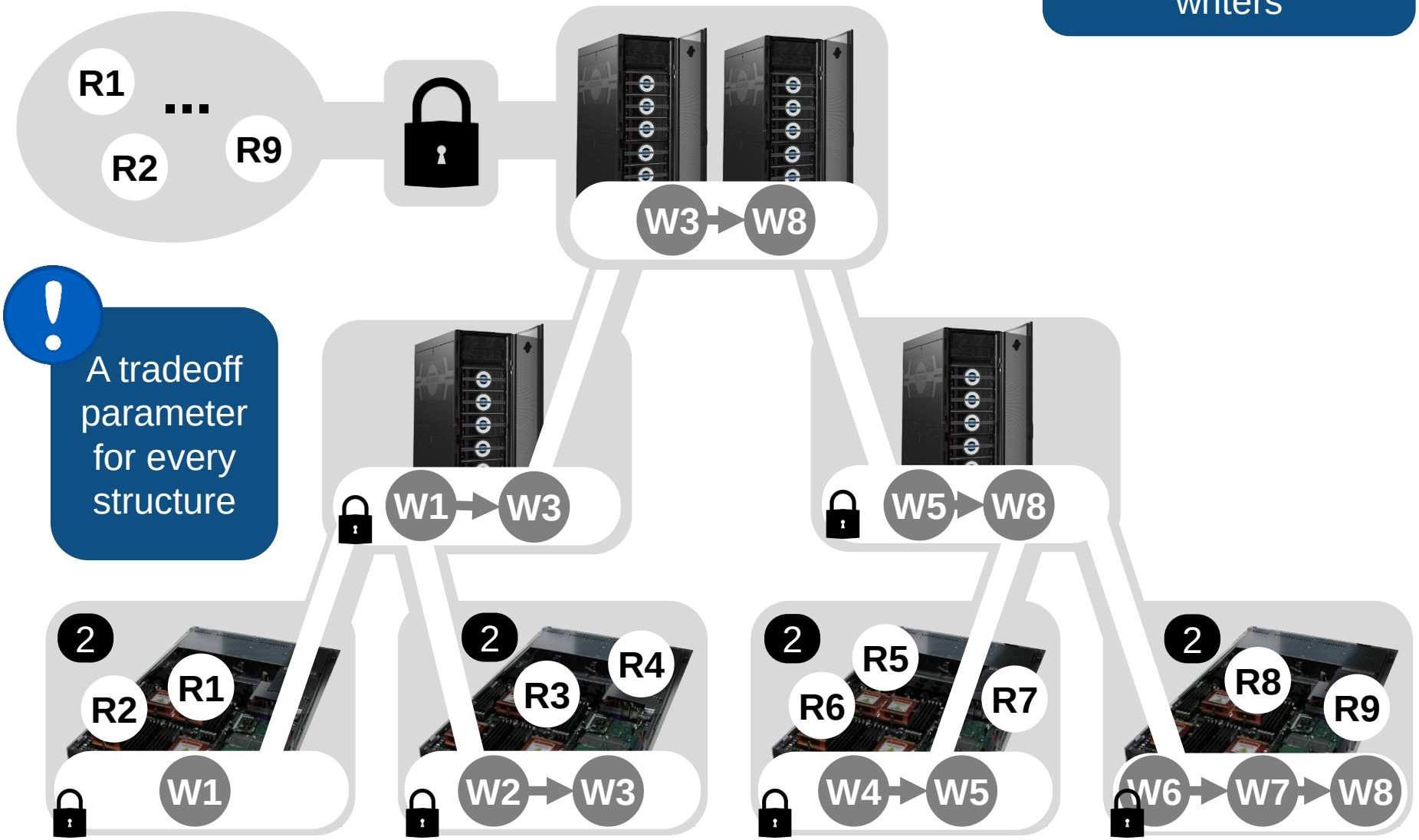
Each DQ: fairness vs throughput of writers

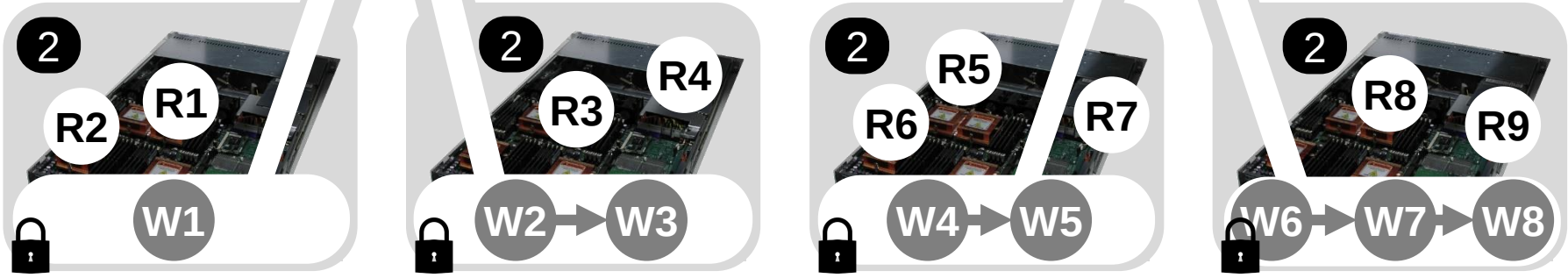


How to ensure tunable performance?

Each DQ: fairness vs throughput of writers

A tradeoff parameter for every structure

DT: a parameter for the throughput of readers vs writers



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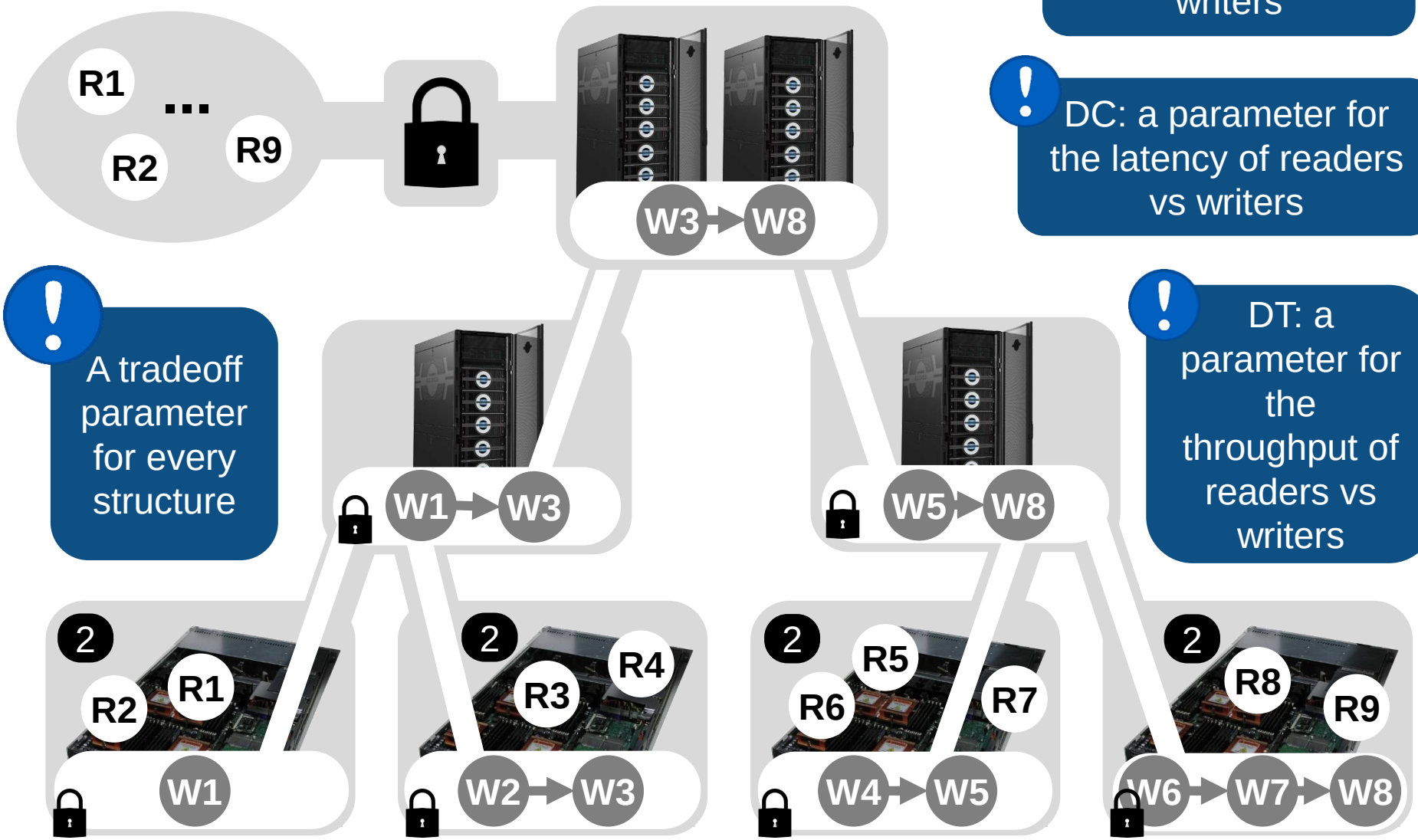

DISTRIBUTED MCS QUEUES (DQS)

Throughput vs Fairness

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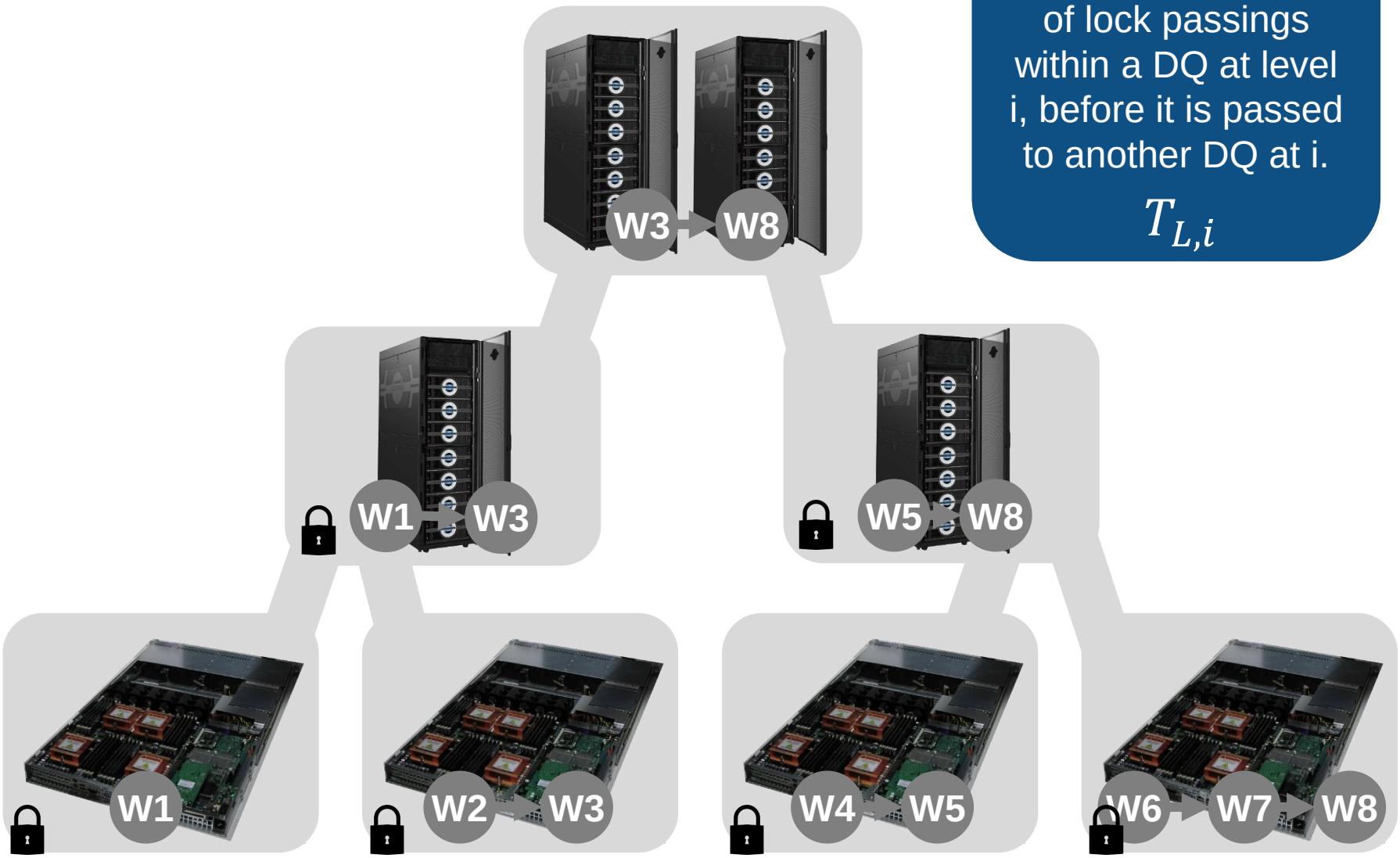
Each DQ: The maximum number of lock passings within a DQ at level i, before it is passed to another DQ at i.

$T_{L,i}$



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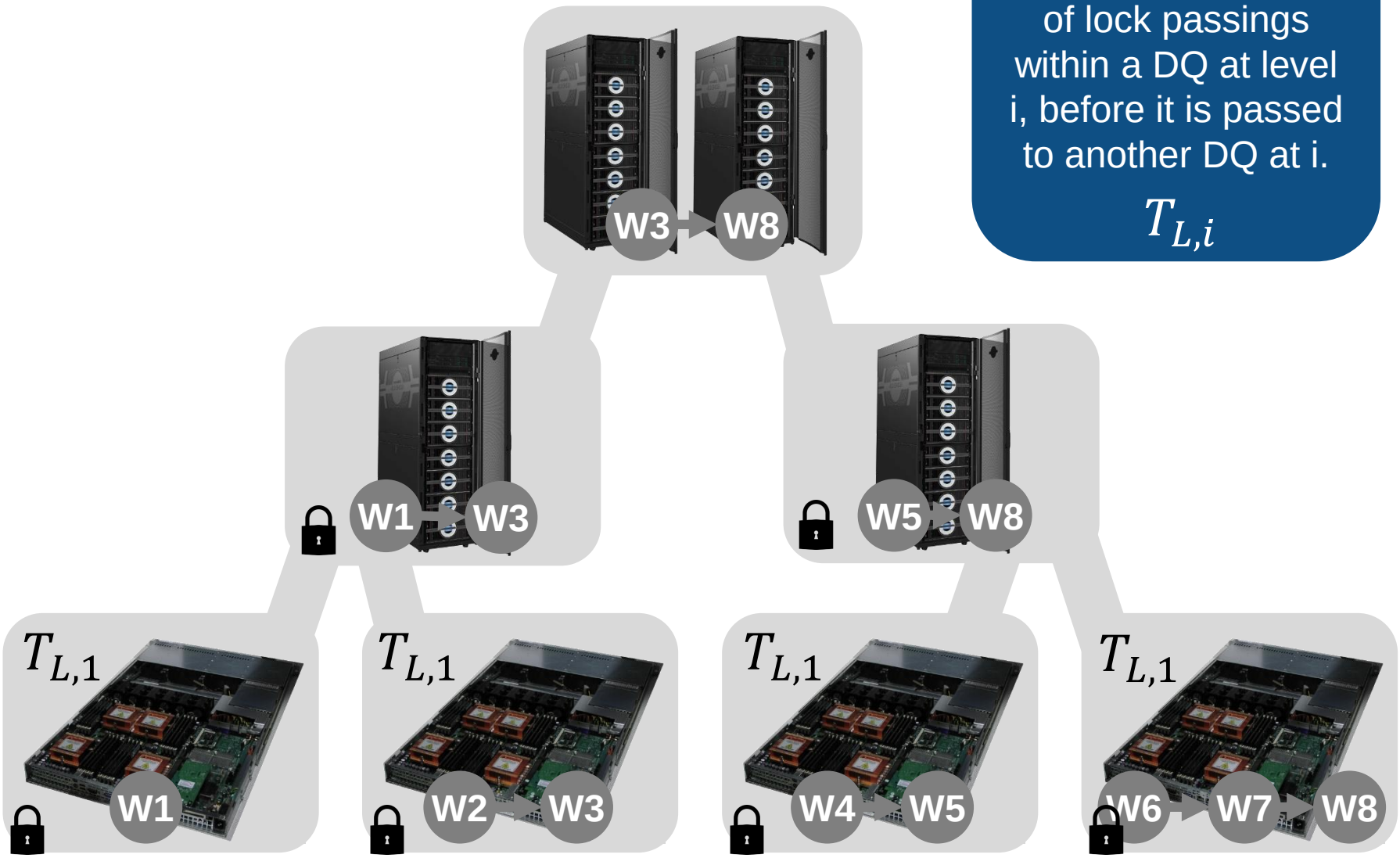

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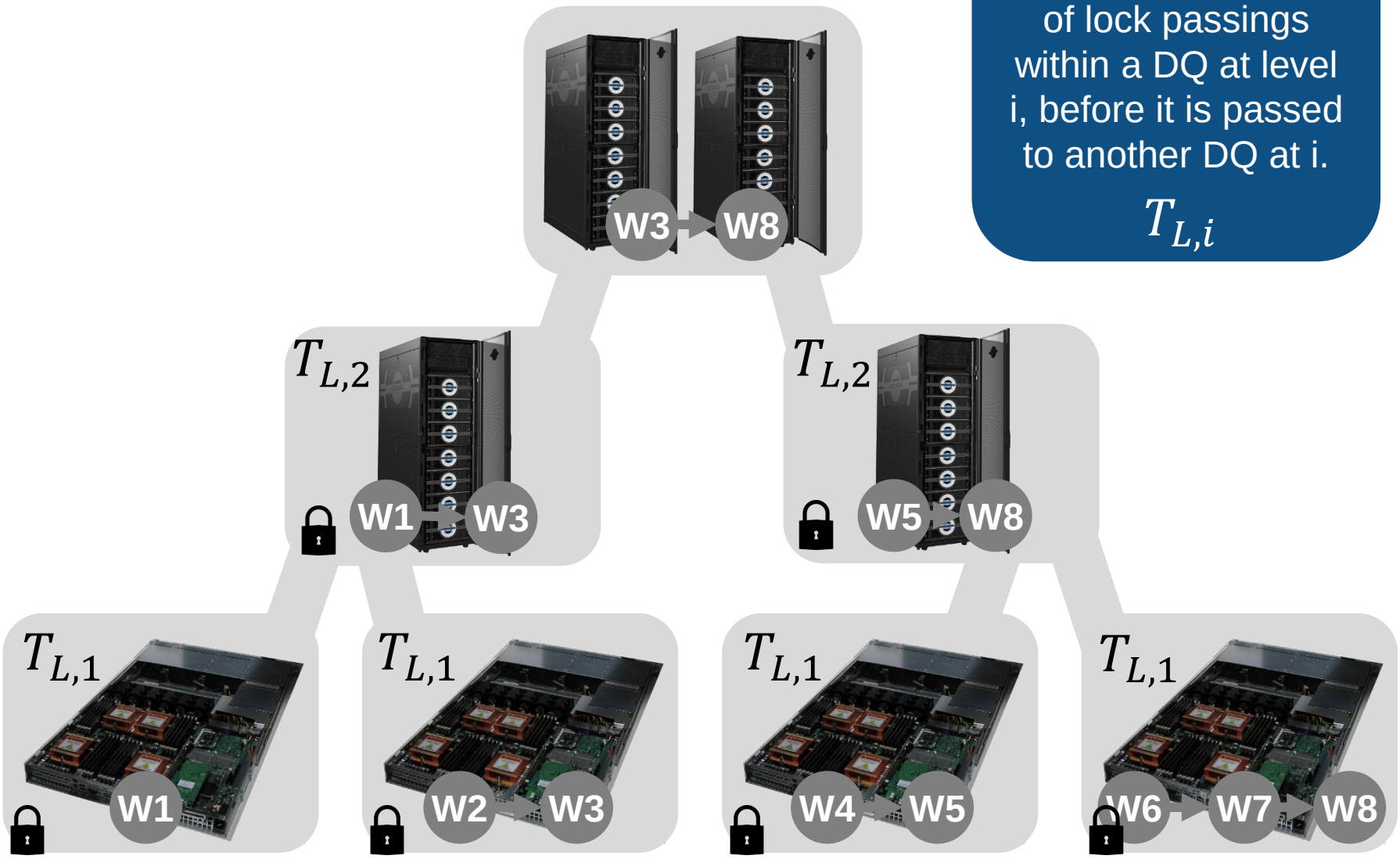

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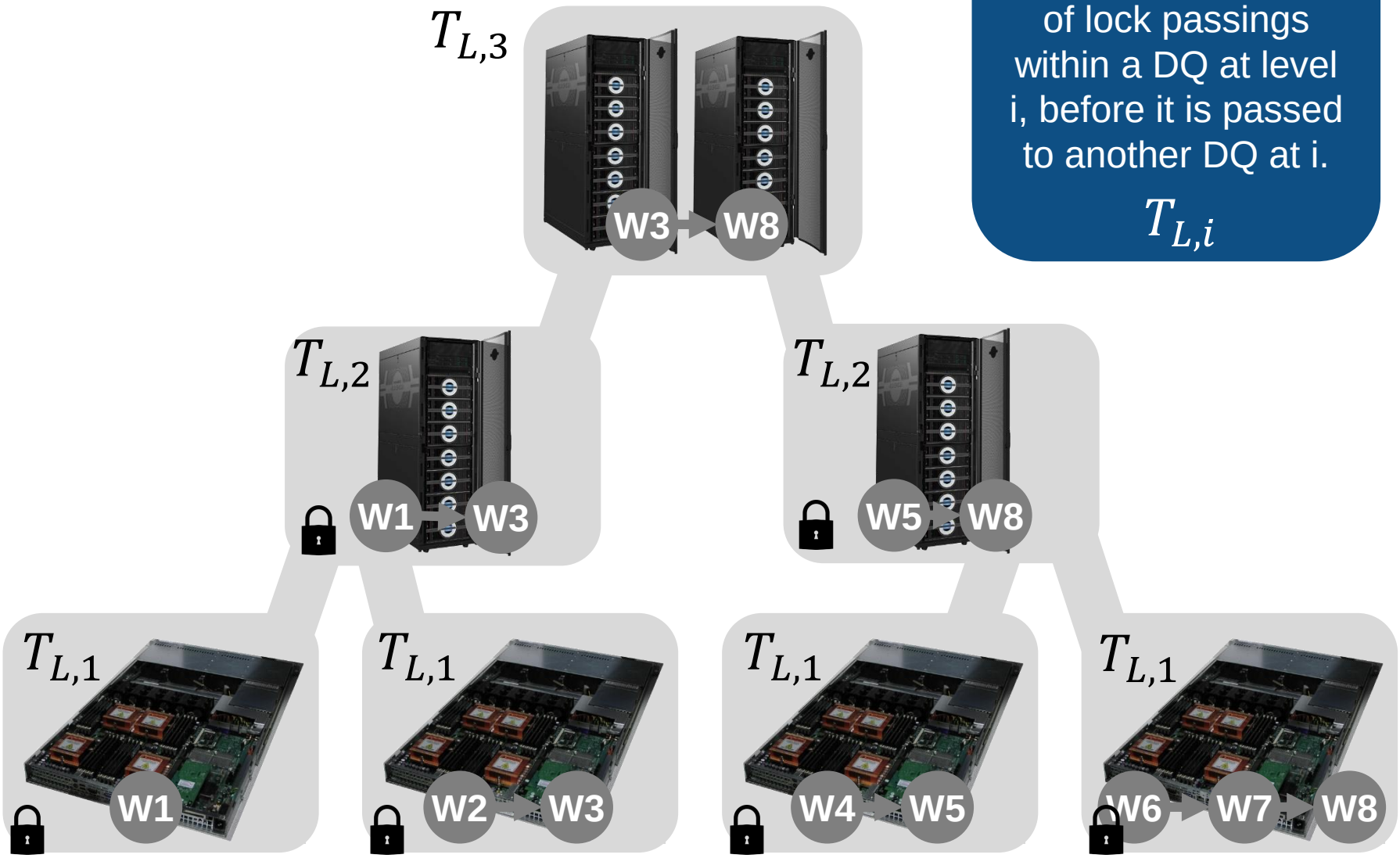

Distributed MCS Queues (DQs)

Throughput vs Fairness

Larger $T_{L,i}$: more throughput at level i.
Smaller $T_{L,i}$: more fairness at level i.

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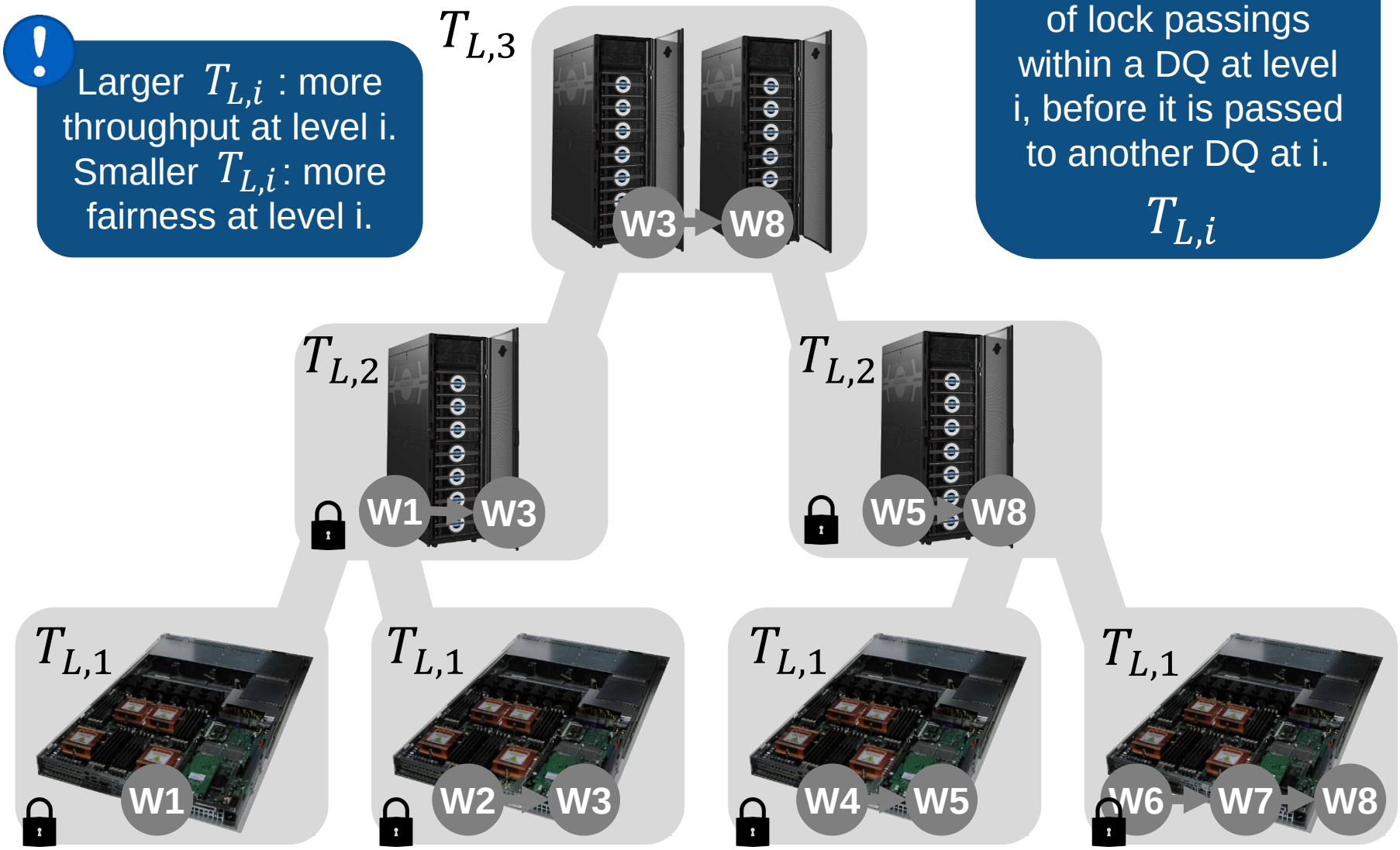
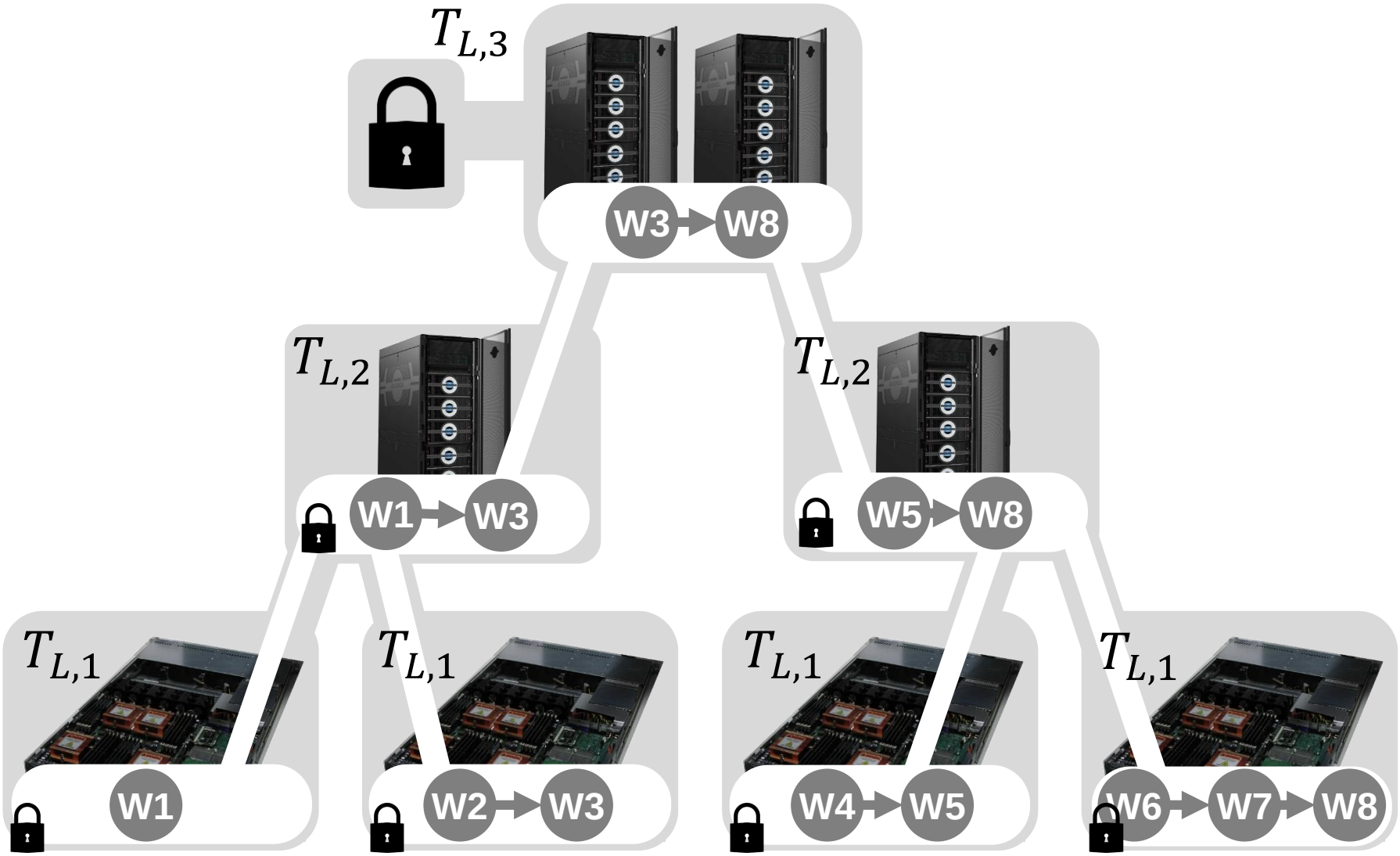
$T_{L,i}$



Distributed Tree of Queues (DT)

Throughput of readers vs writers



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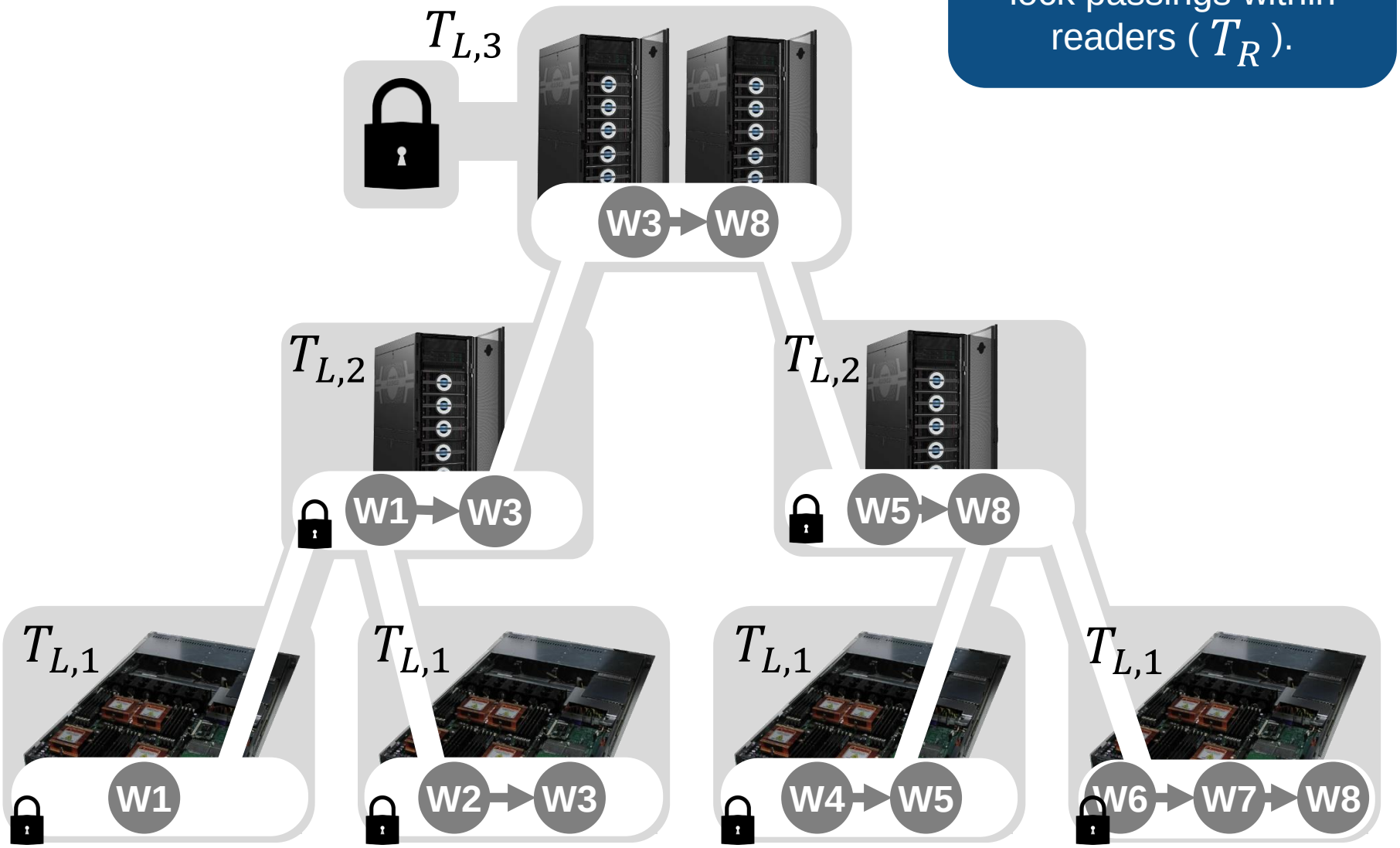
DT: The maximum number of consecutive lock passings within readers (T_R).



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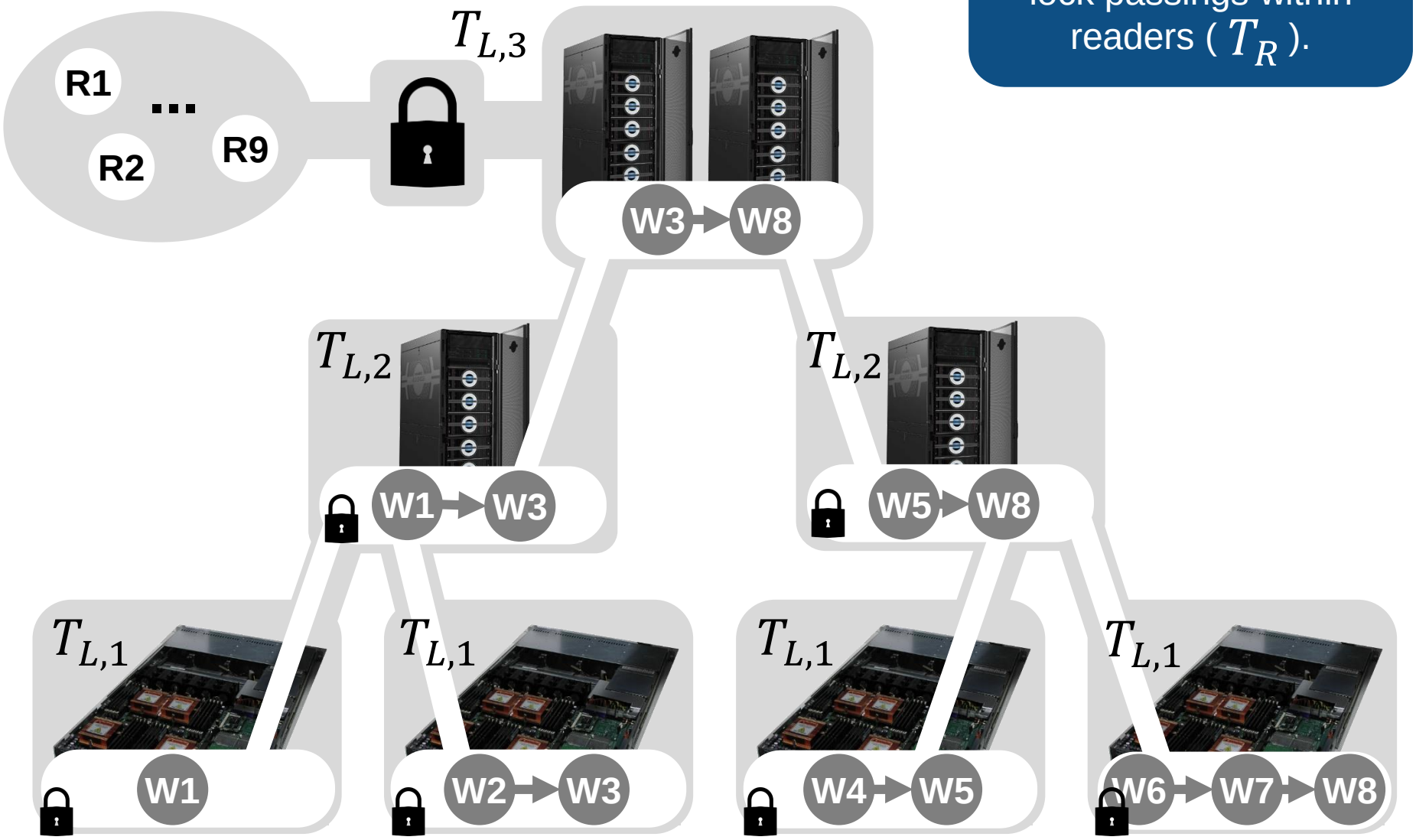

DISTRIBUTED COUNTER (DC)

Latency of readers vs writers

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$$k = T_{DC}$$

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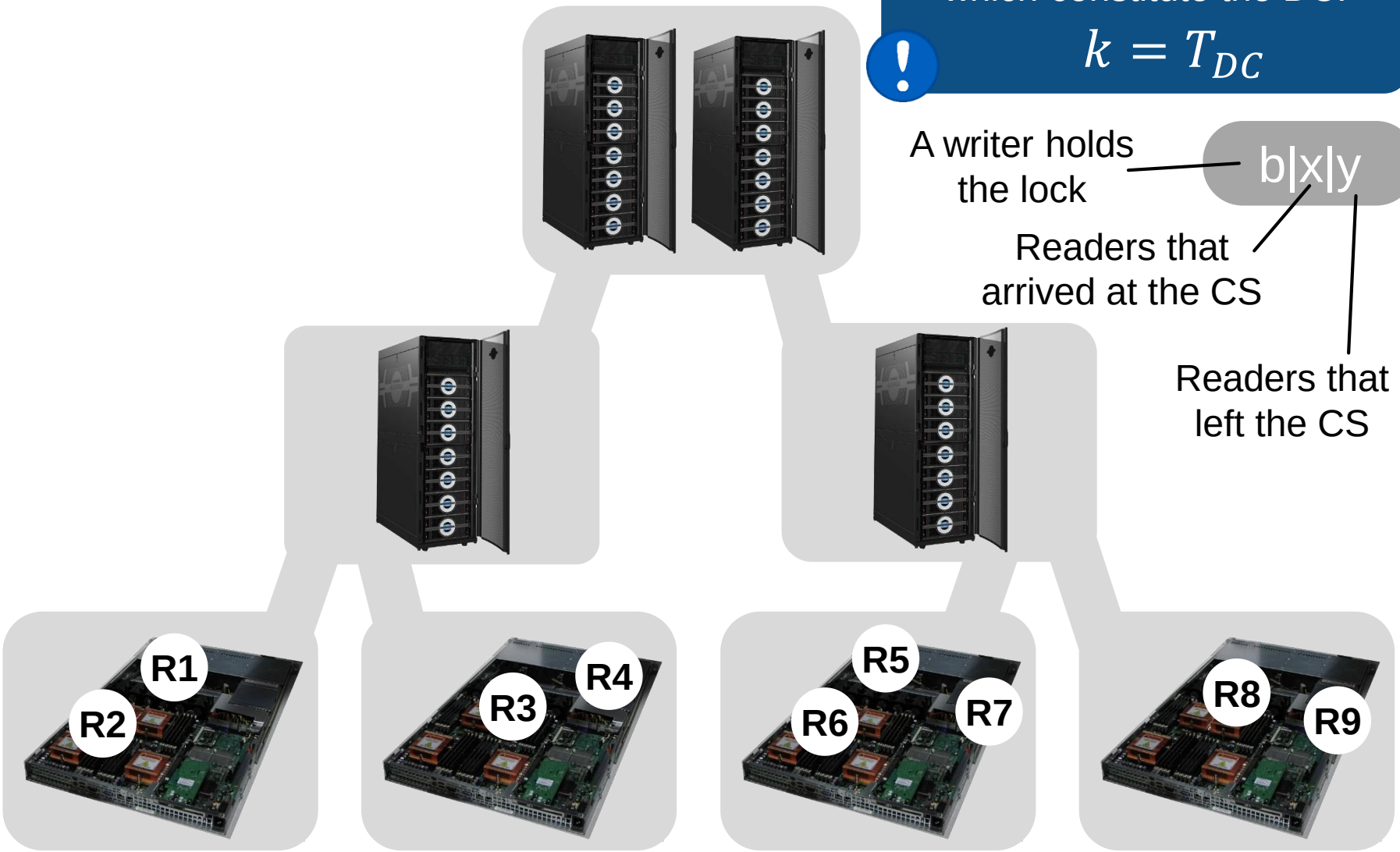

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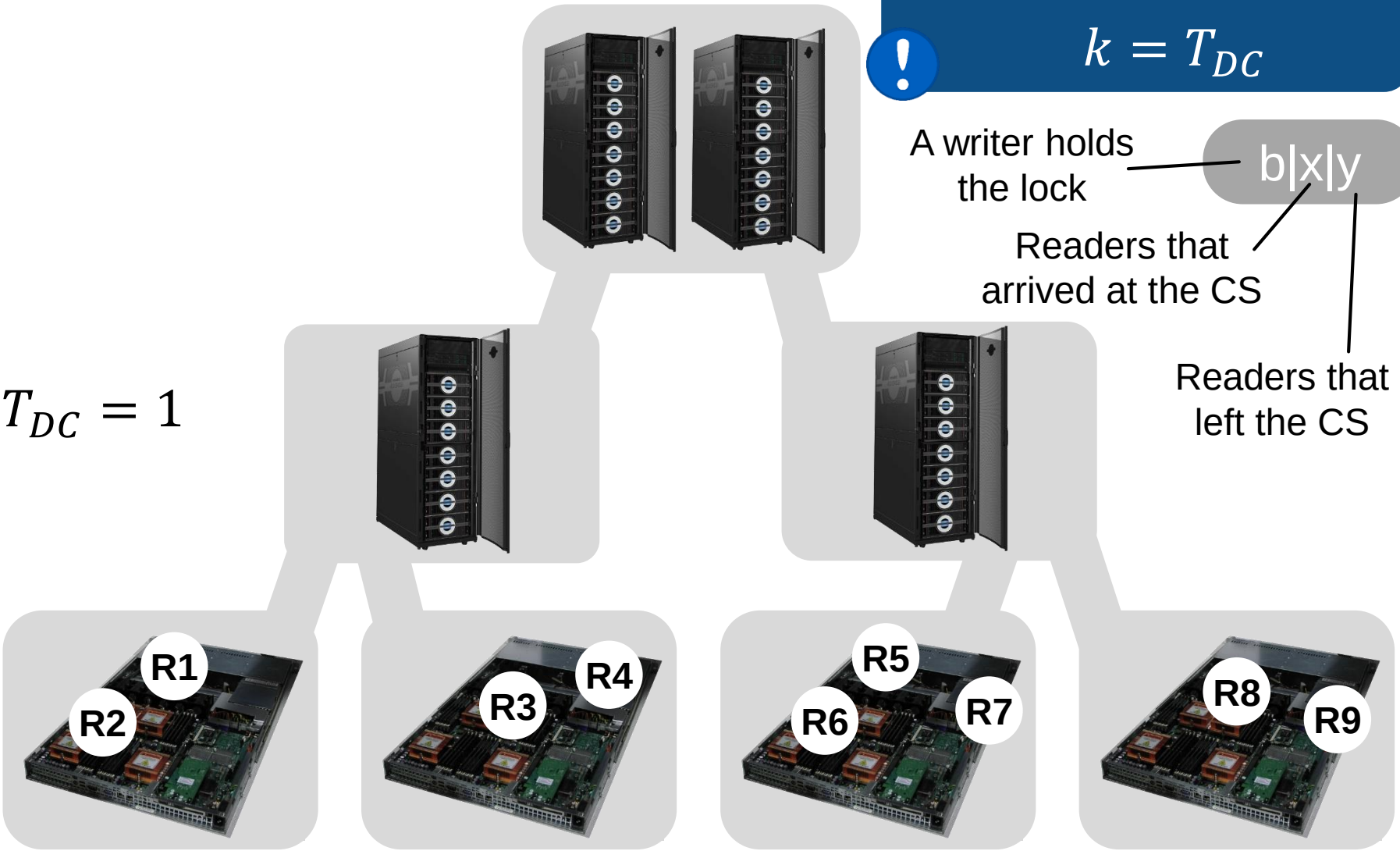

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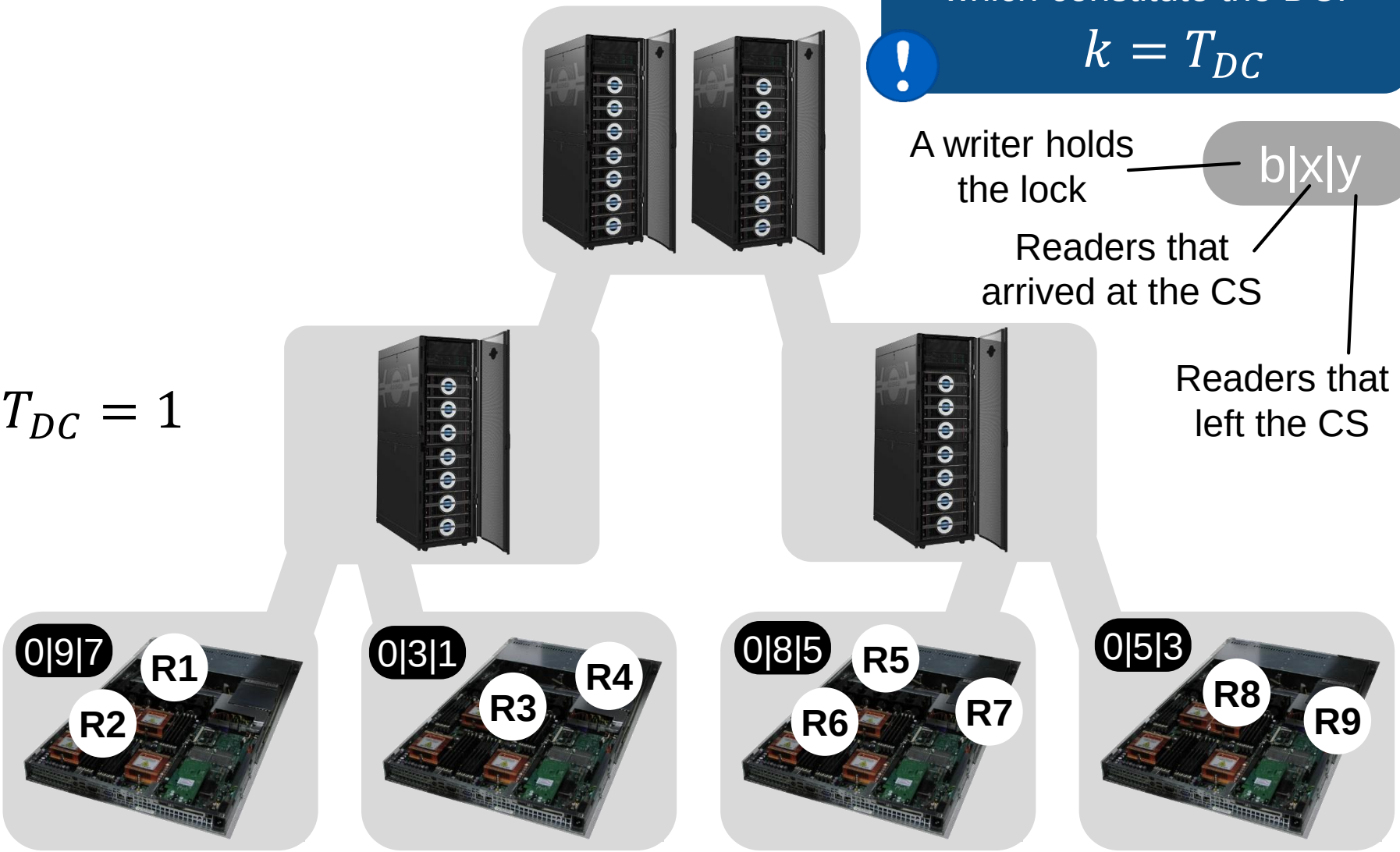

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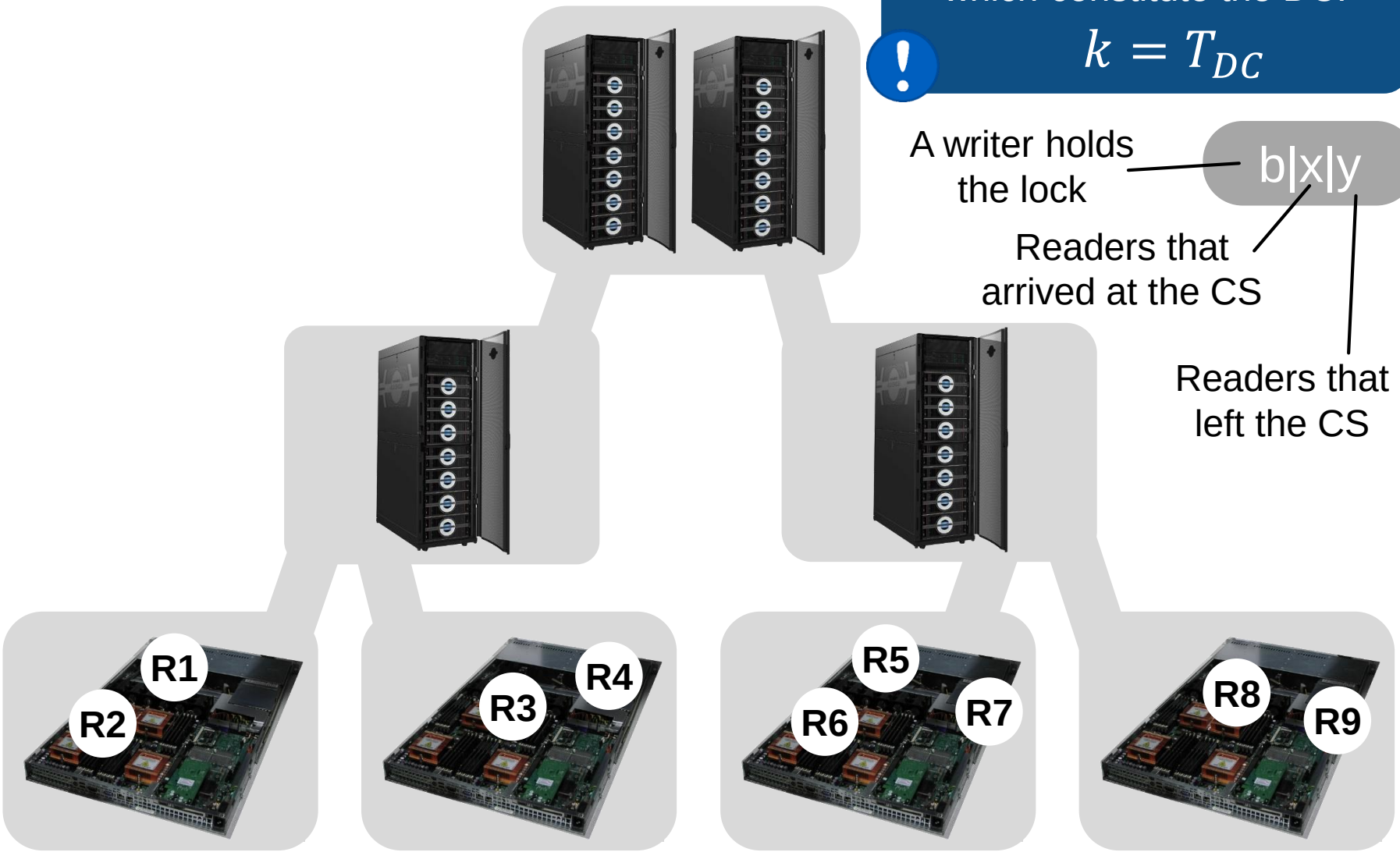

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b|x|y

Readers that arrived at the CS

Readers that left the CS

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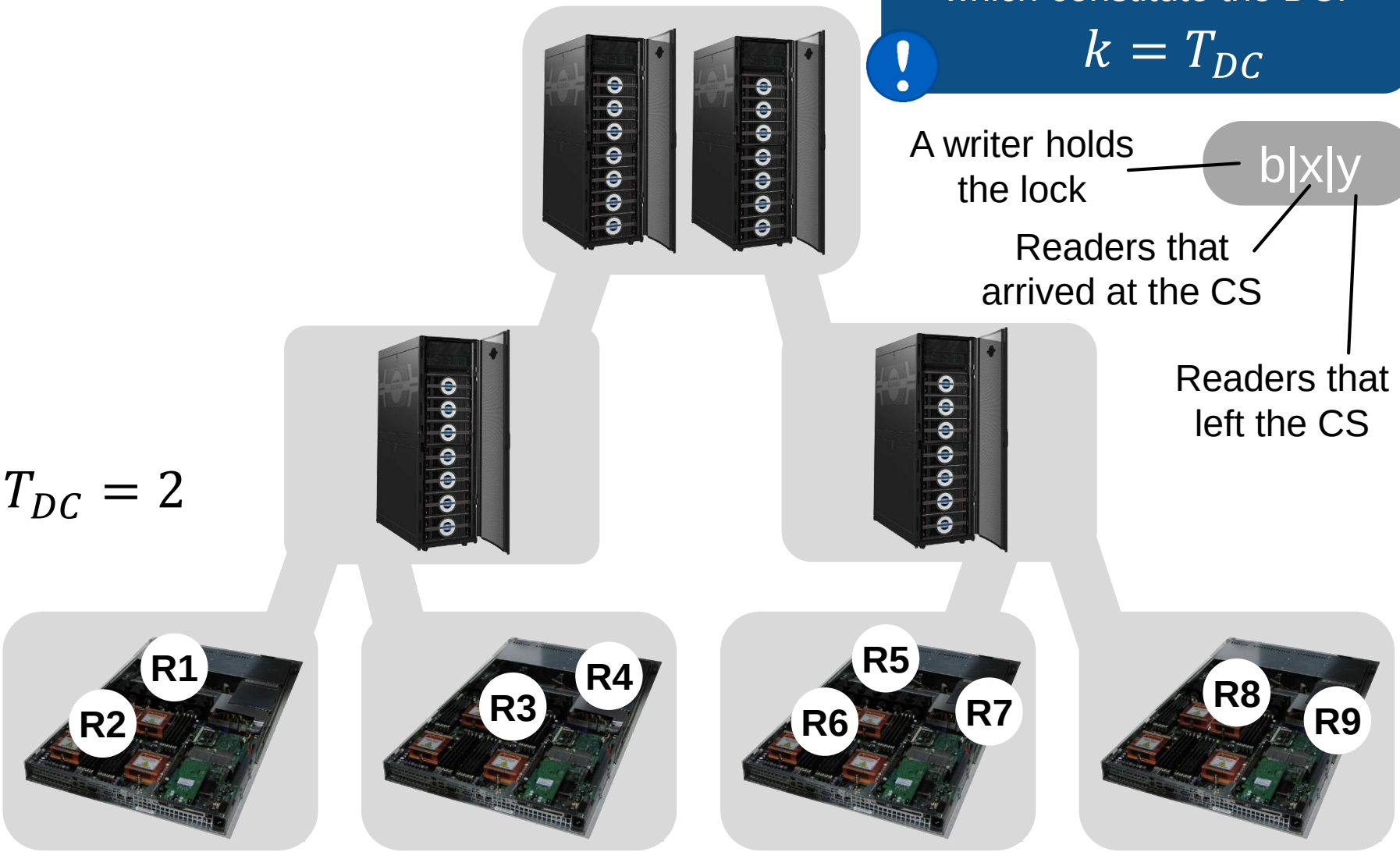

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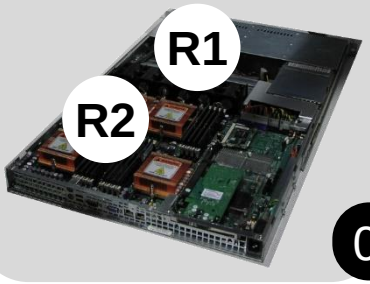

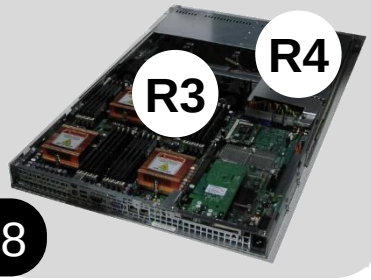

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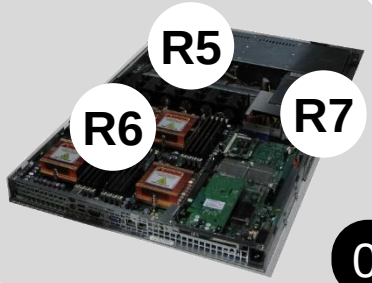

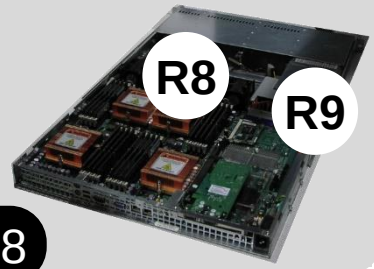

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b|x|y

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The Space of Designs

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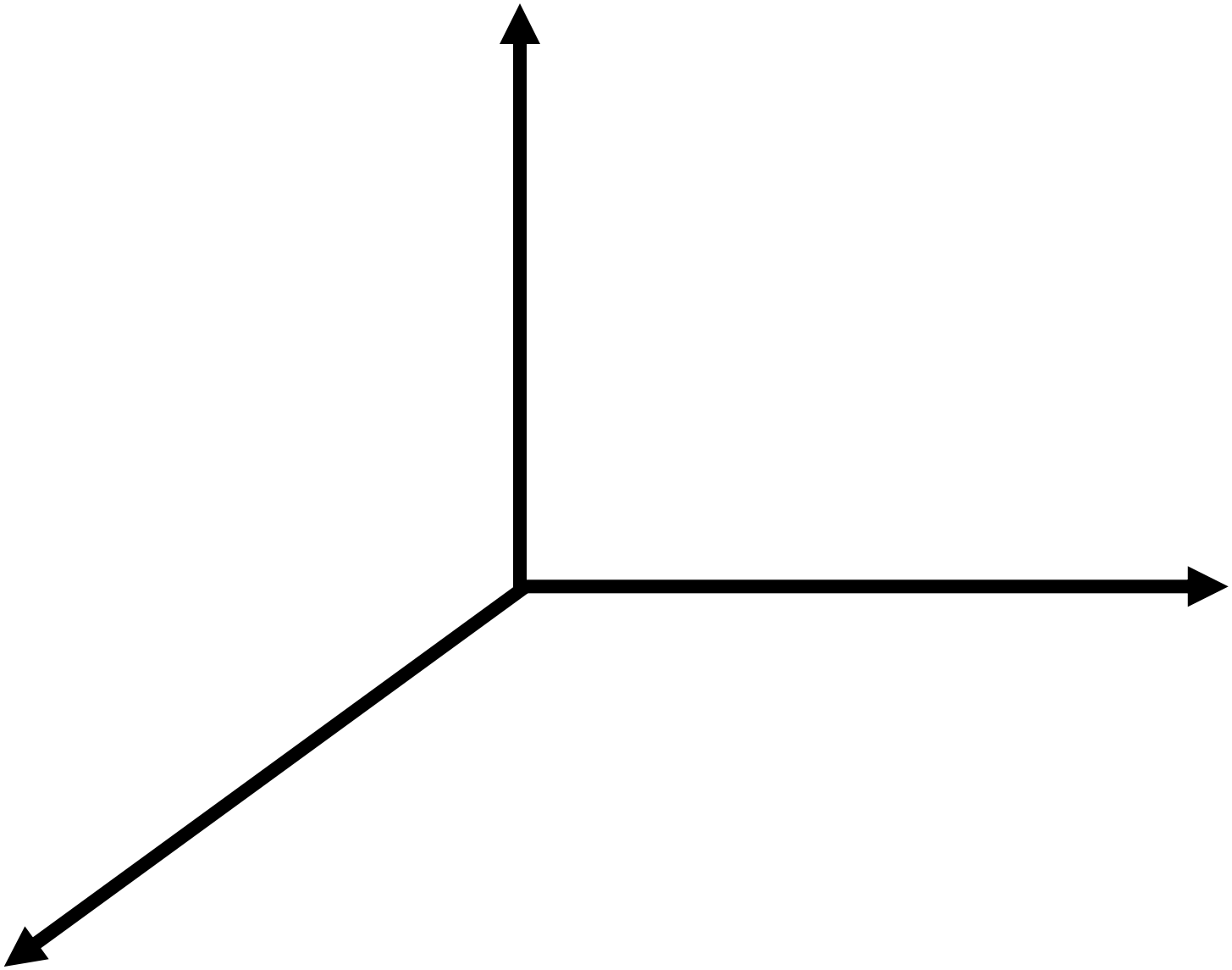

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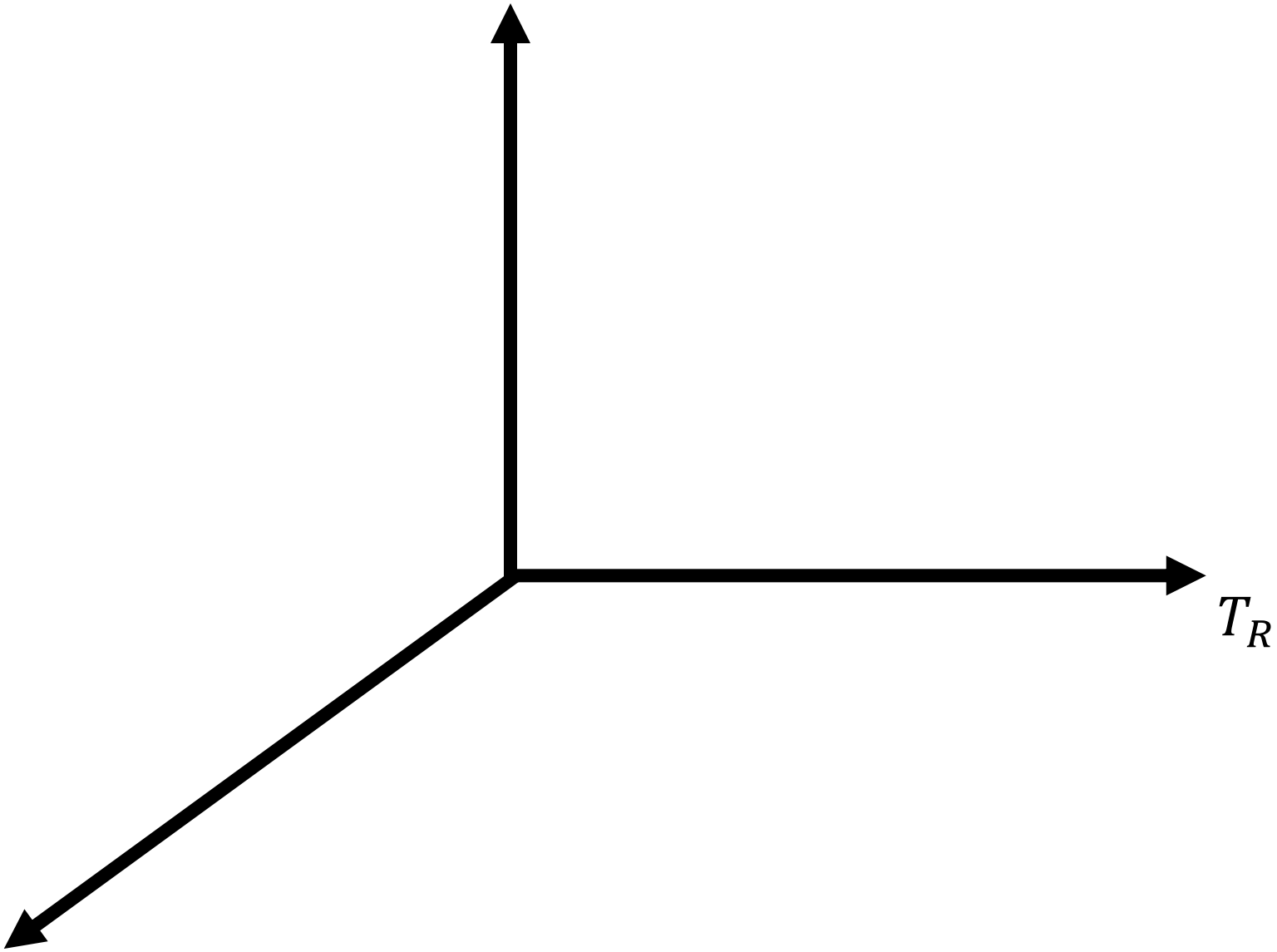

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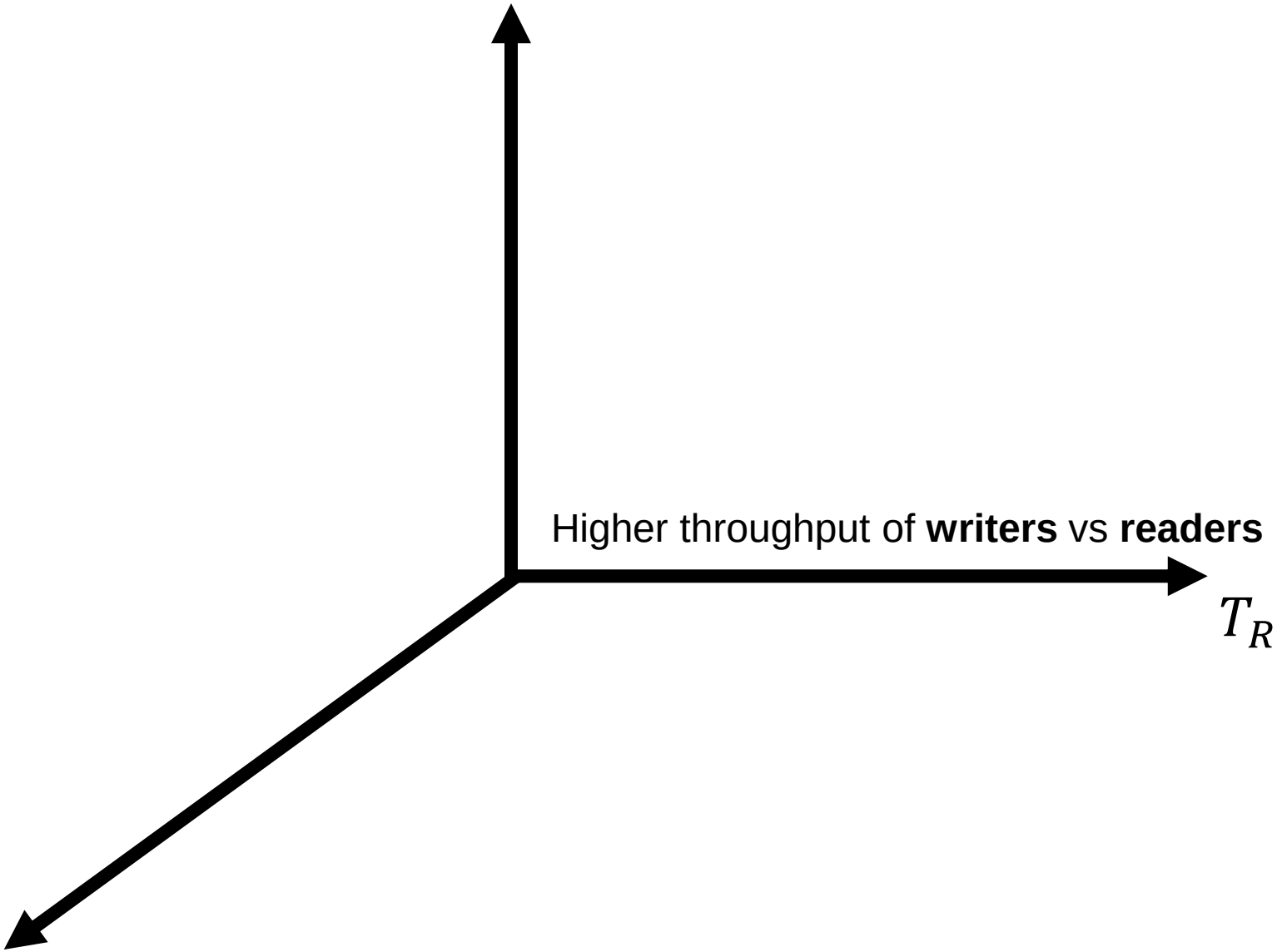

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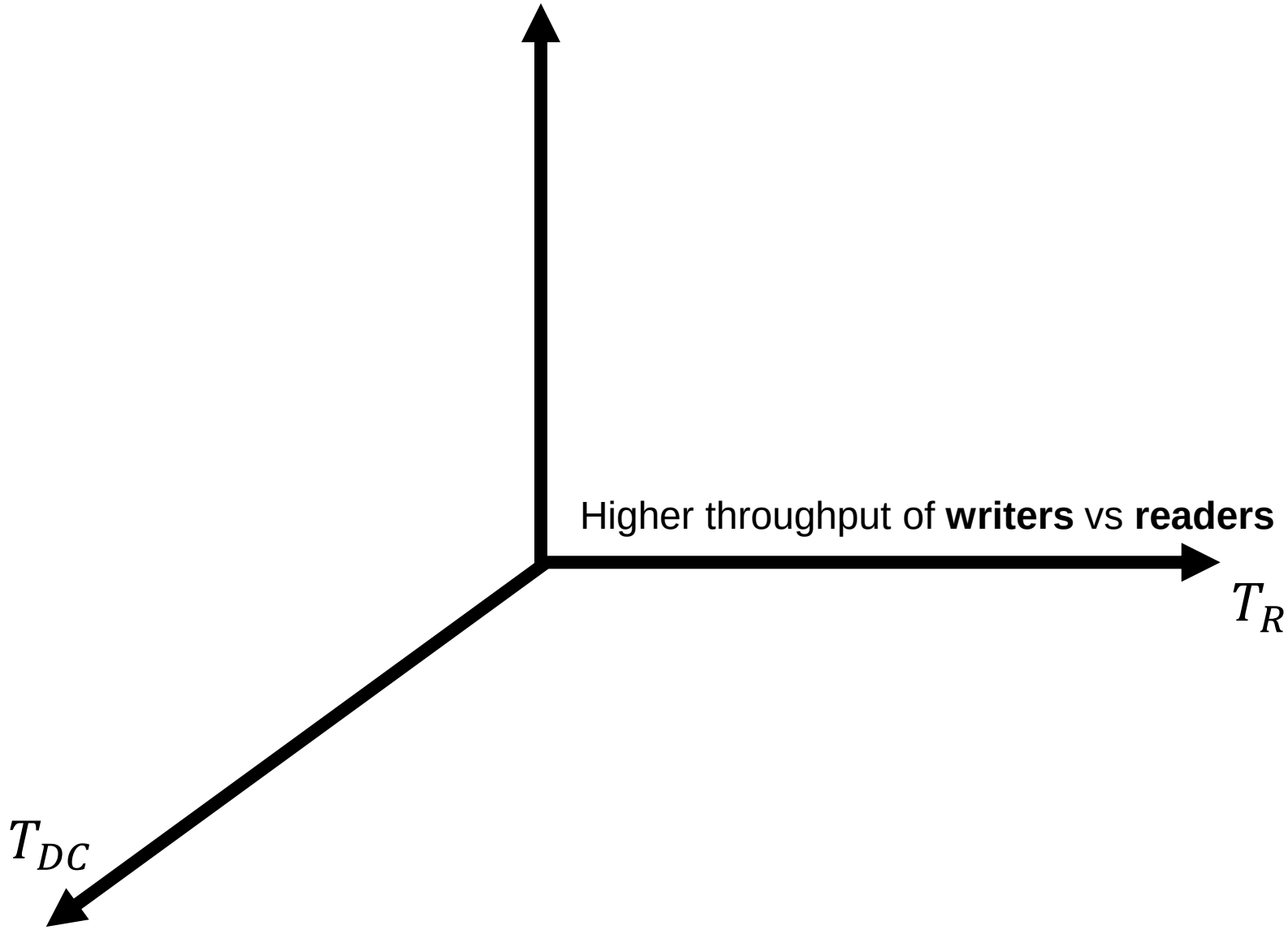

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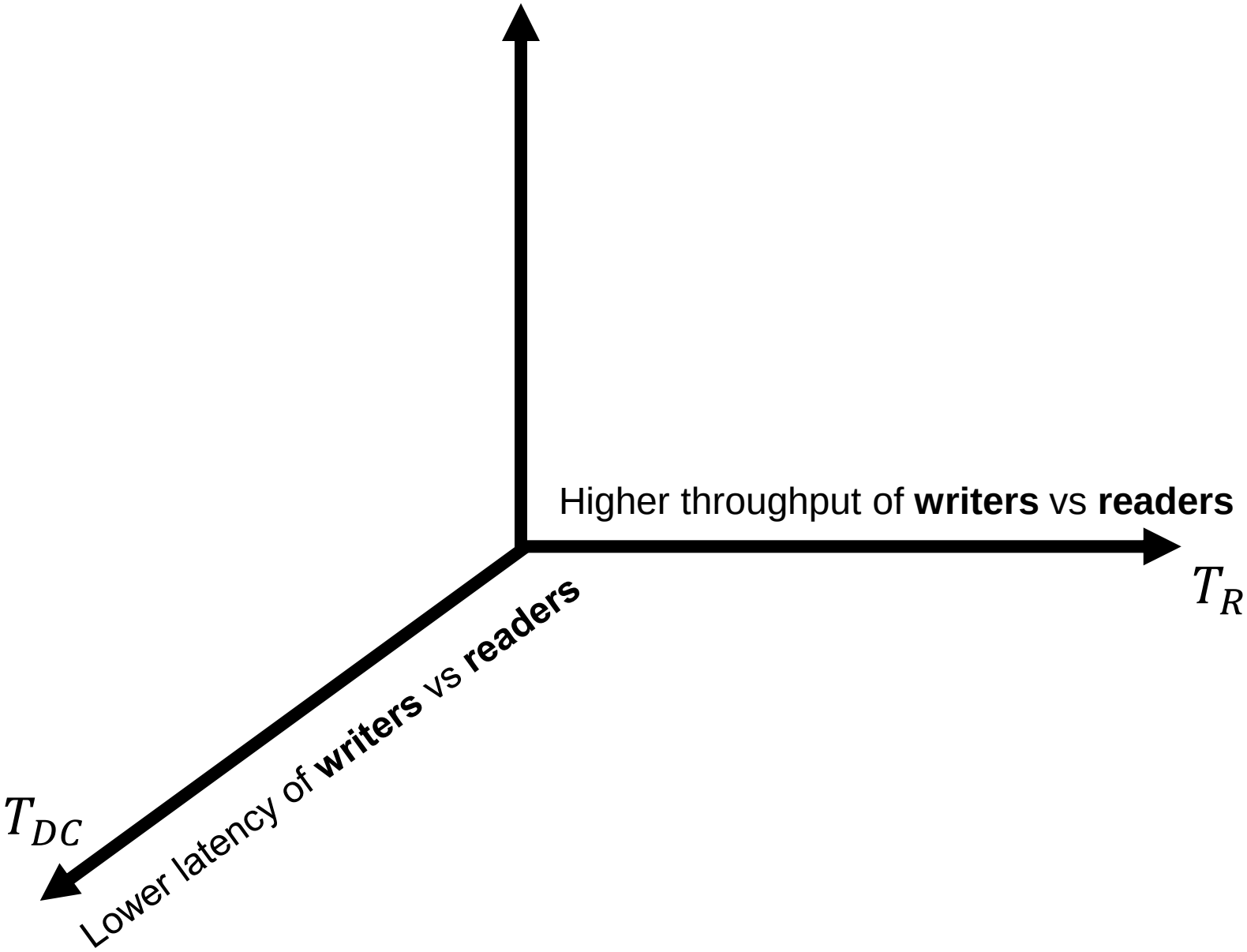

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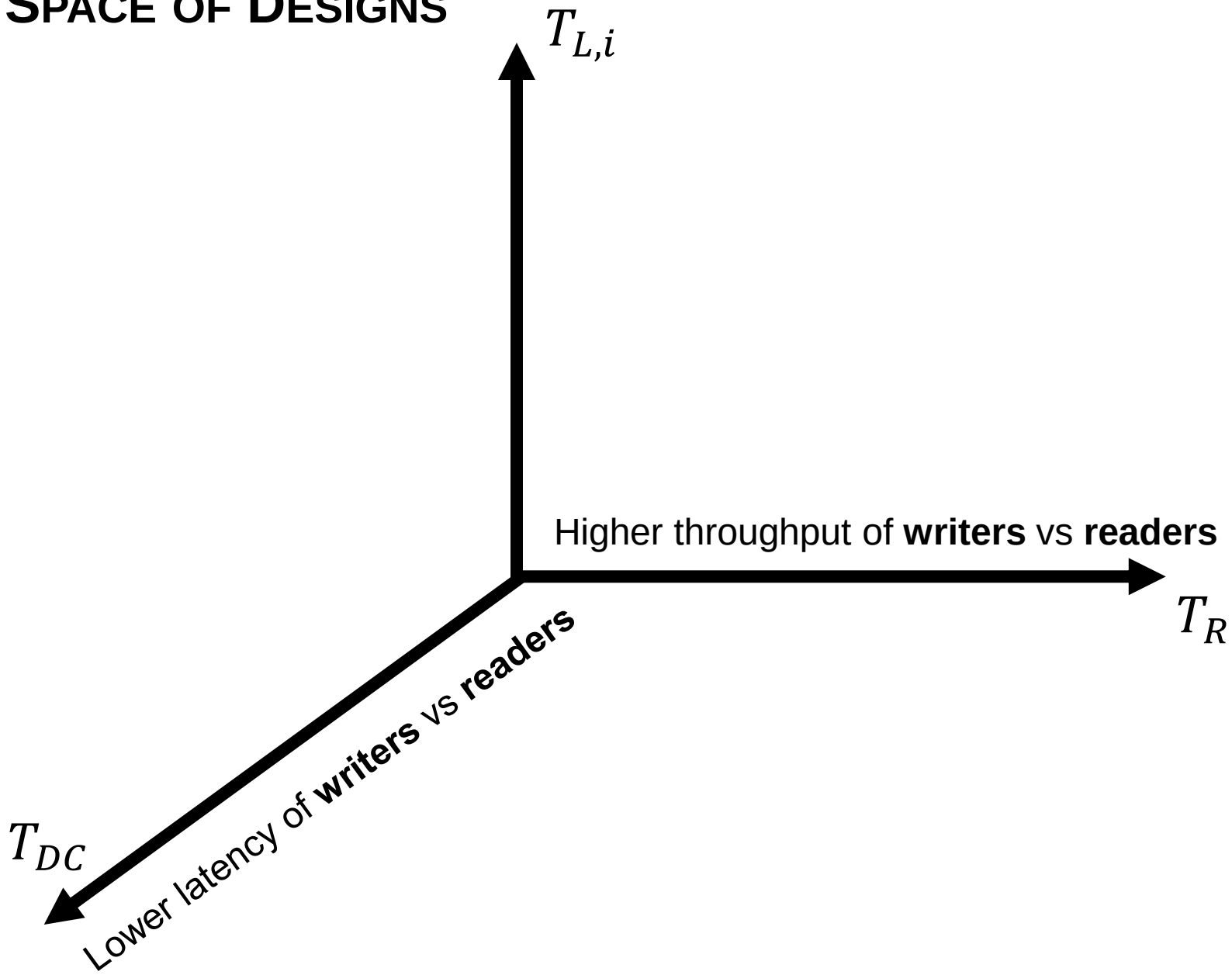

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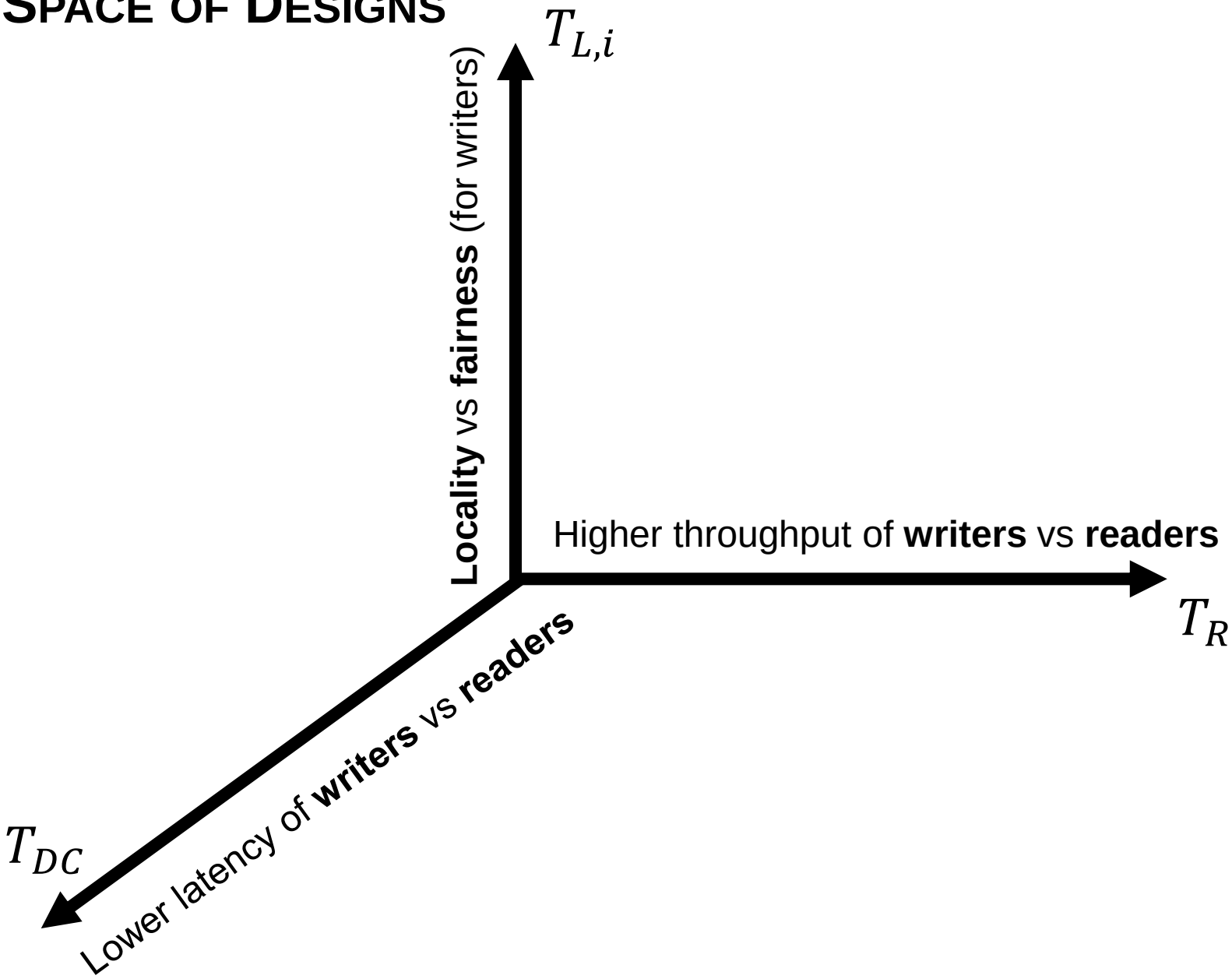

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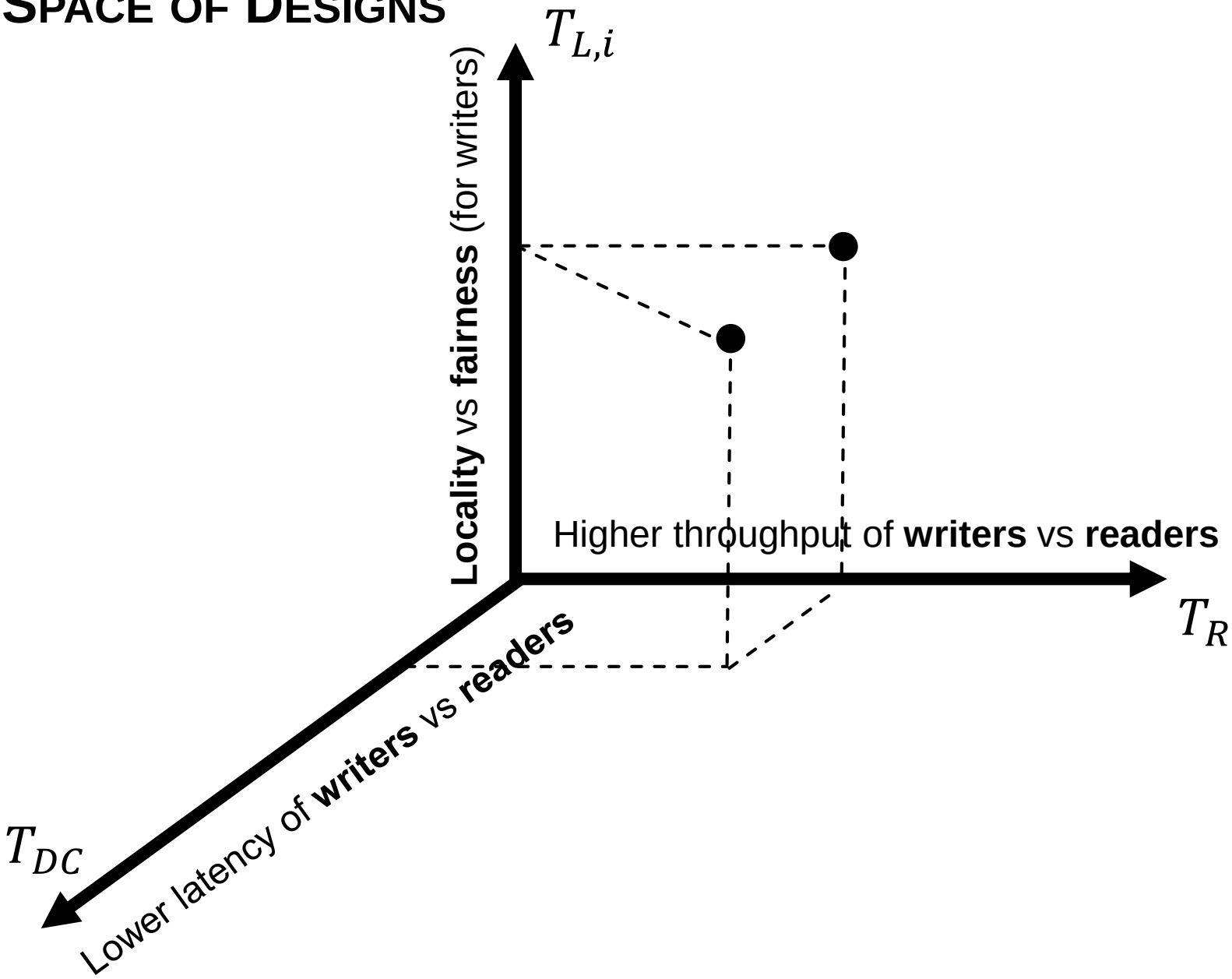

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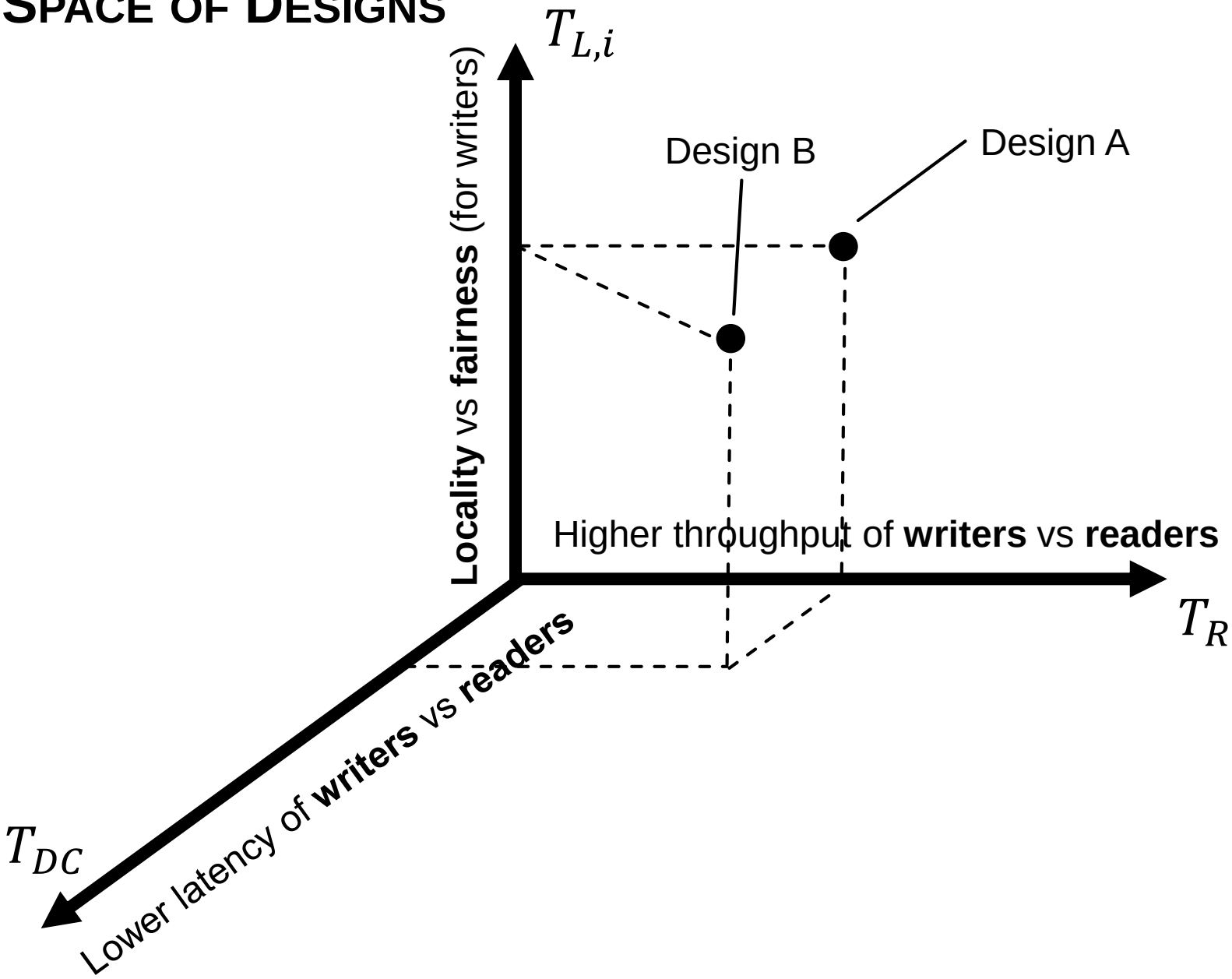
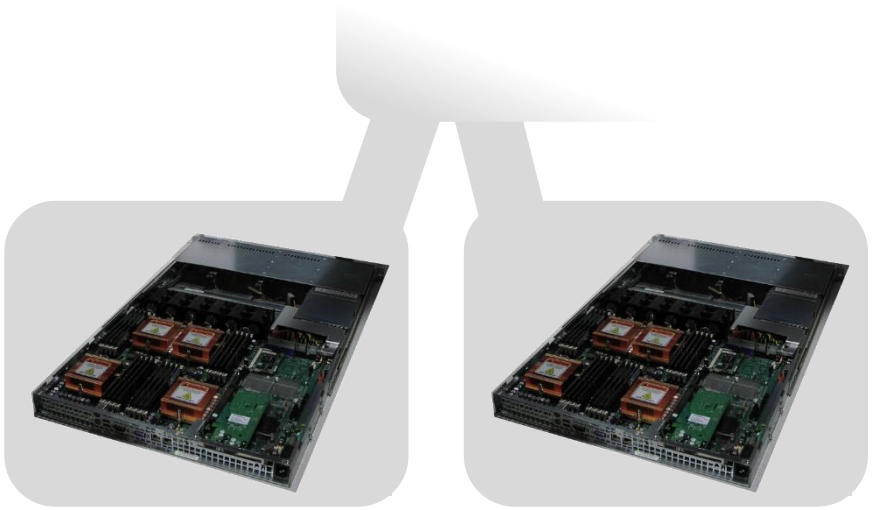


Lock Acquire by Readers



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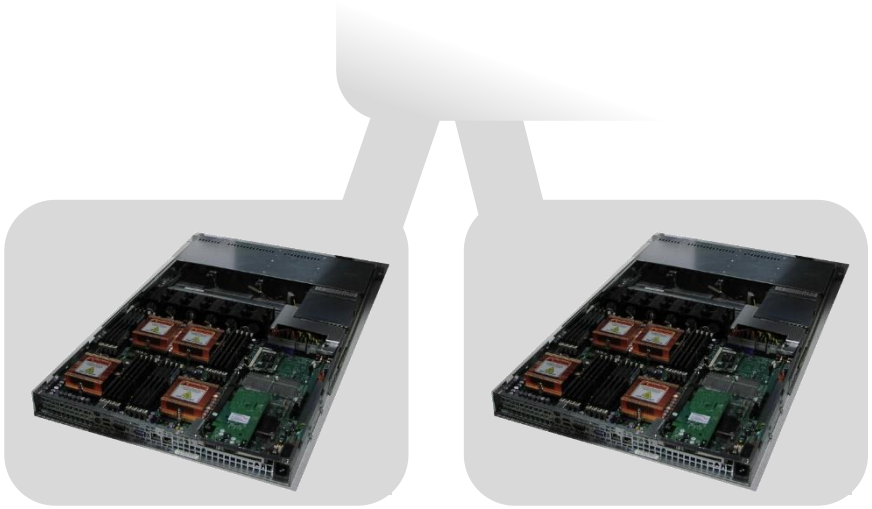
A lightweight acquire protocol for readers: only one atomic fetch-and-add (FAA) operation



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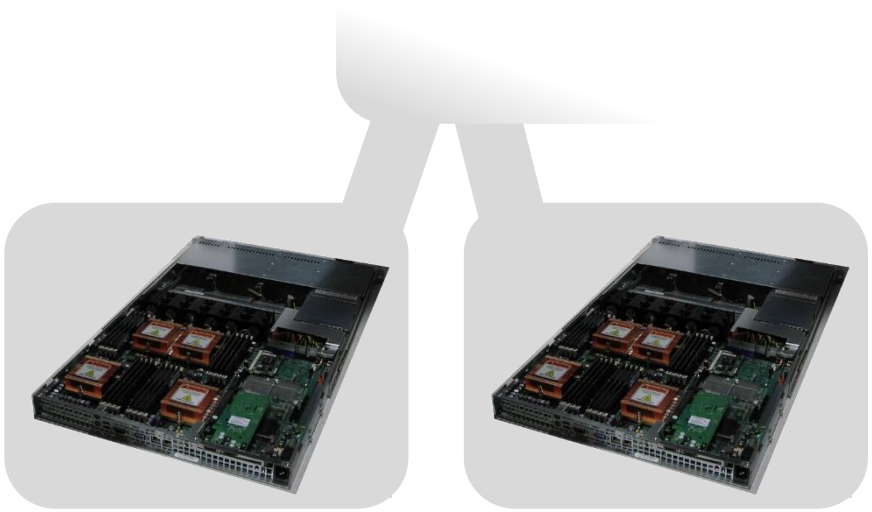

A writer holds the lock

b|x|y

Readers that arrived at the CS

Readers that left the CS

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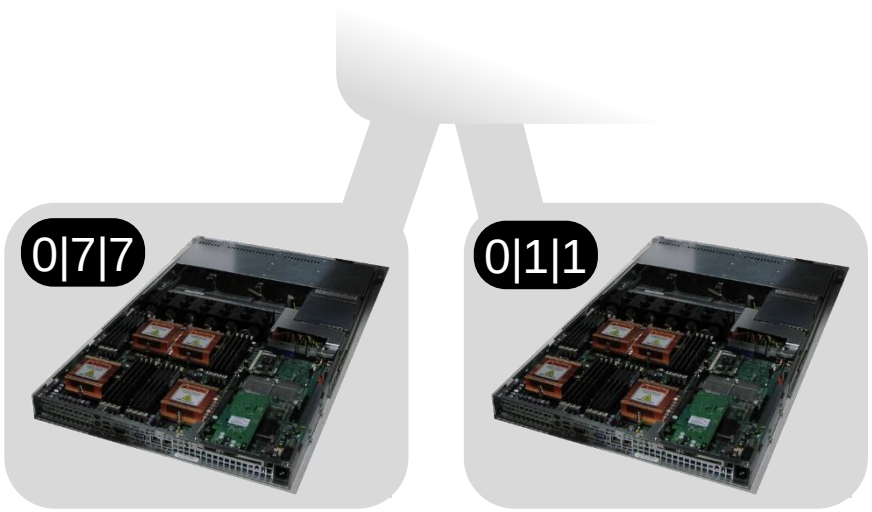

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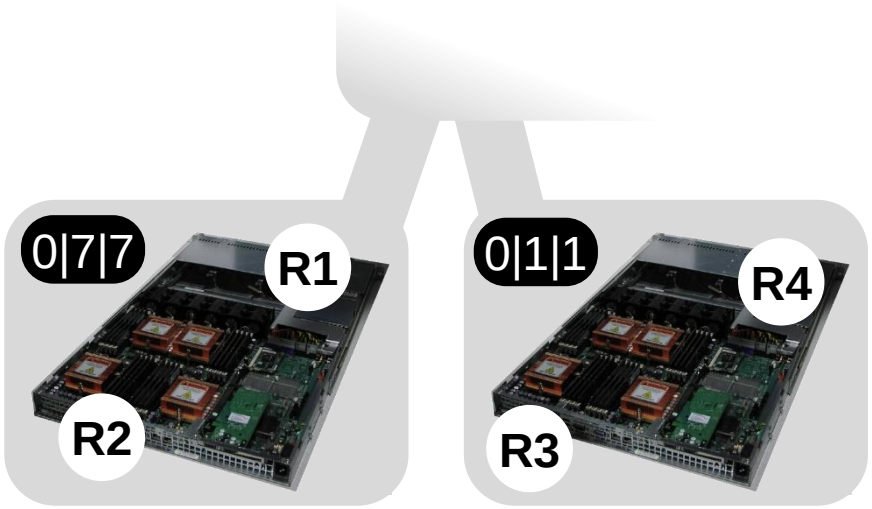

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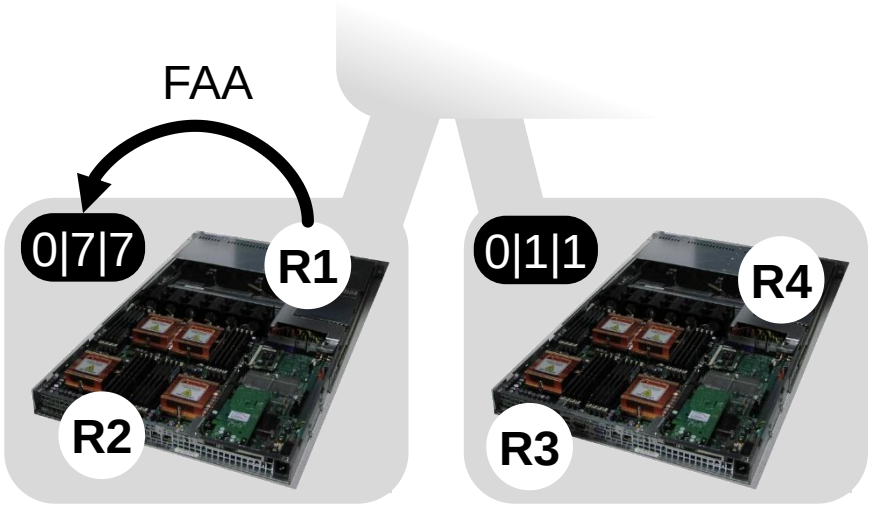

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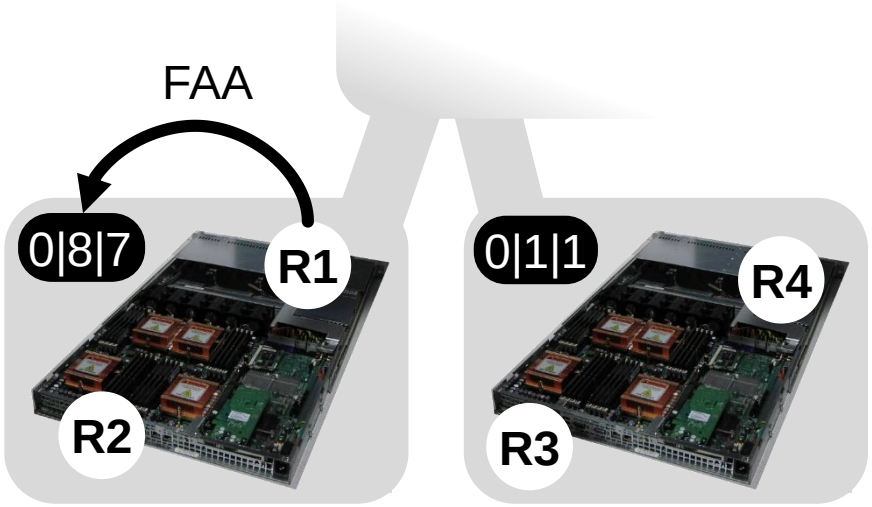


A writer holds the lock

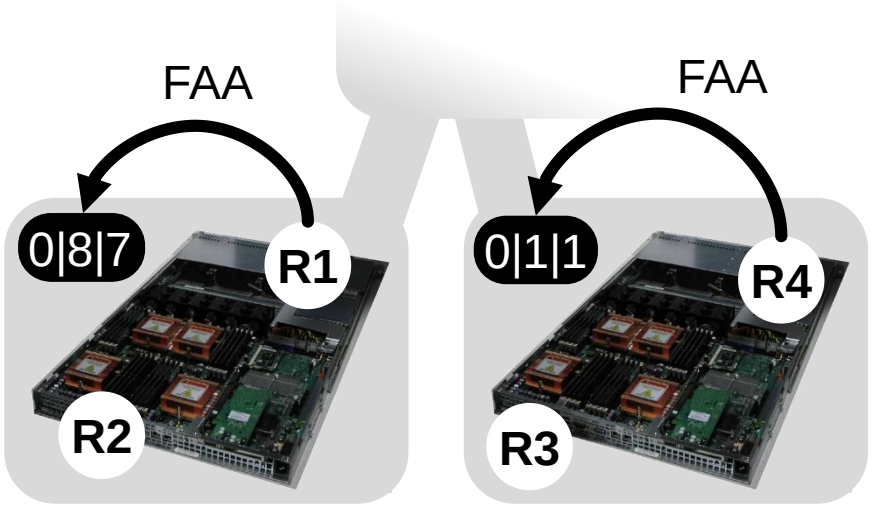
b|x|y

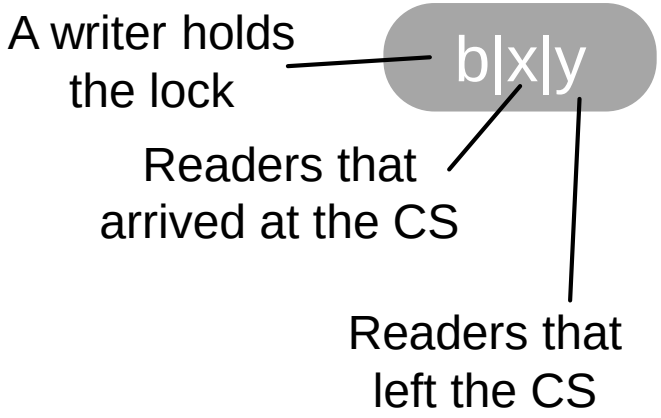
Readers that arrived at the CS

Readers that left the CS

Lock Acquire by Readers

A lightweight acquire protocol for readers: only one atomic fetch-and-add (FAA) operation





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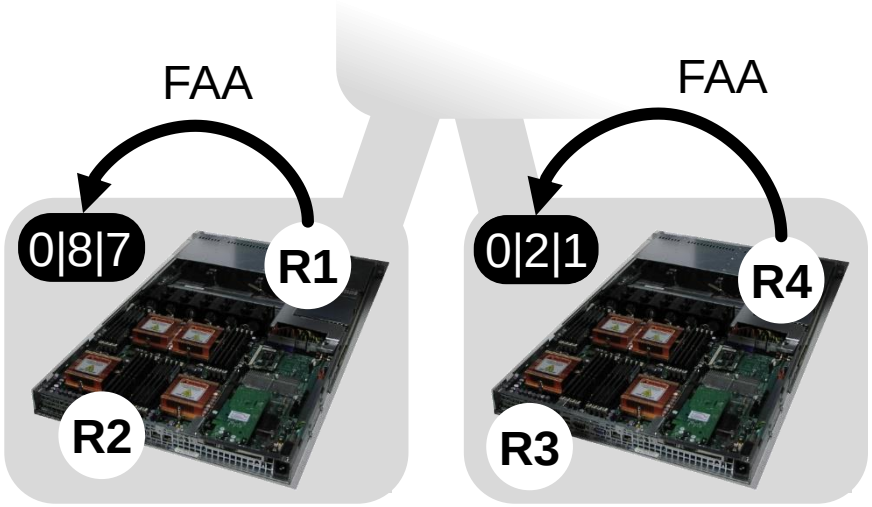

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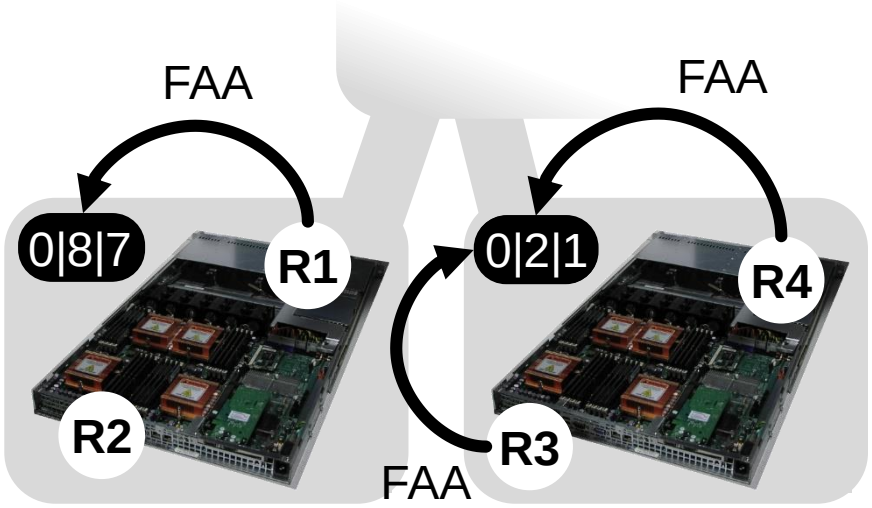

A writer holds the lock

b|x|y

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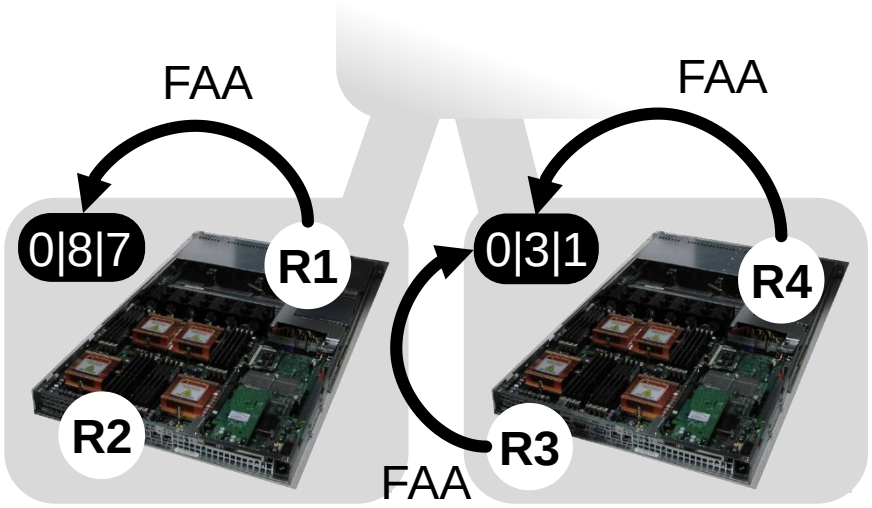

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b|x|y

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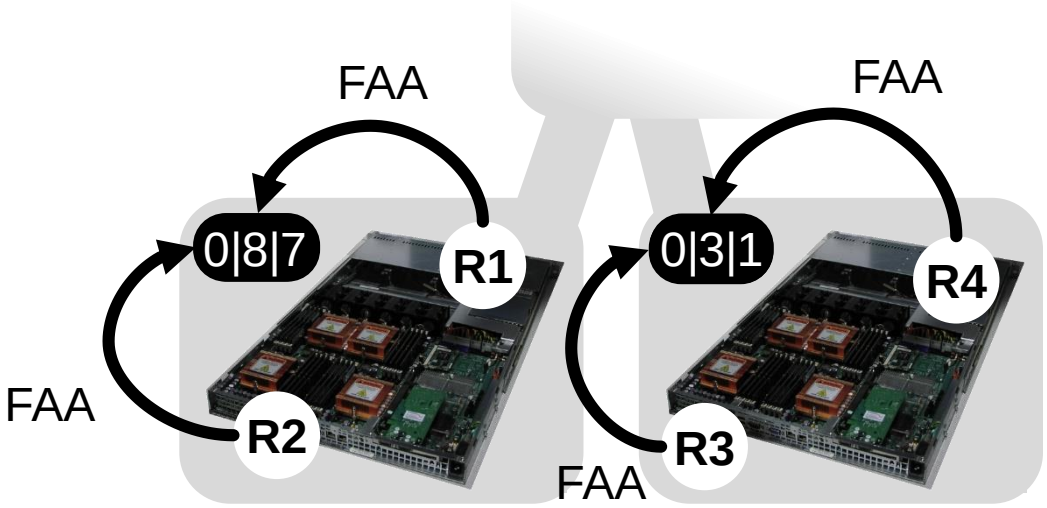

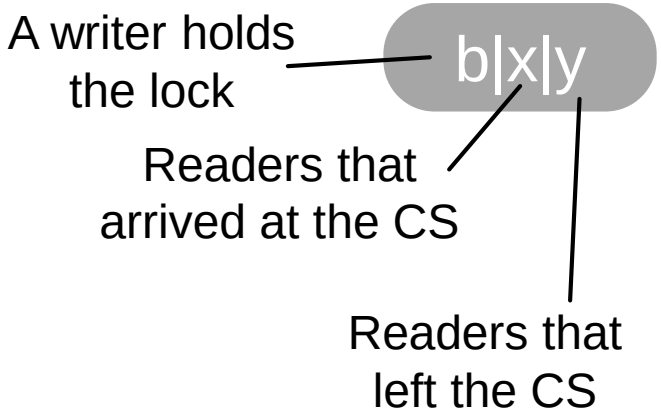

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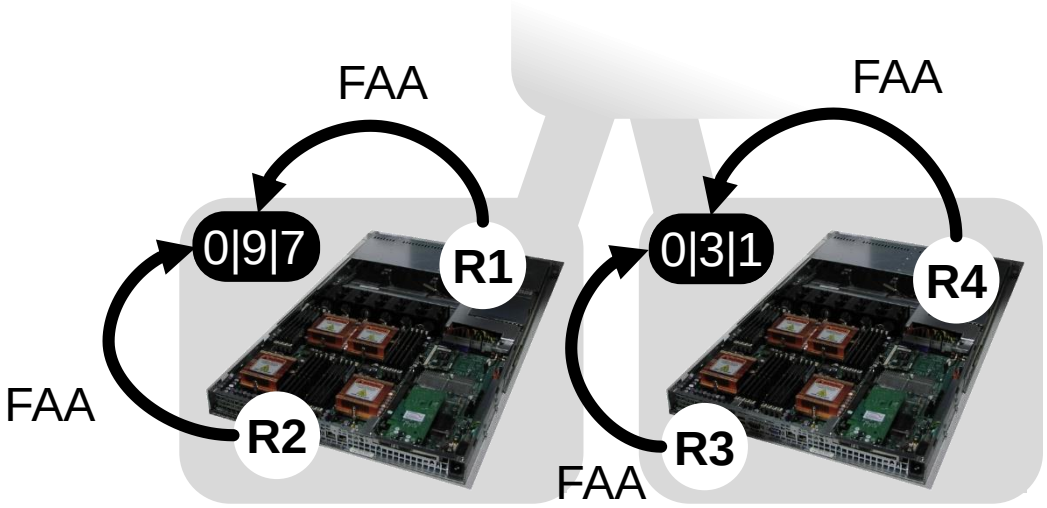

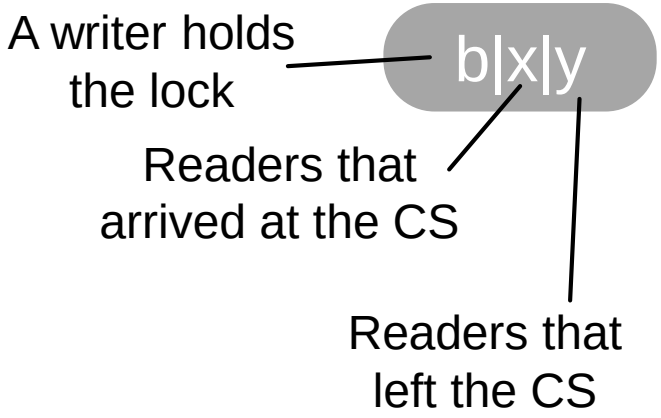

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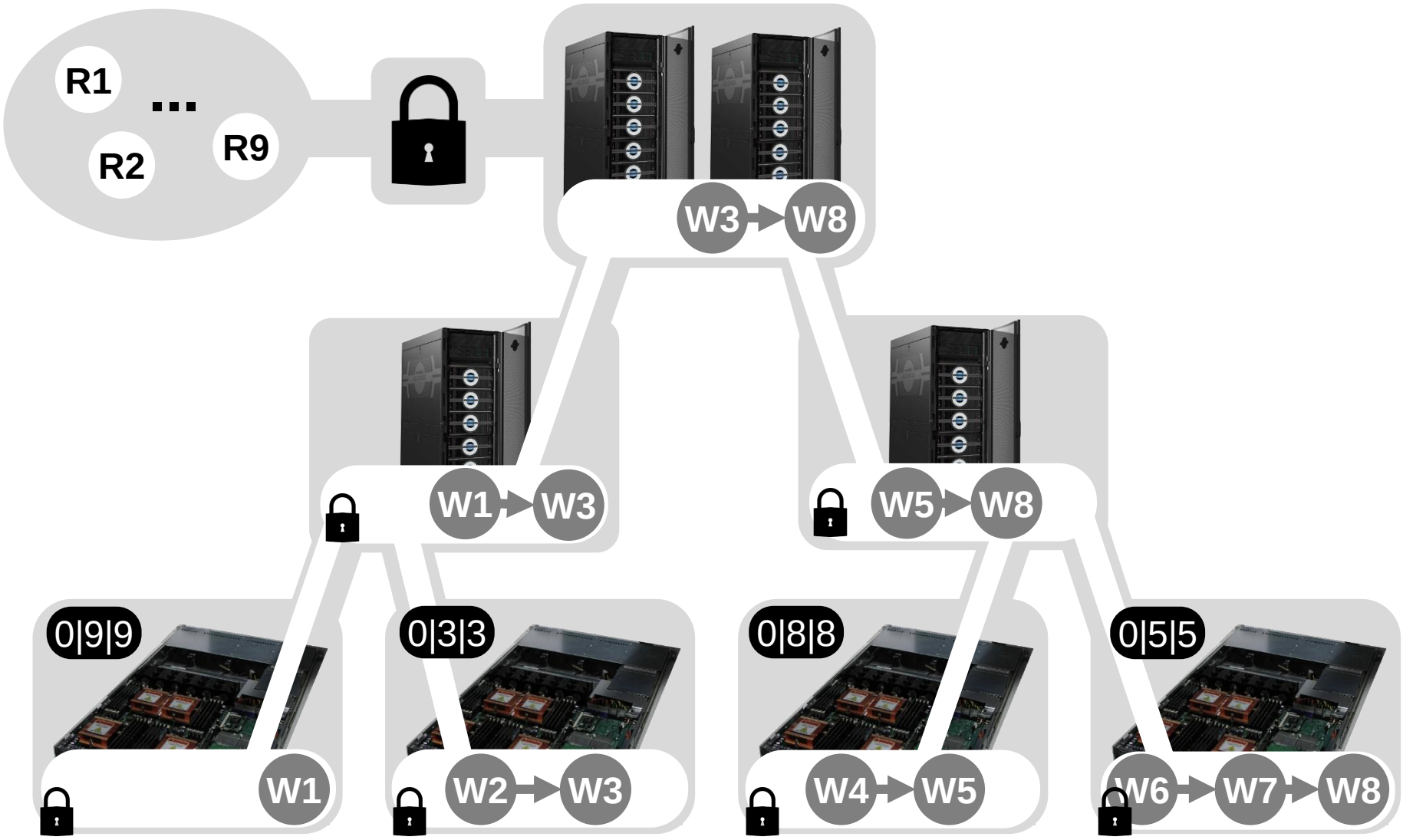

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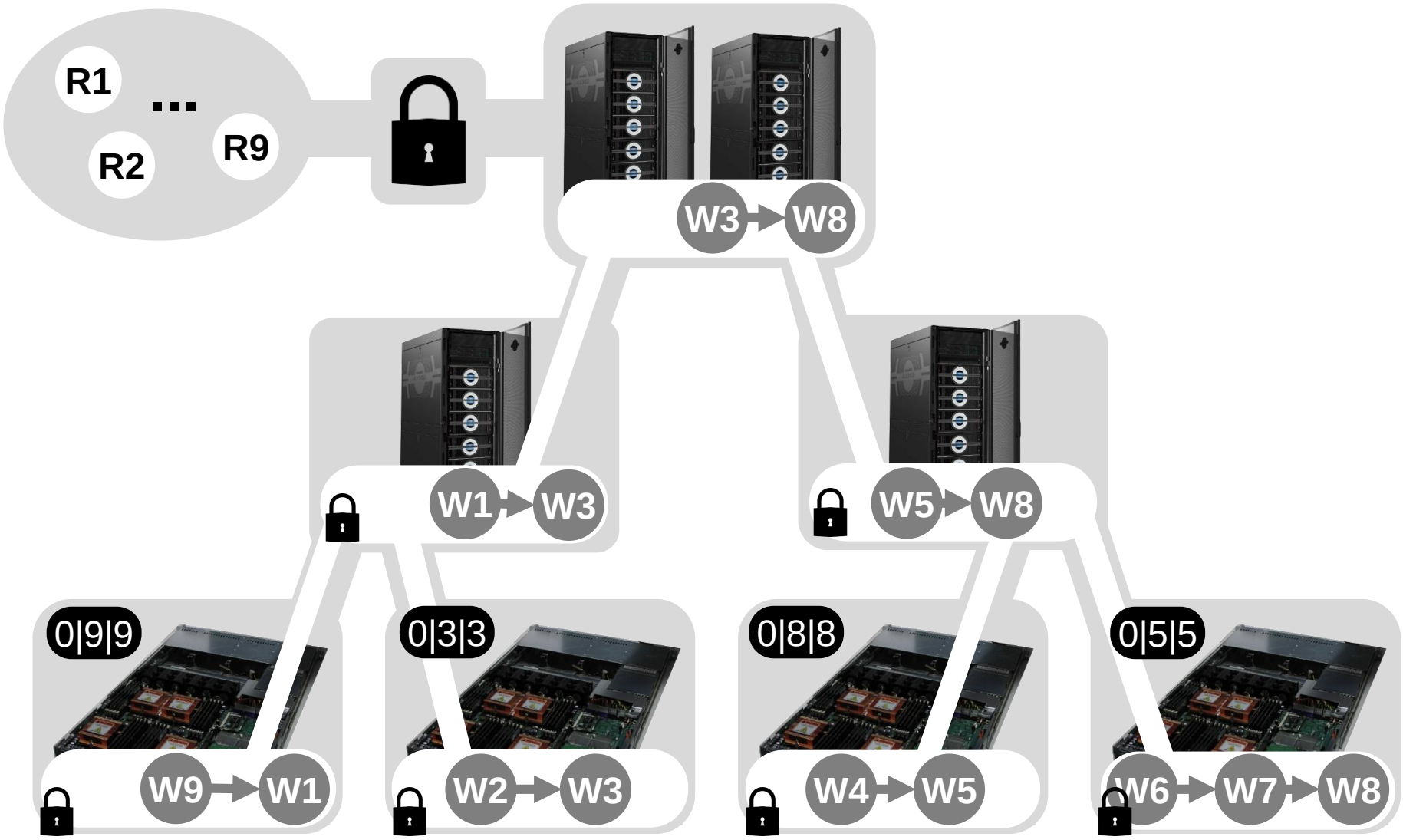

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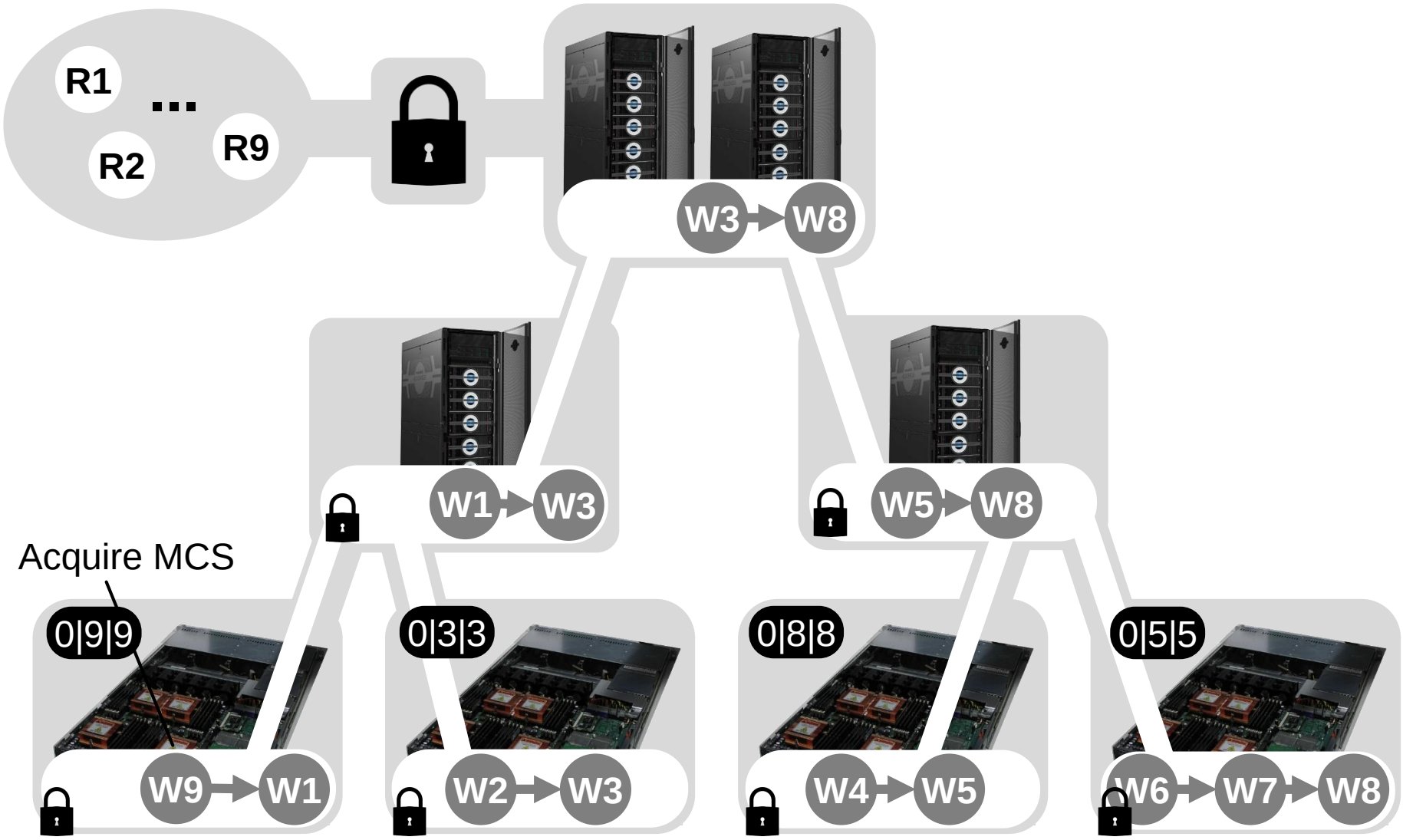

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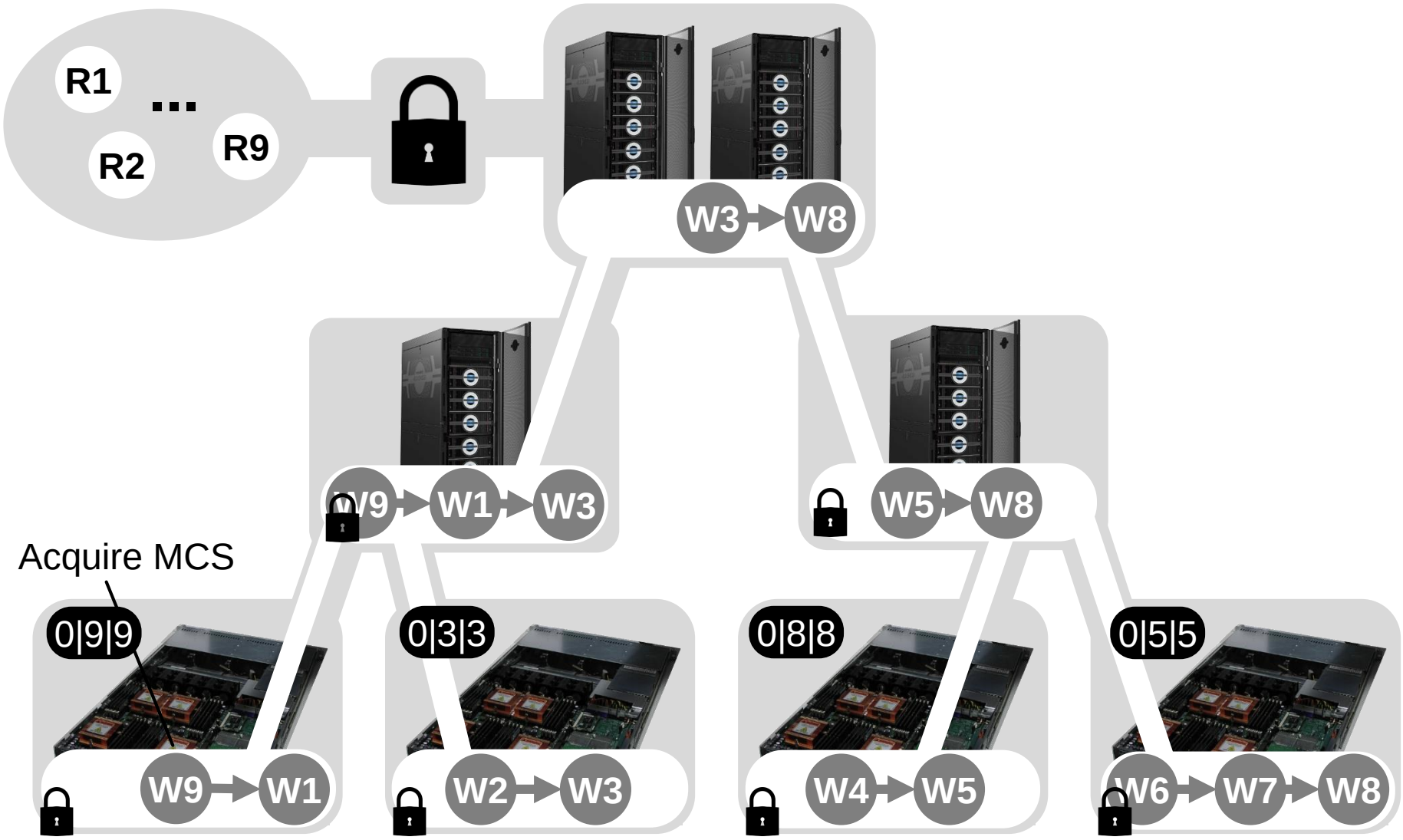

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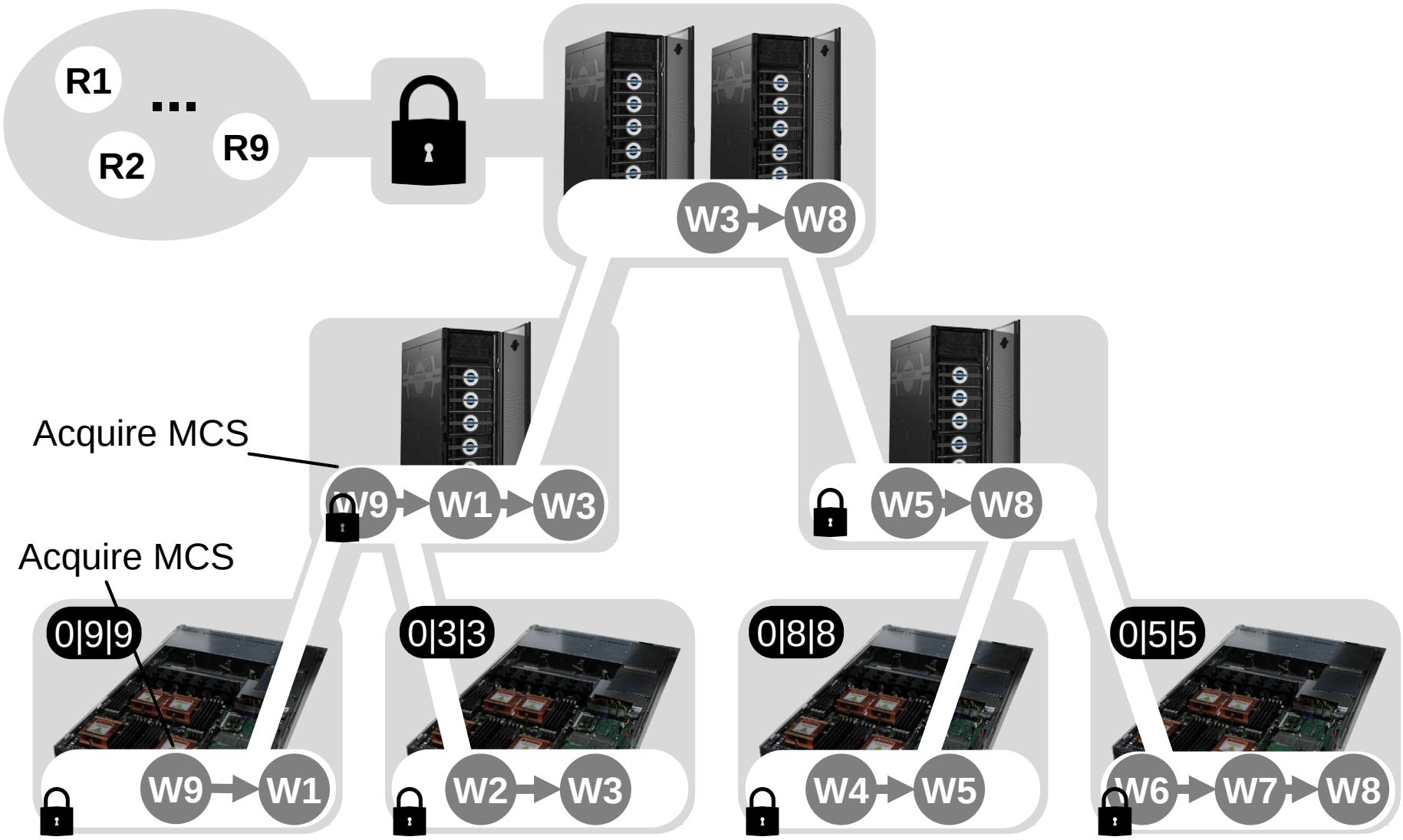

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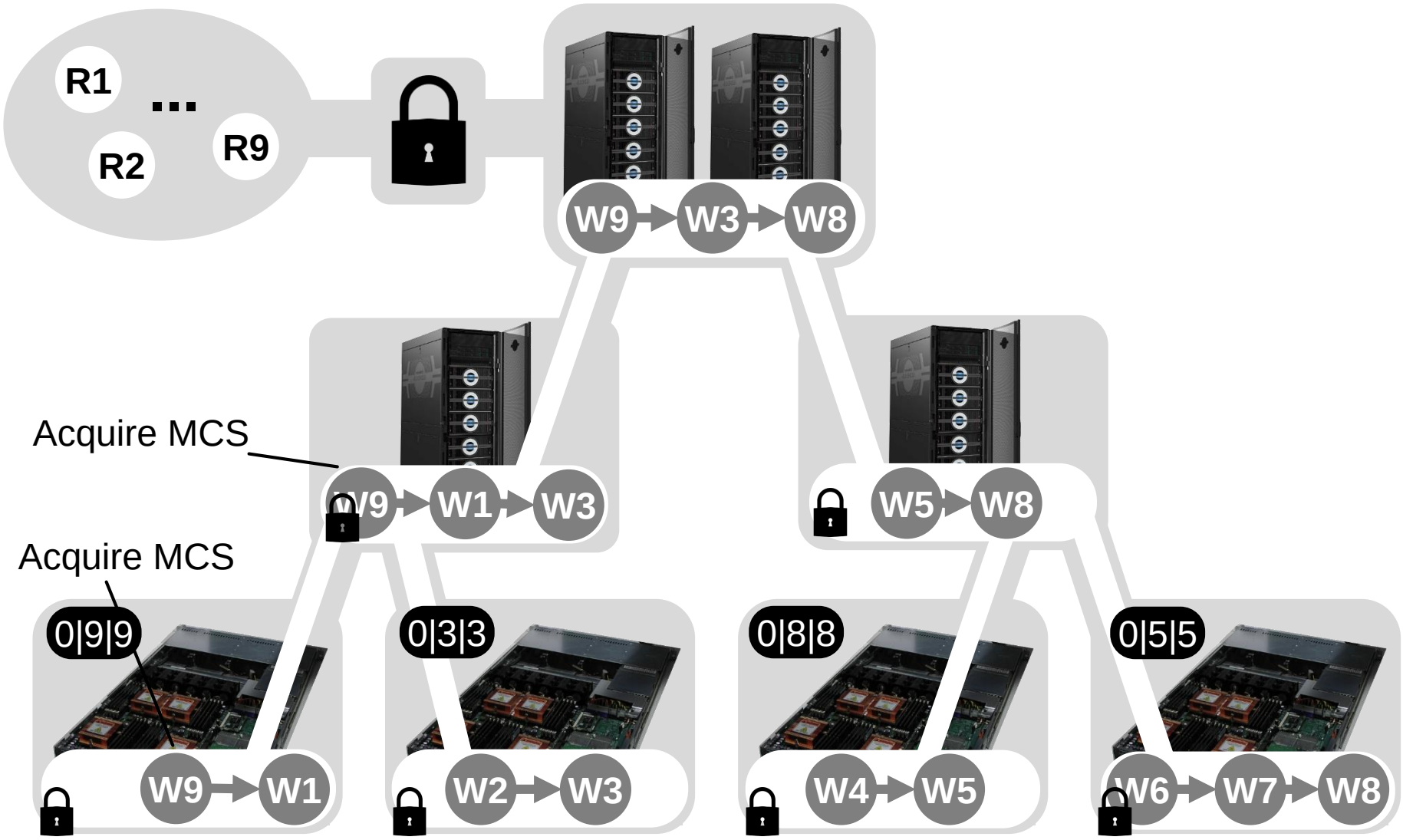

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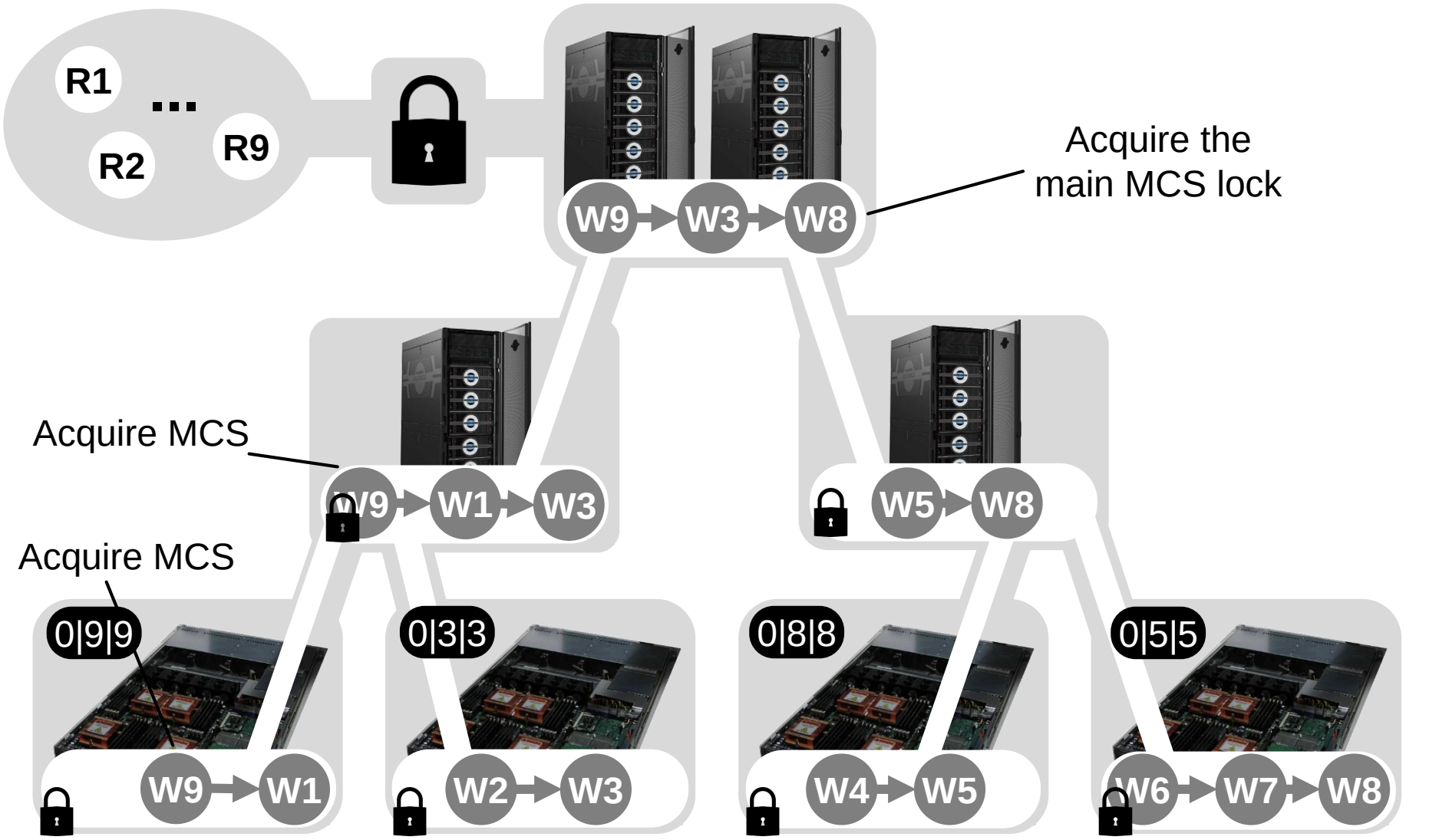

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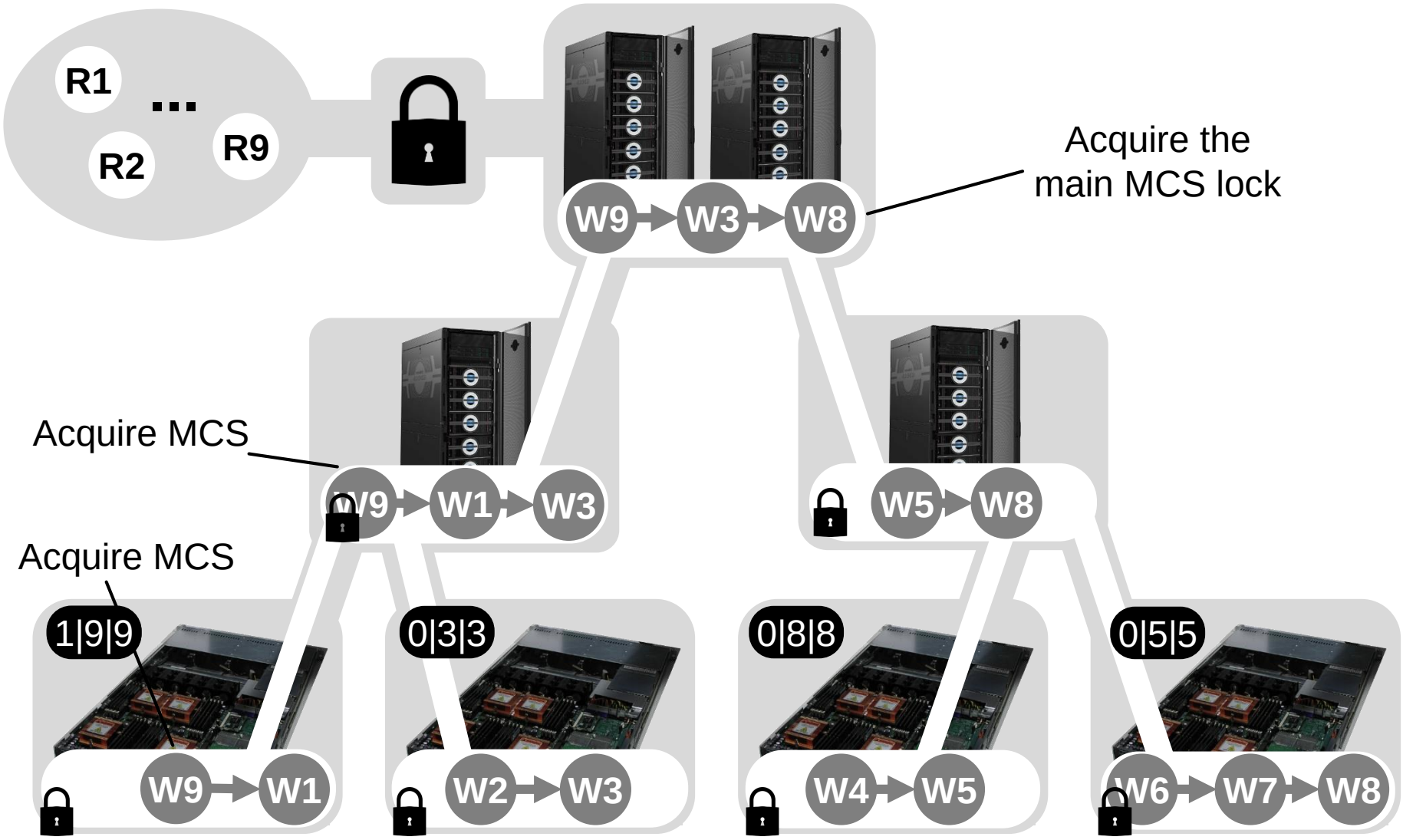

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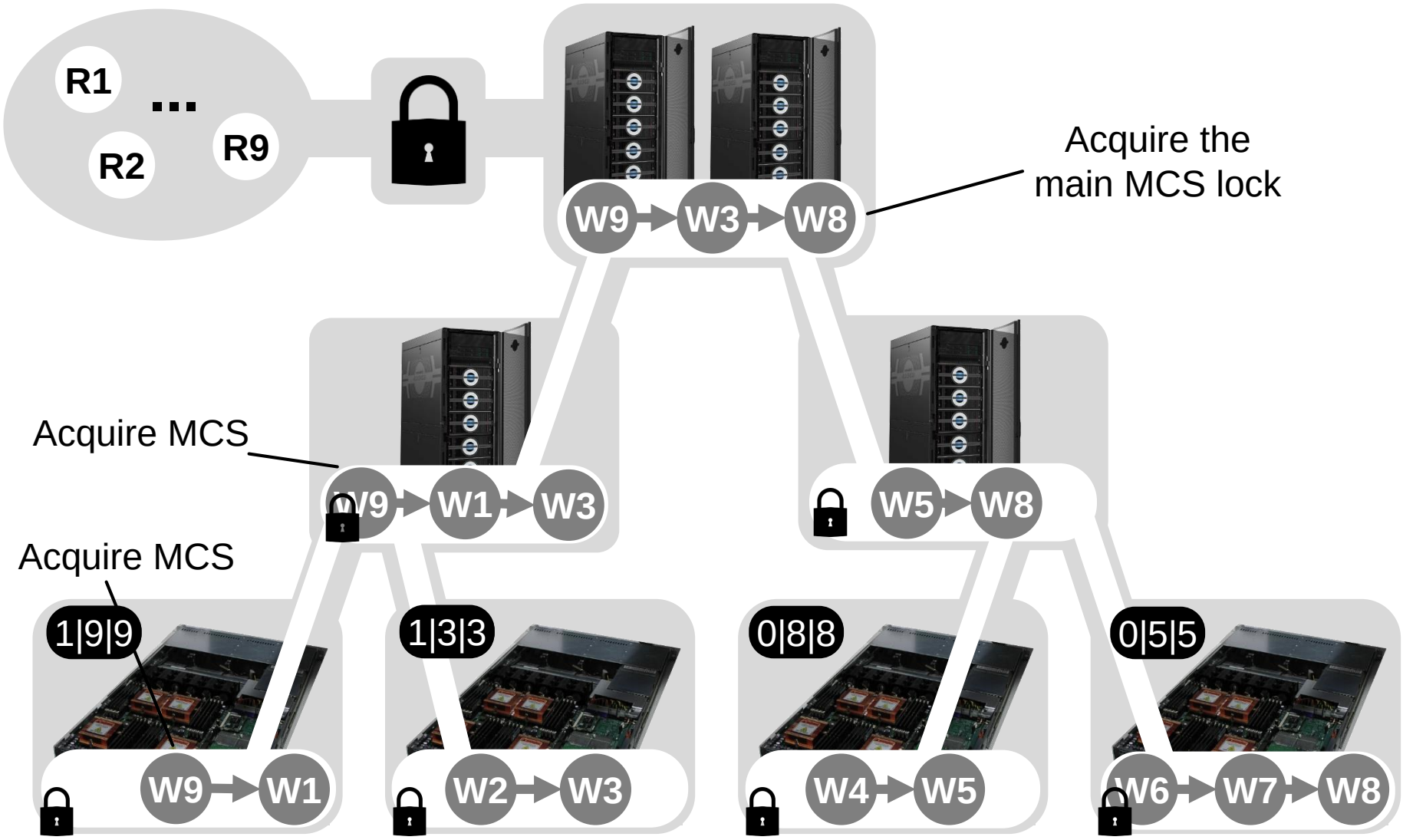

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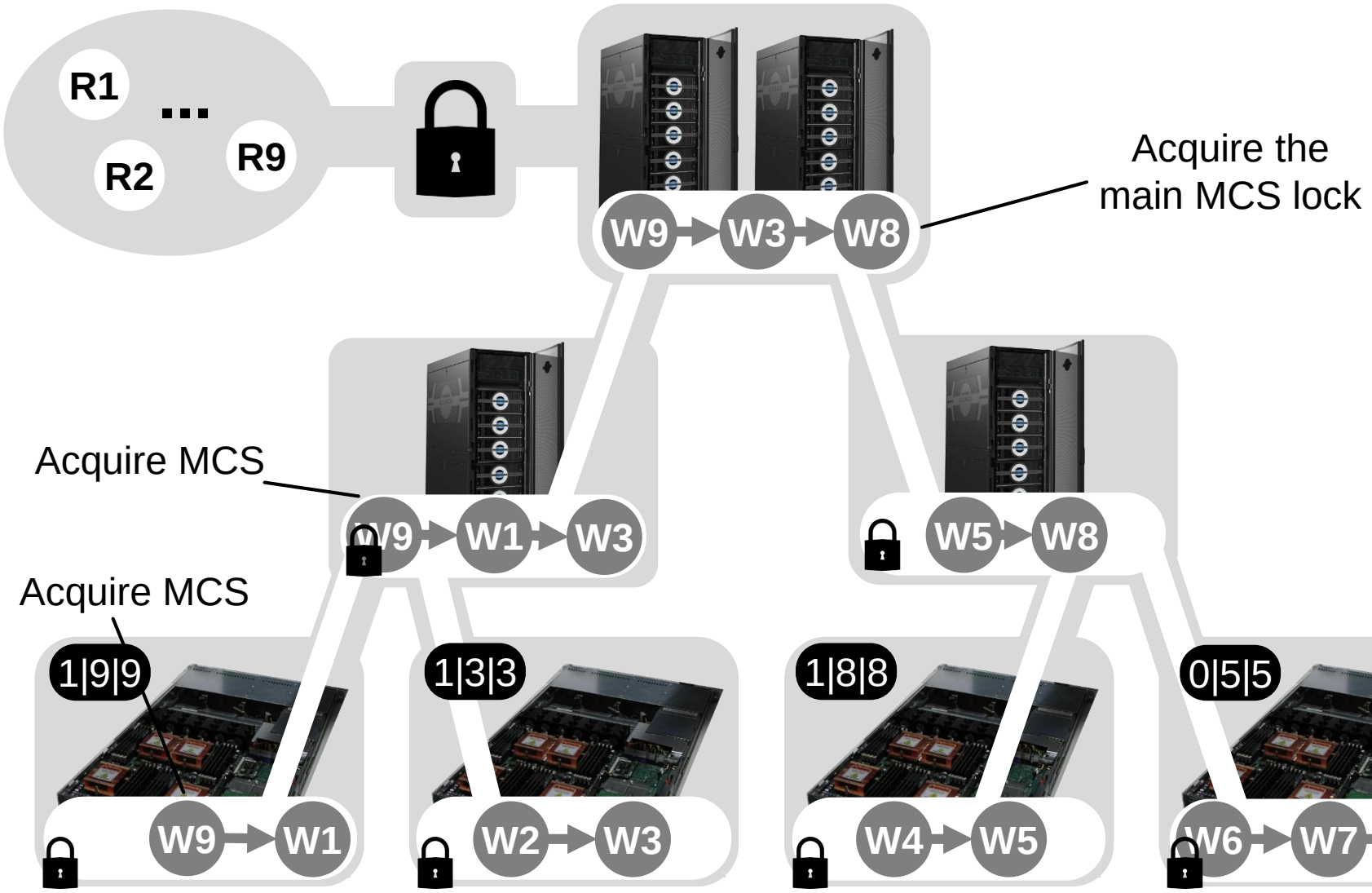

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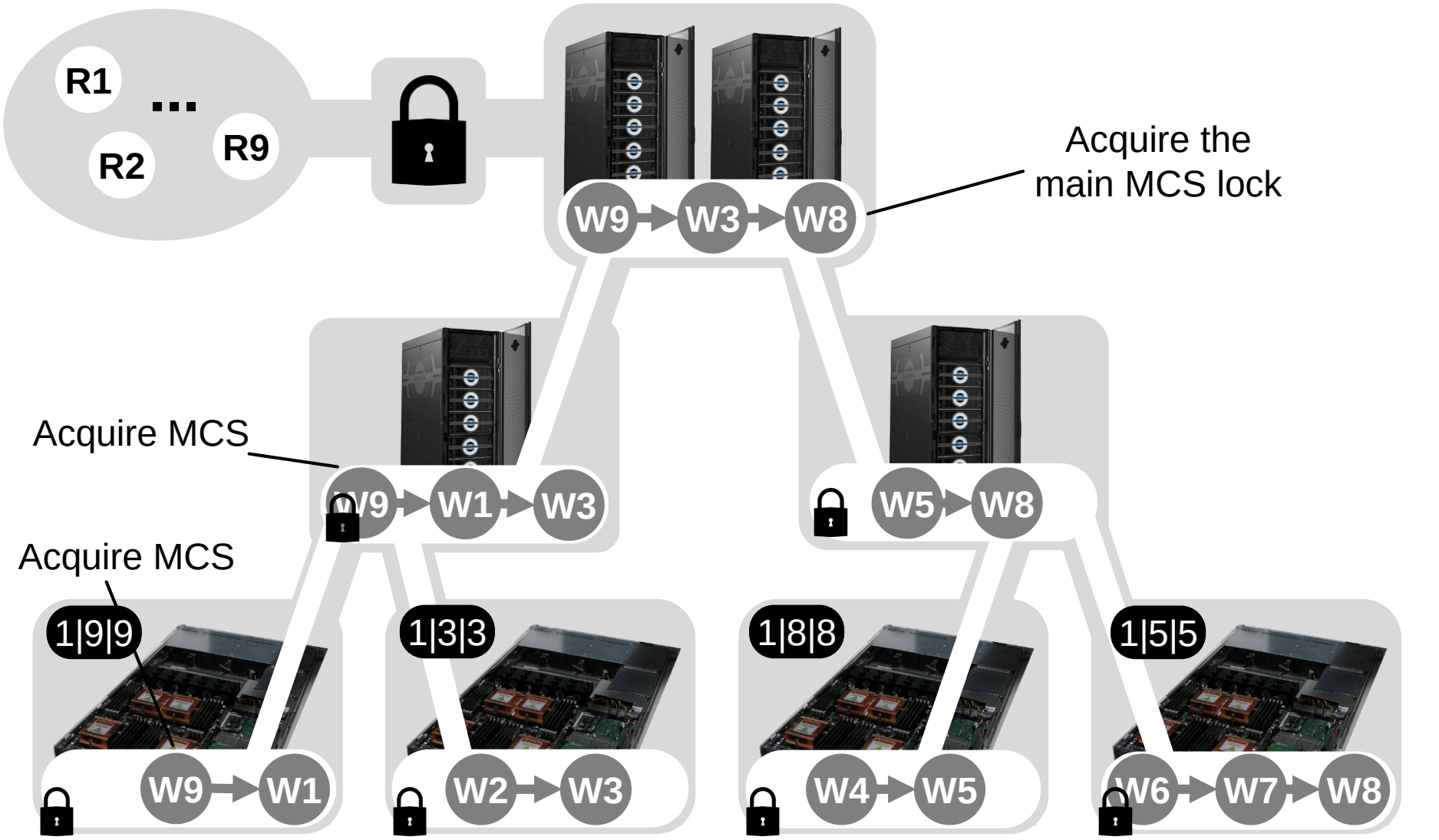

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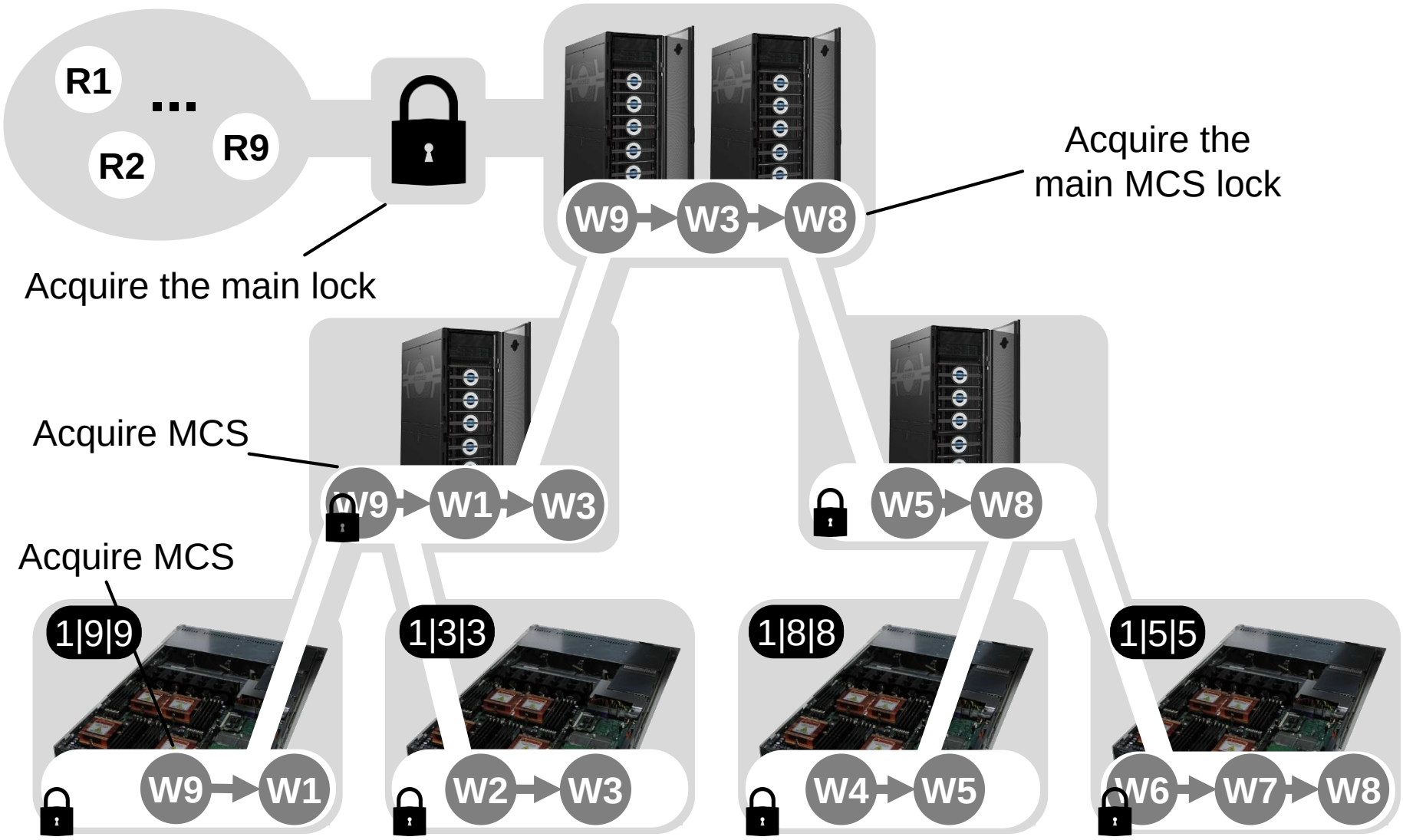
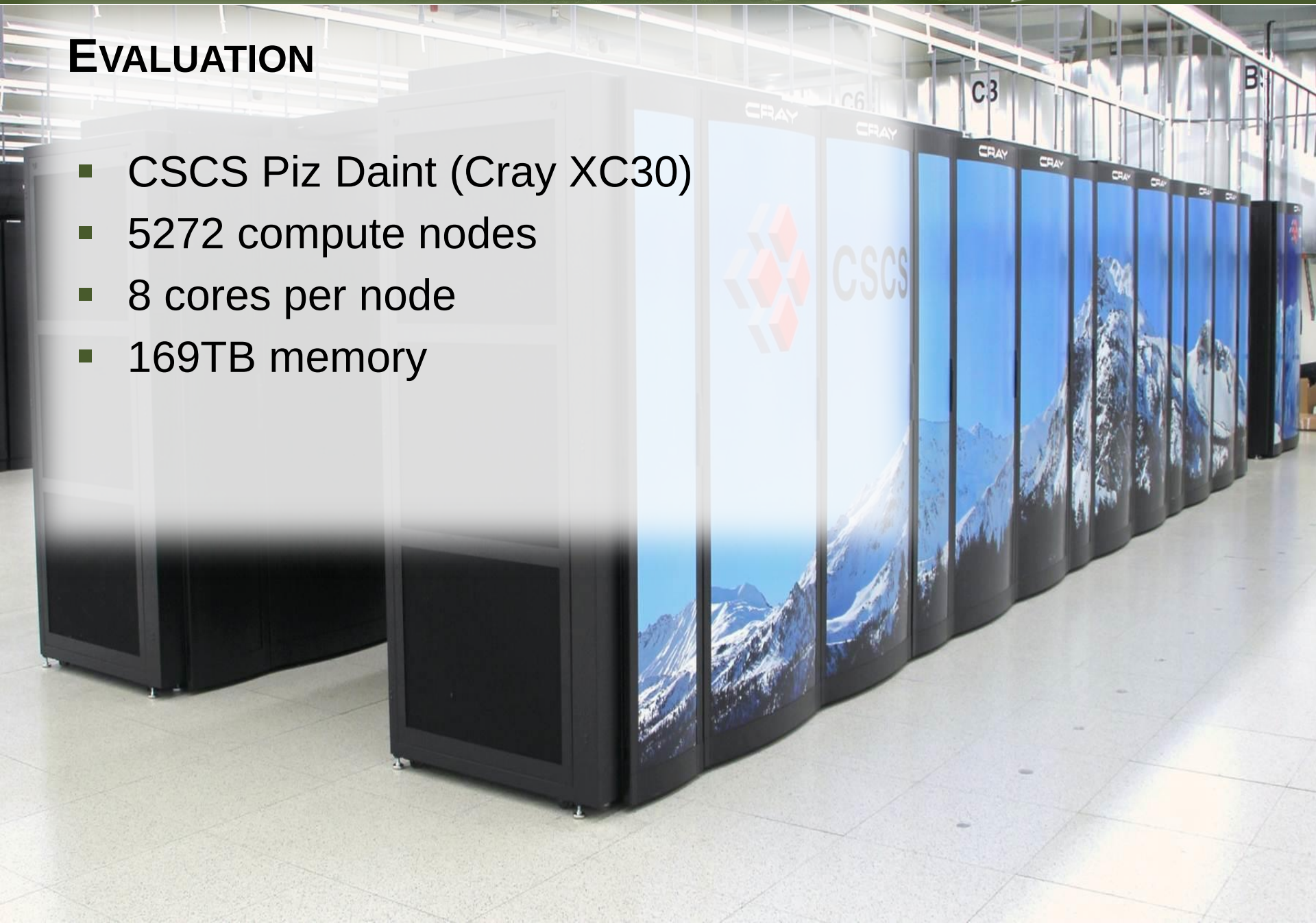


EVALUATION



- CSCS Piz Daint (Cray XC30)
- 5272 compute nodes
- 8 cores per node
- 169TB memory

Evaluation
Considered Benchmarks

Evaluation
Considered Benchmarks

The **latency** benchmark

Evaluation
Considered Benchmarks

The **latency** benchmark

Throughput benchmarks:

- Empty-critical-section
- Single-operation
- Wait-after-release
- Workload-critical-section

Evaluation
Considered Benchmarks

The **latency** benchmark

Throughput benchmarks:

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- Wait-after-release
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DHT

Distributed hashtable evaluation

EVALUATION

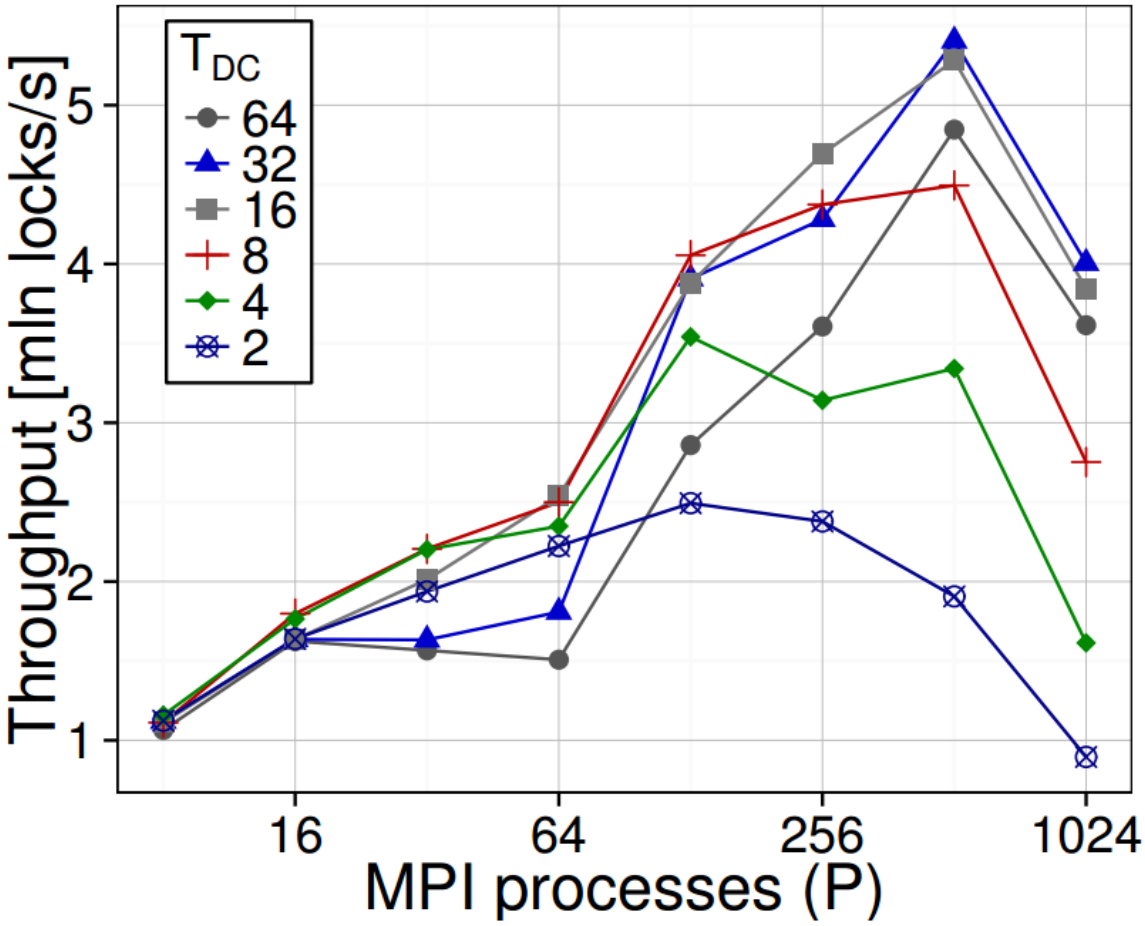
DISTRIBUTED COUNTER ANALYSIS

0|9|7 0|3|1

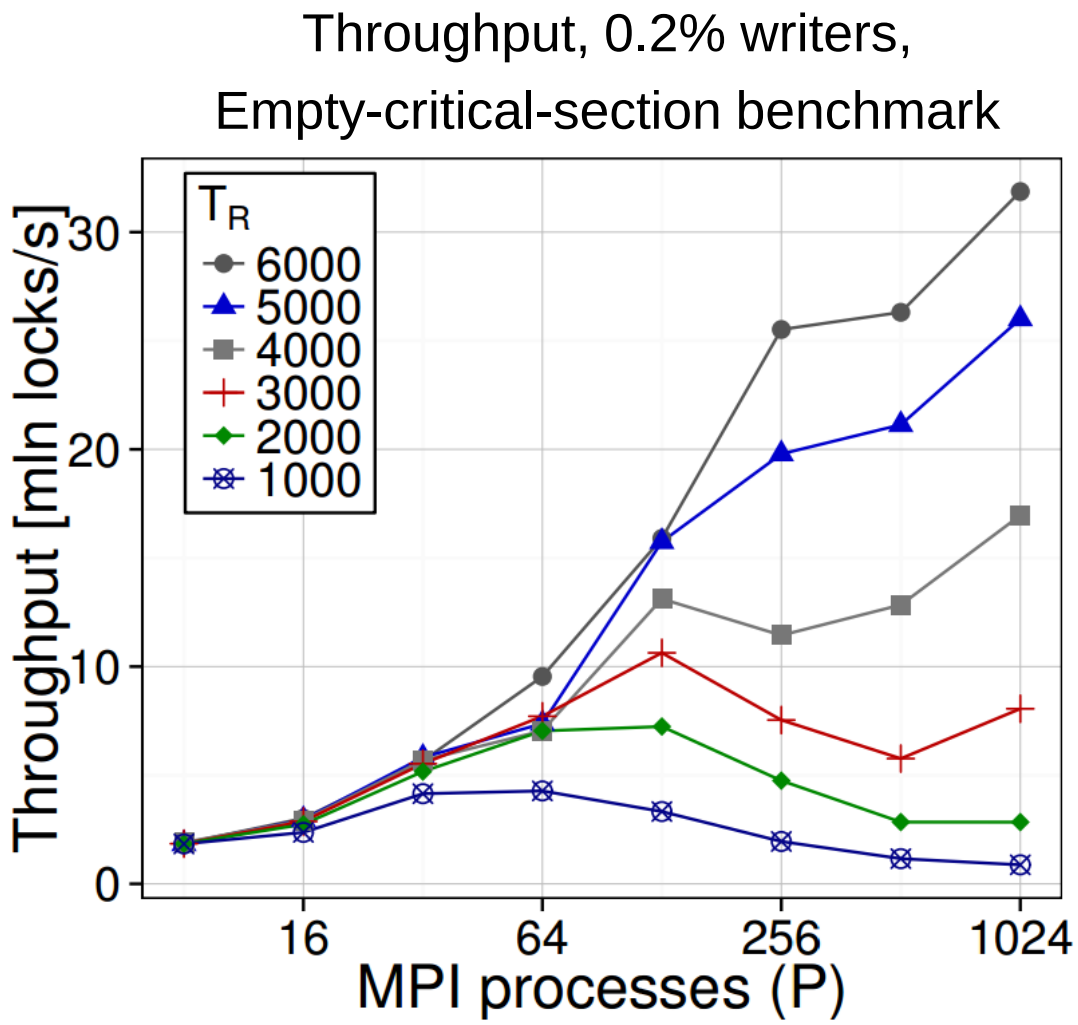
0|12|8

Throughput, 2% writers

Single-operation benchmark

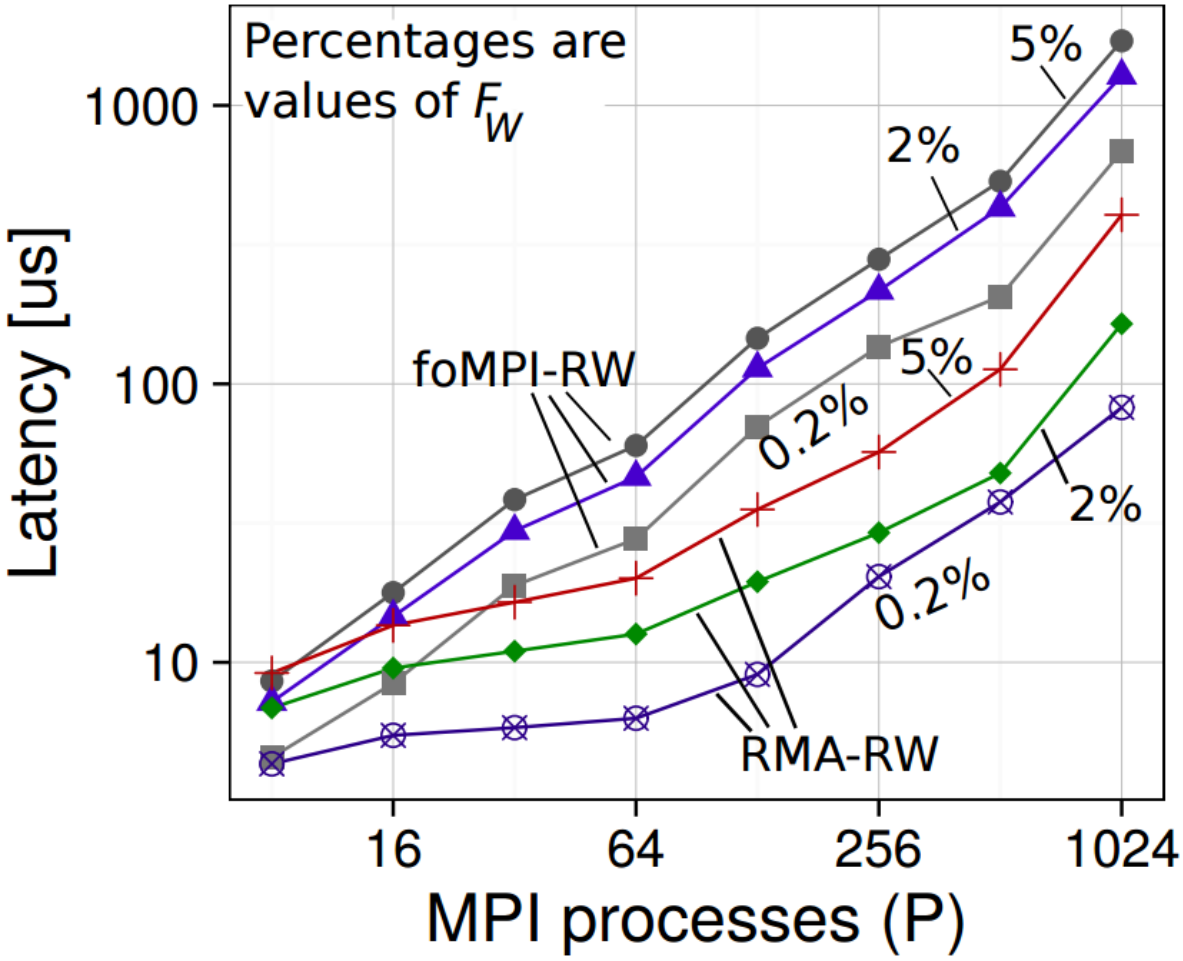


EVALUATION
READER THRESHOLD ANALYSIS



EVALUATION

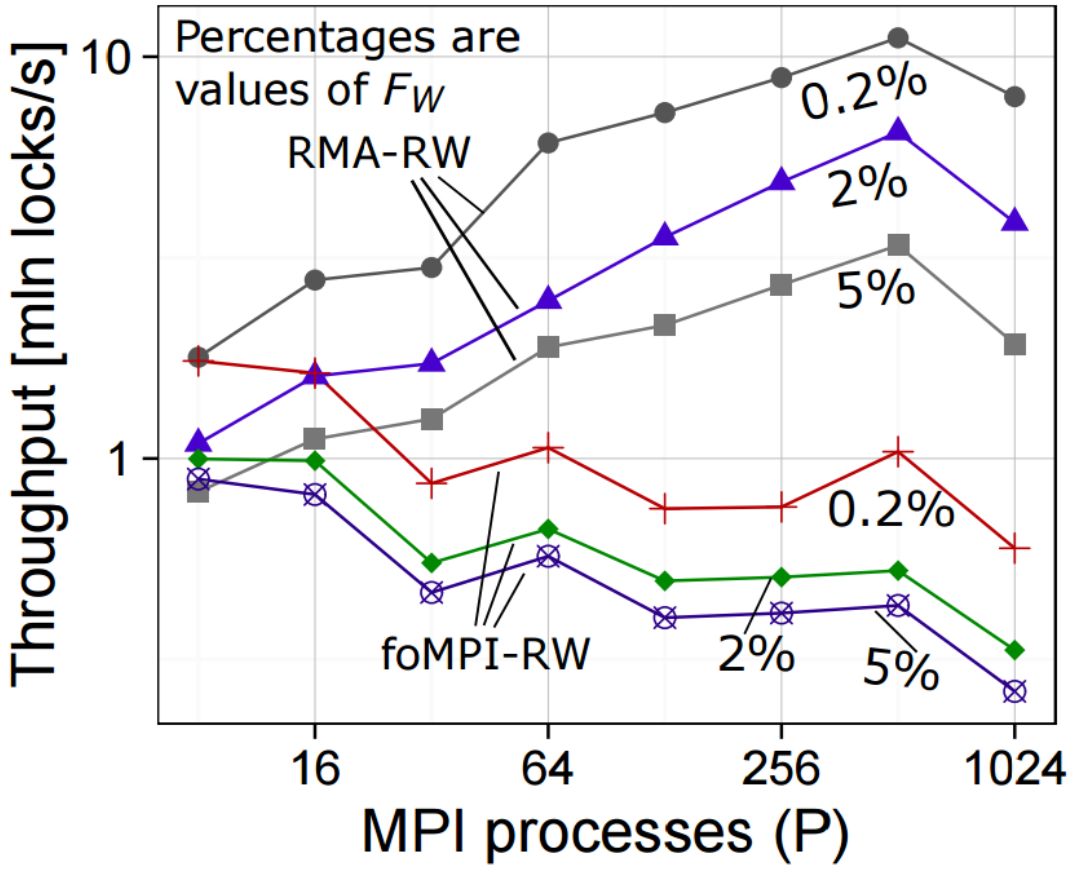
COMPARISON TO THE STATE-OF-THE-ART



[1] R. Gerstenberger et al. Enabling Highly-scalable Remote Memory Access Programming with MPI-3 One Sided. ACM/IEEE Supercomputing 2013.

EVALUATION
COMPARISON TO THE STATE-OF-THE-ART

Throughput, single-operation benchmark



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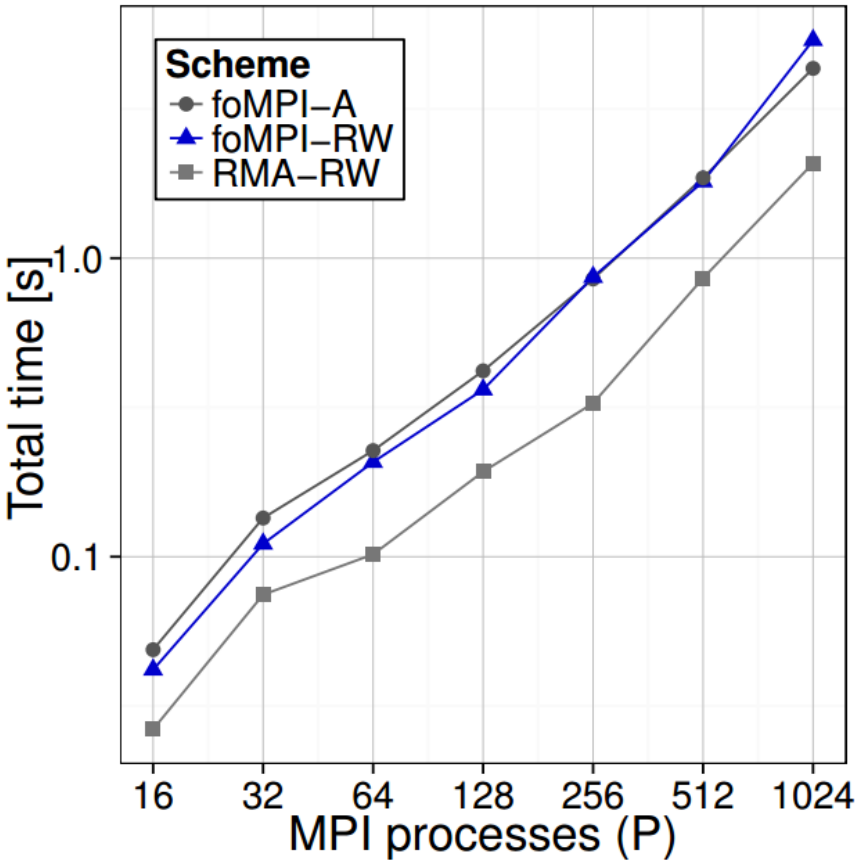
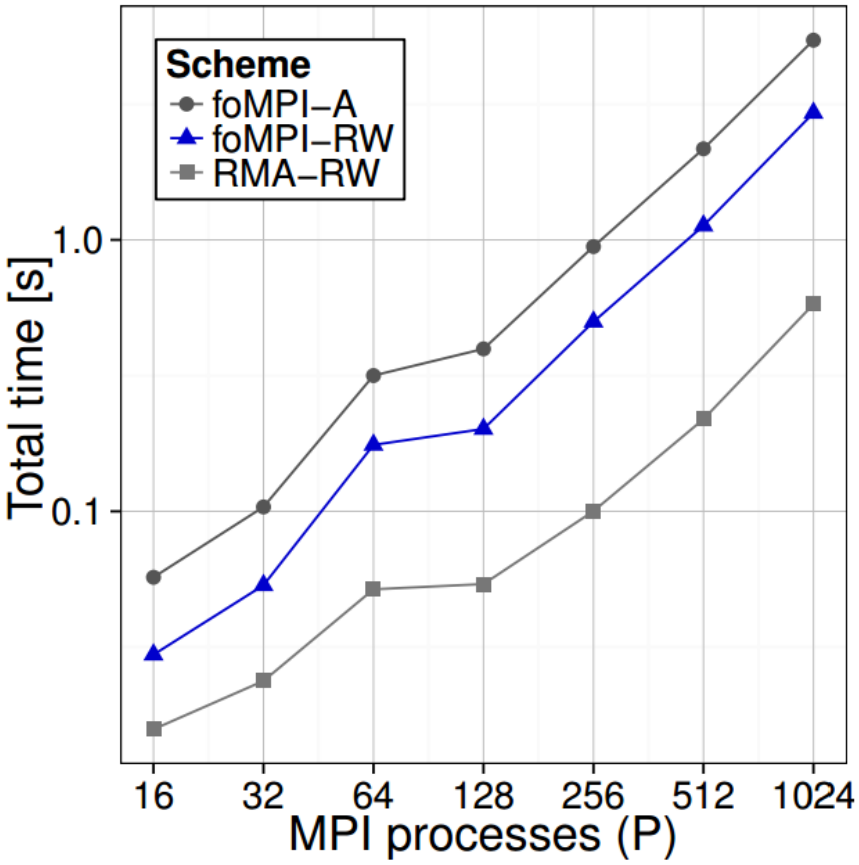
EVALUATION
DISTRIBUTED HASHTABLE

20% writers



10% writers



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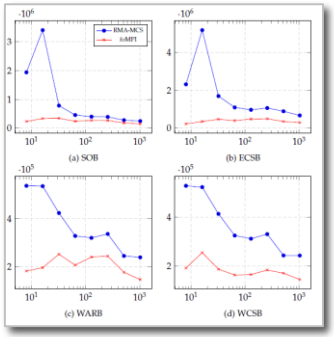
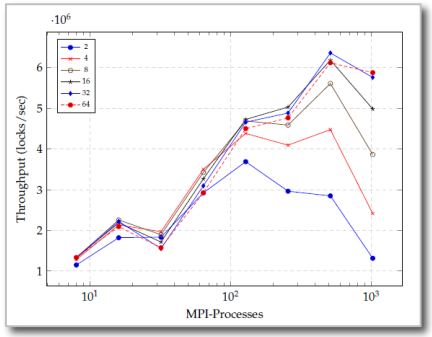
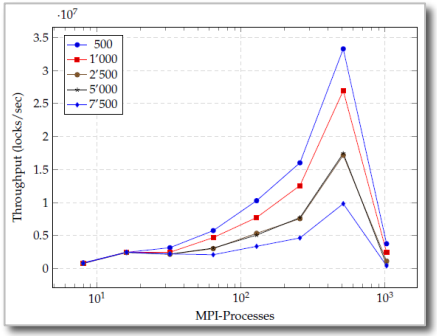
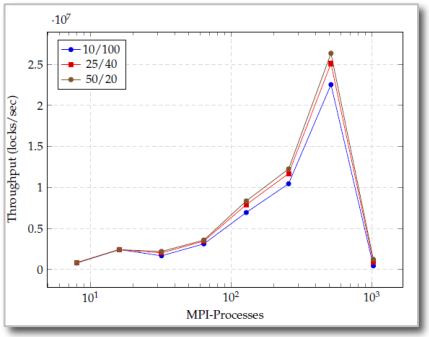
Other Analyses

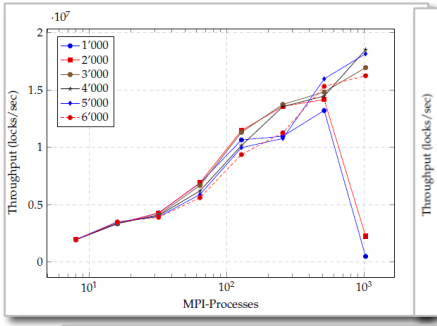
OTHER ANALYSES

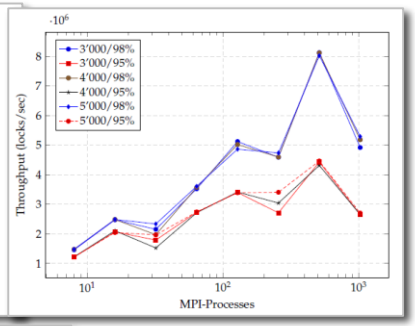


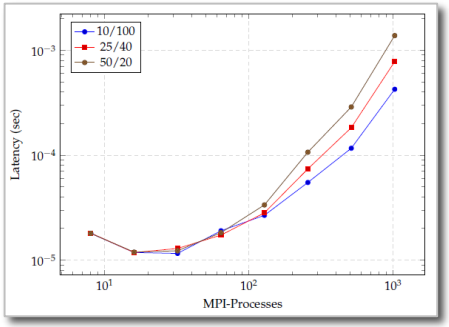


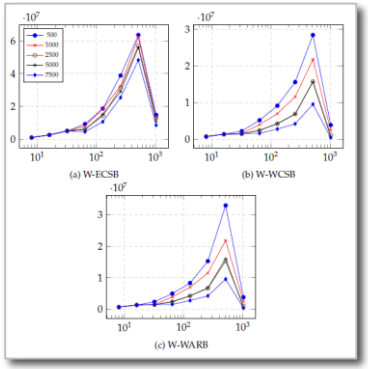


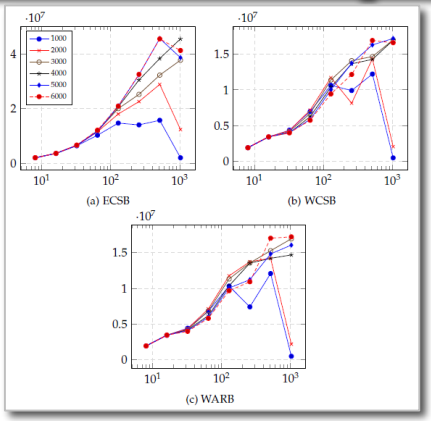


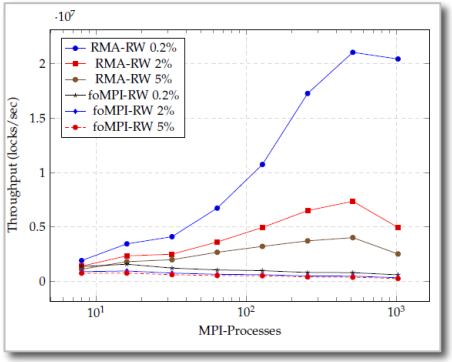


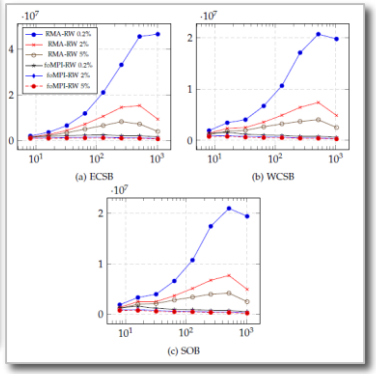


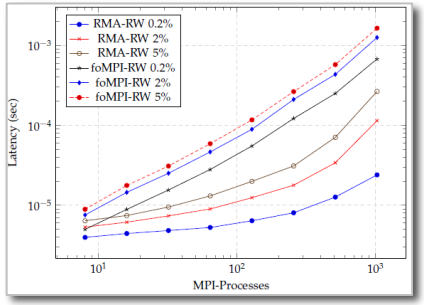












CONCLUSIONS

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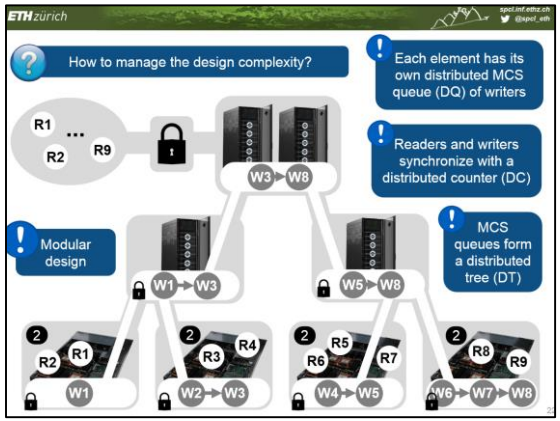
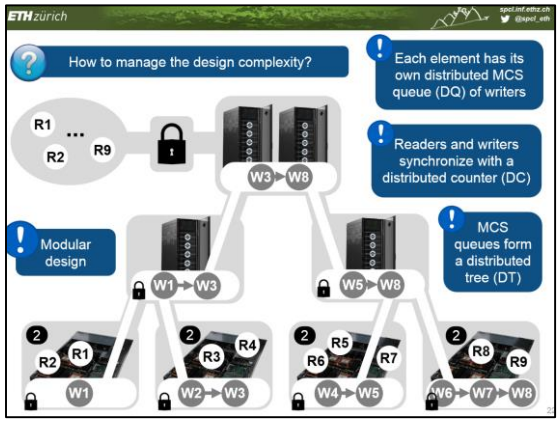


Modular distributed RMA lock, correctness with SPIN

CONCLUSIONS



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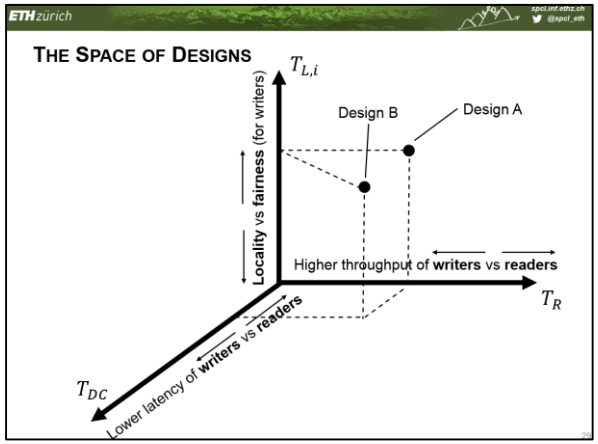
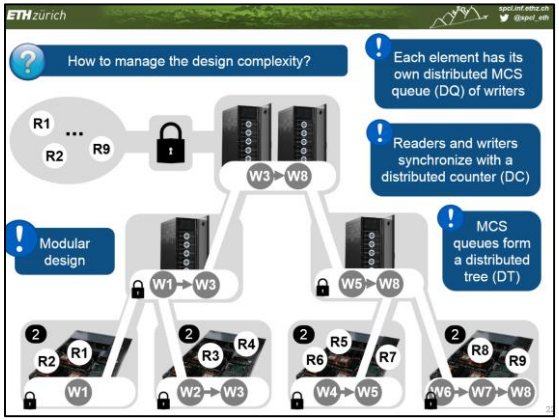


Parameter-based design, feasible with various RMA libs/languages

CONCLUSIONS



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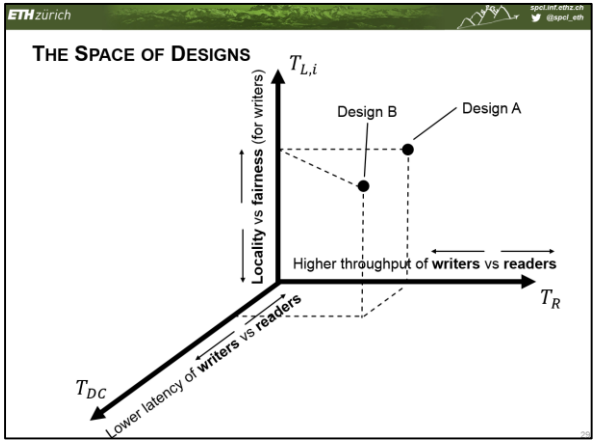

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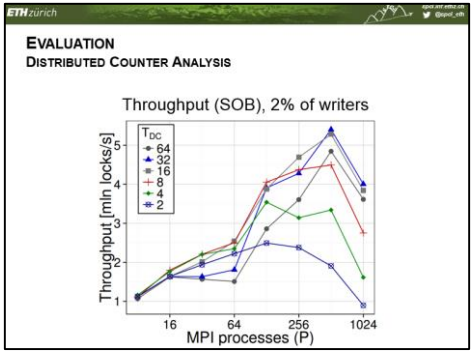
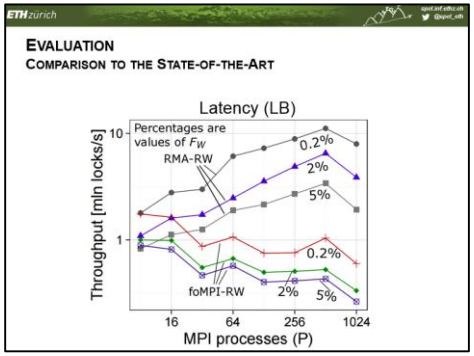
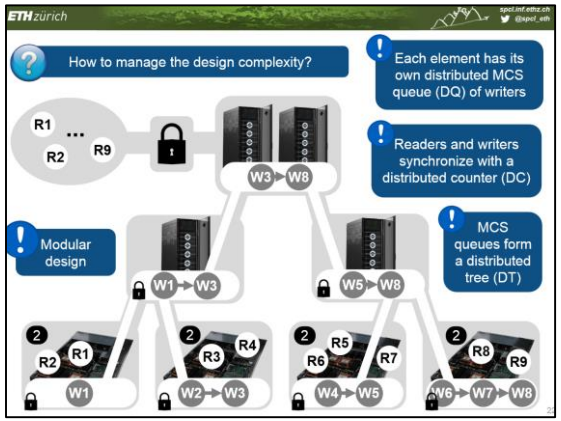




Improves latency and throughput over state-of-the-art

CONCLUSIONS



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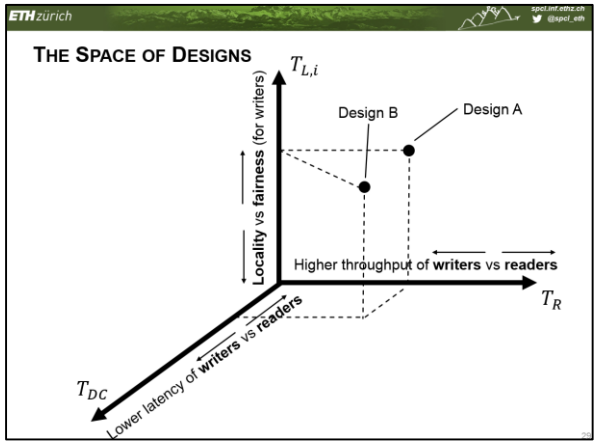

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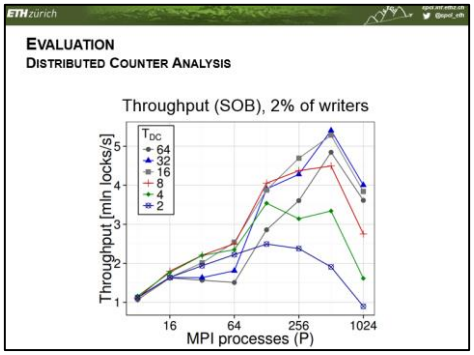

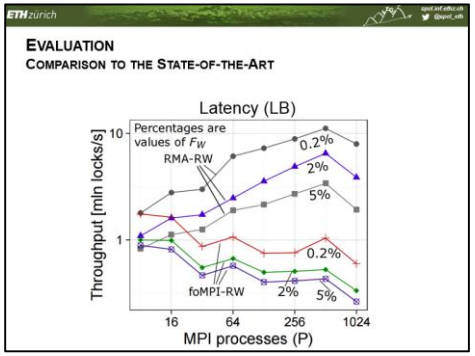

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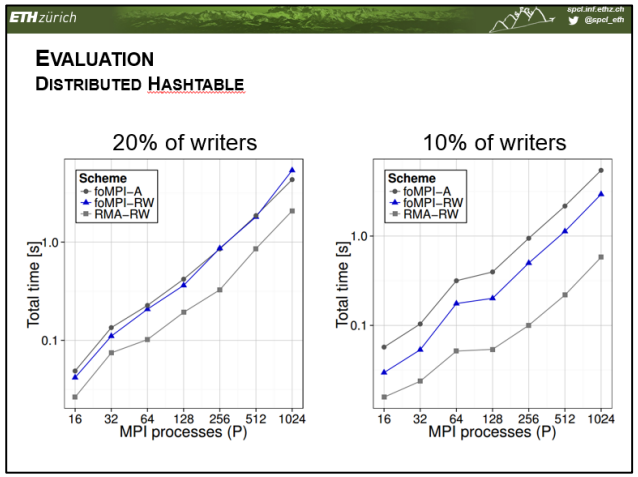
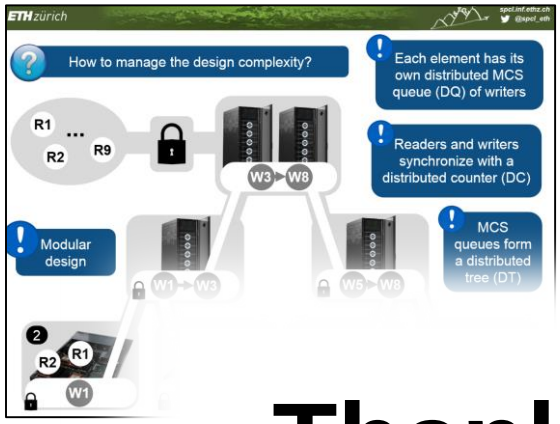
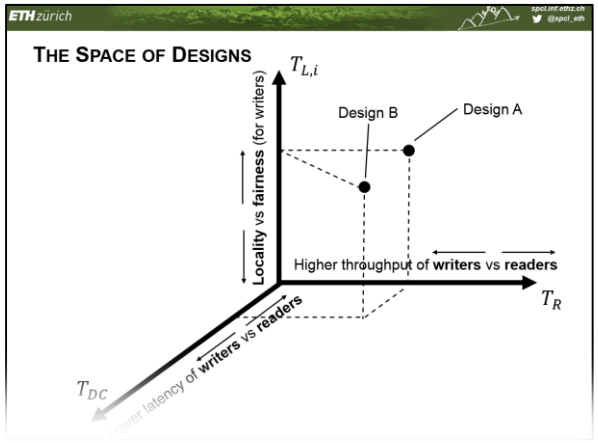


Enables high-performance distributed hashtabled

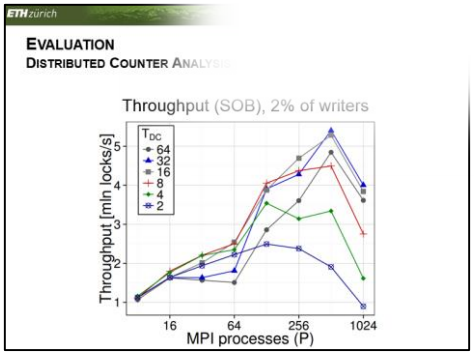
CONCLUSIONS



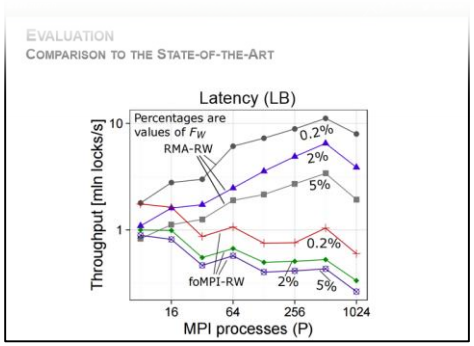


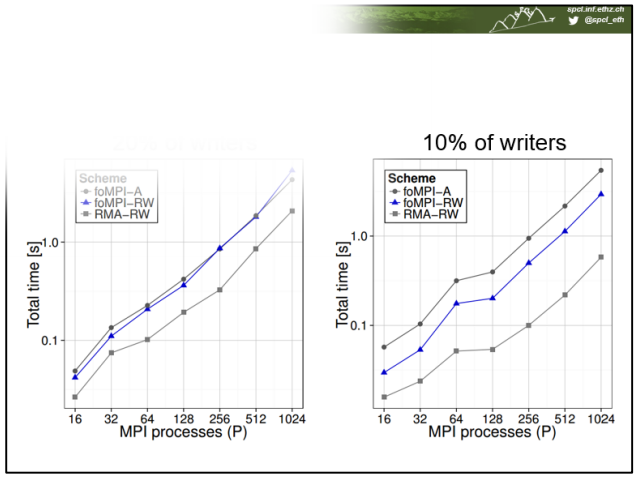
Modular d… corre… …ible …es

Thank you for your attention



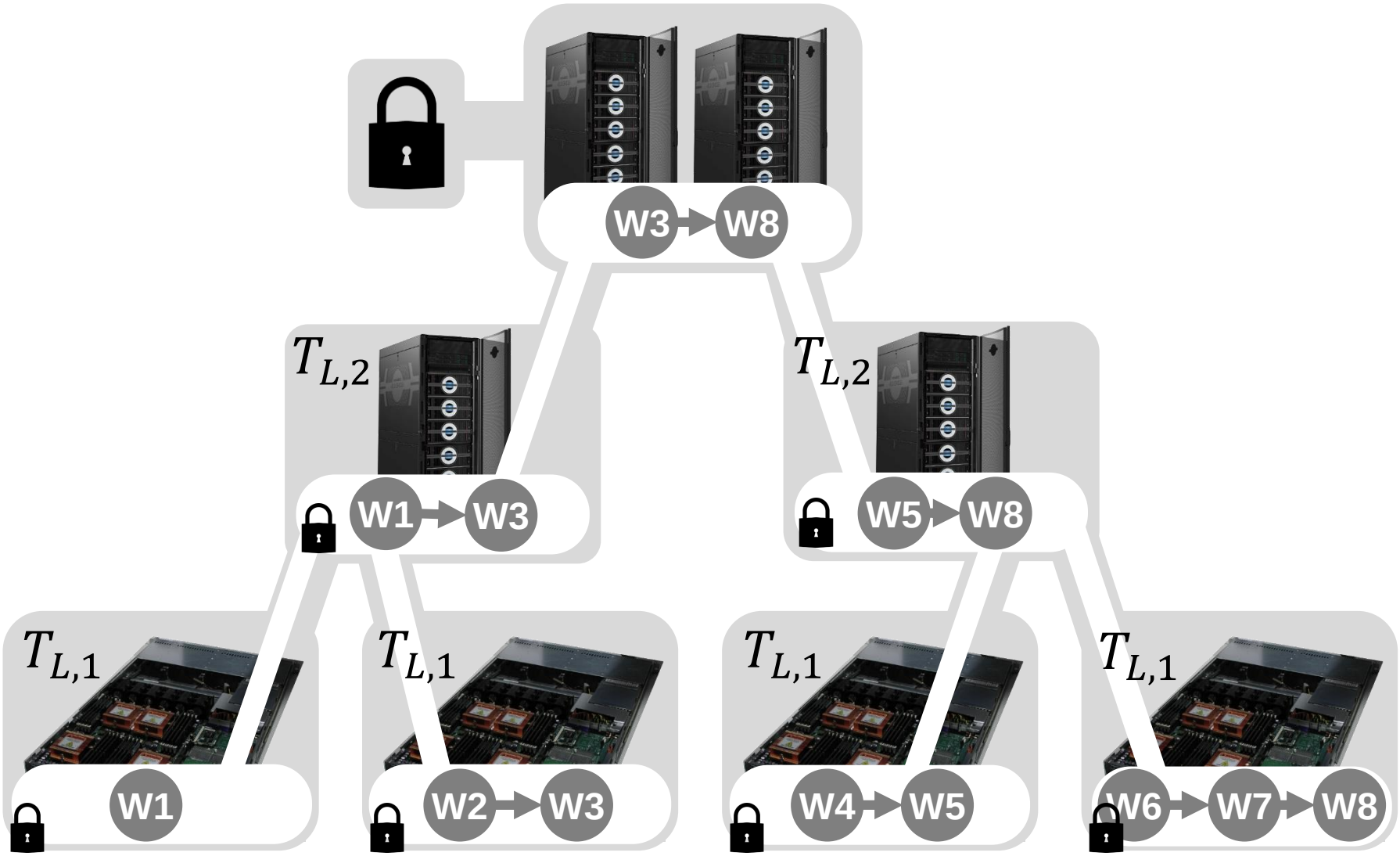
Improves latency and throughput over state-of-the-art





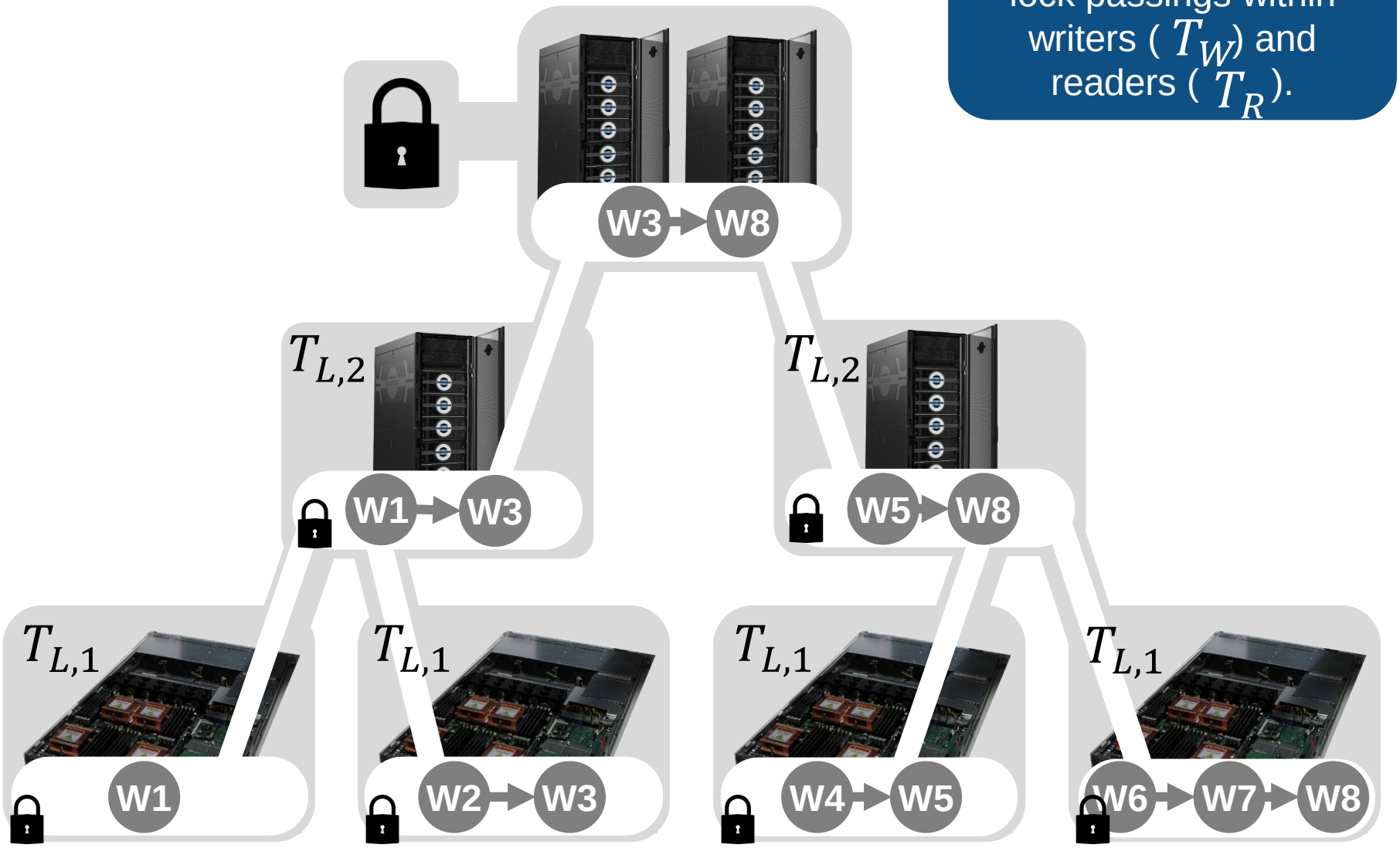
Enables high-performance distributed hashtabled

DISTRIBUTED TREE OF QUEUES (DT)
Throughput of readers vs writers



Distributed Tree of Queues (DT)
Throughput of readers vs writers

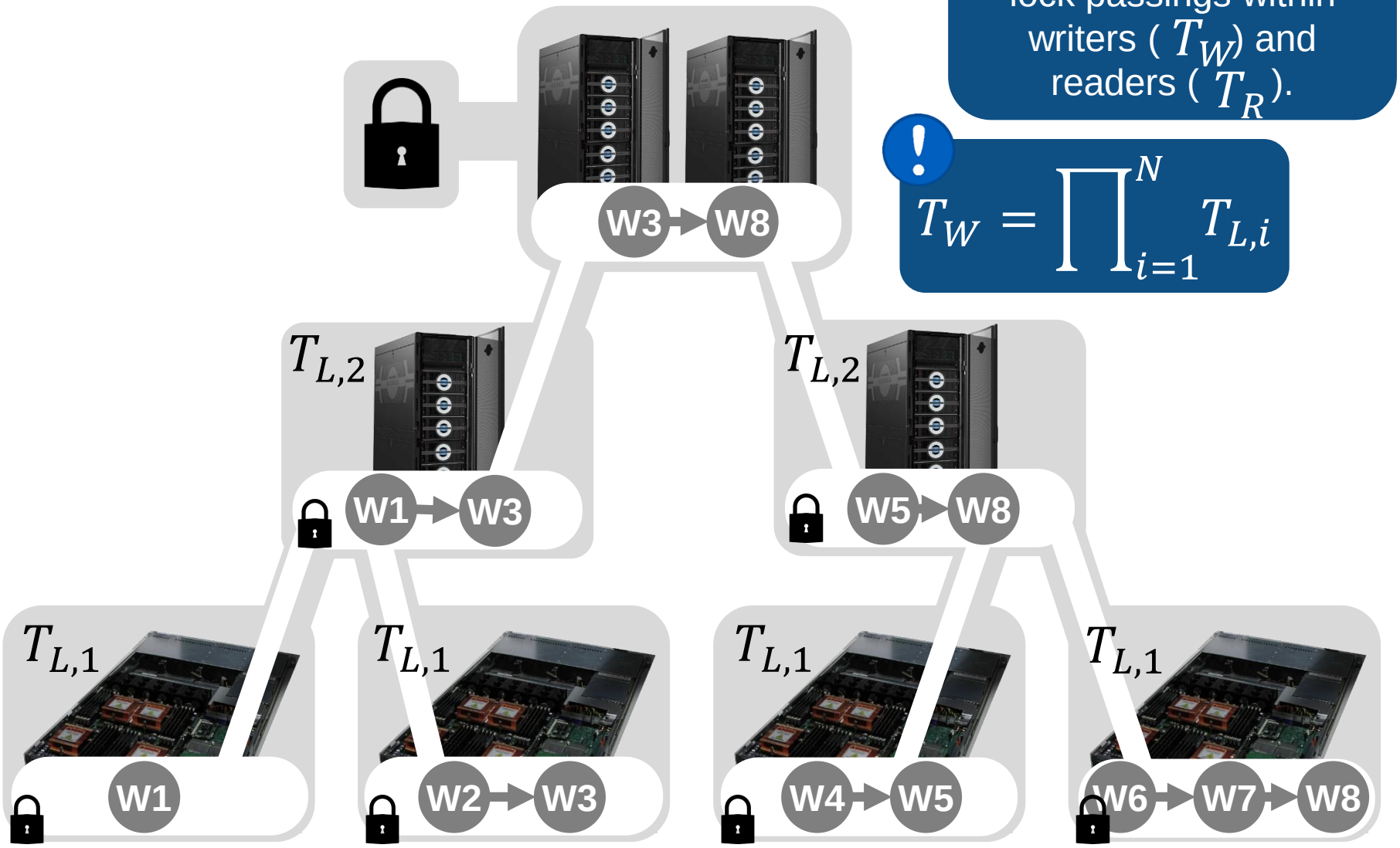
DT: The maximum number of consecutive lock passings within writers (T_W) and readers (T_R).



Distributed Tree of Queues (DT)
Throughput of readers vs writers

DT: The maximum number of consecutive lock passings within writers (T_W) and readers (T_R).

$$T_W = \prod_{i=1}^{N} T_{L,i}$$



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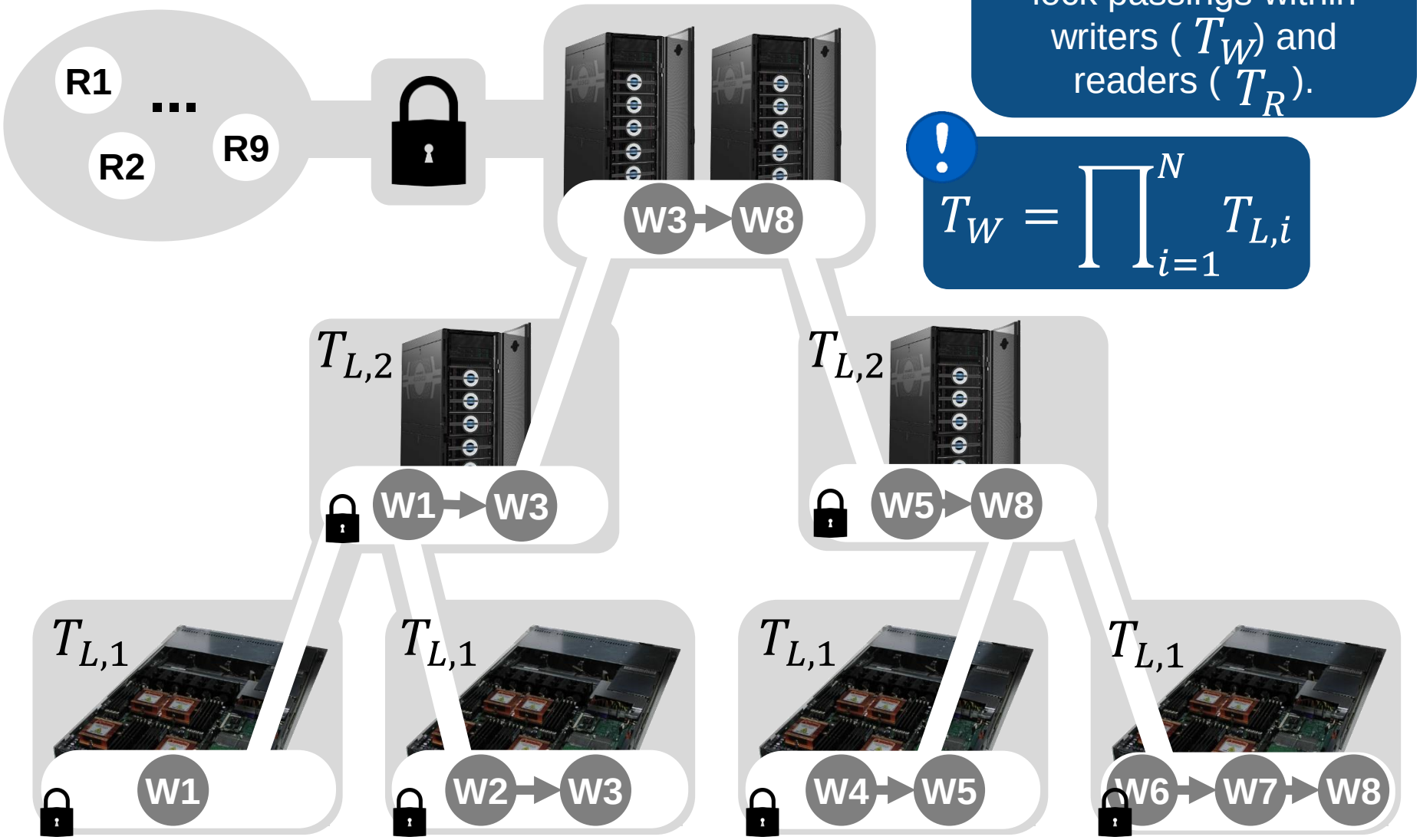
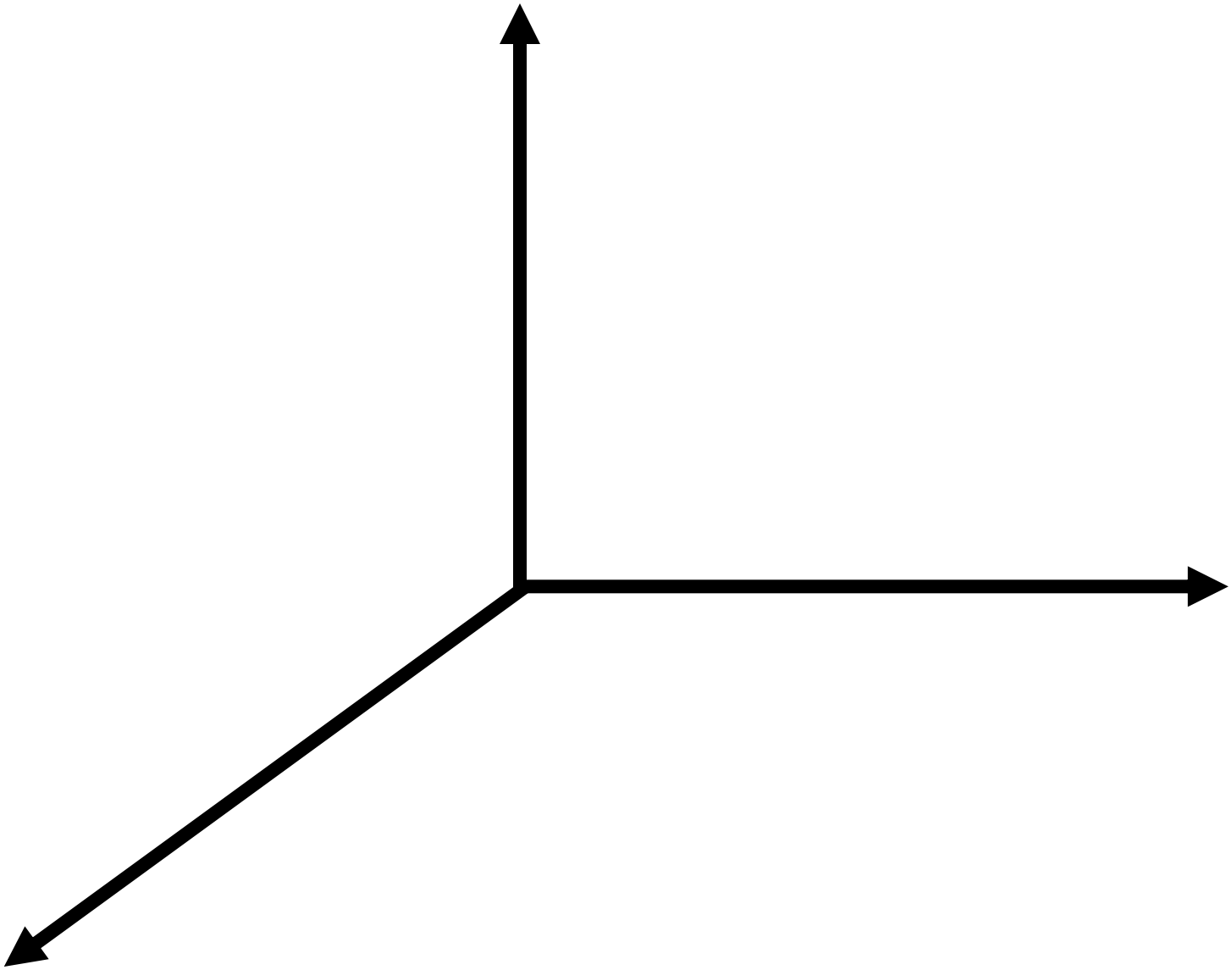
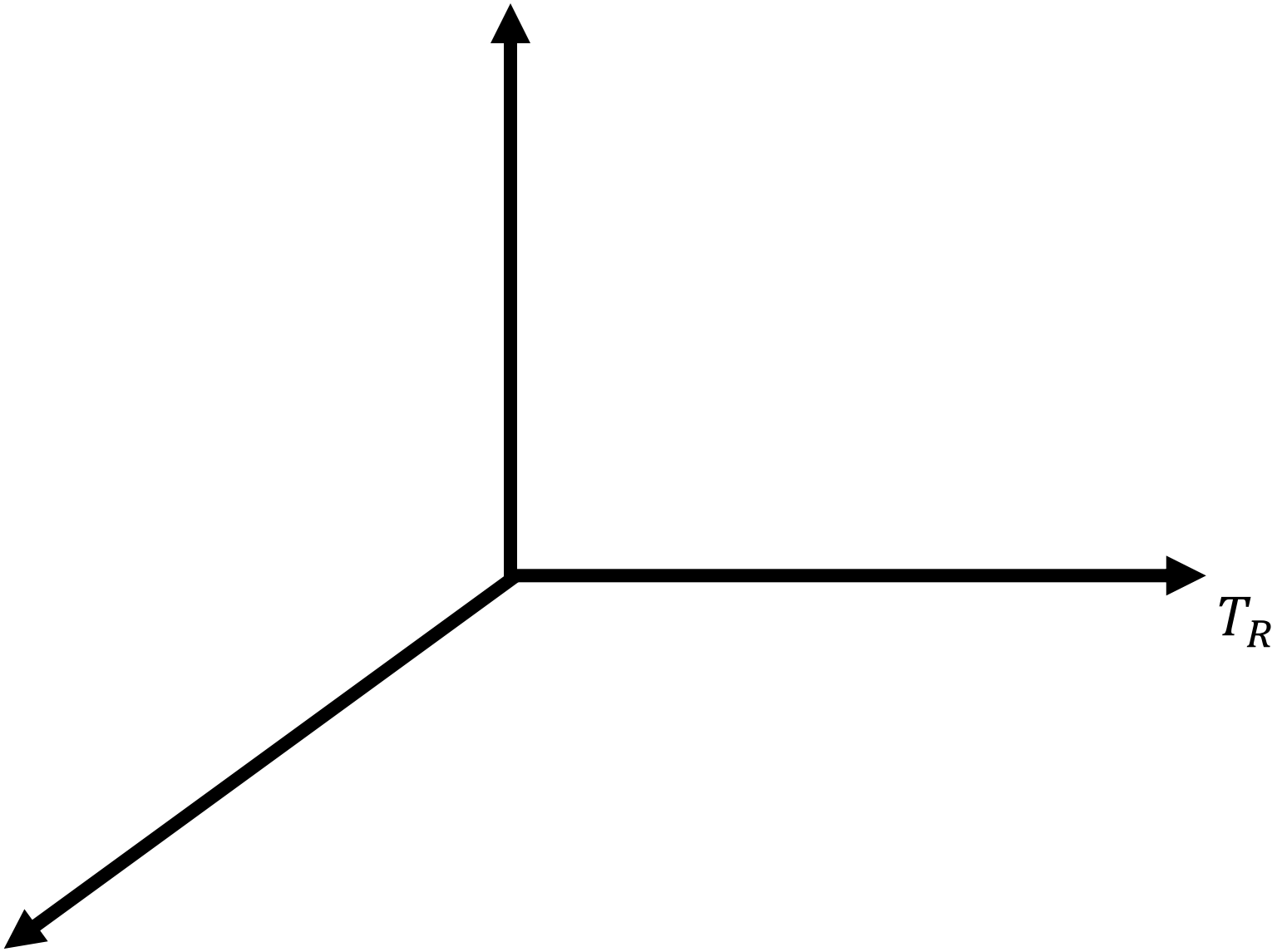


The Space of Designs

The Space of Designs



The Space of Designs



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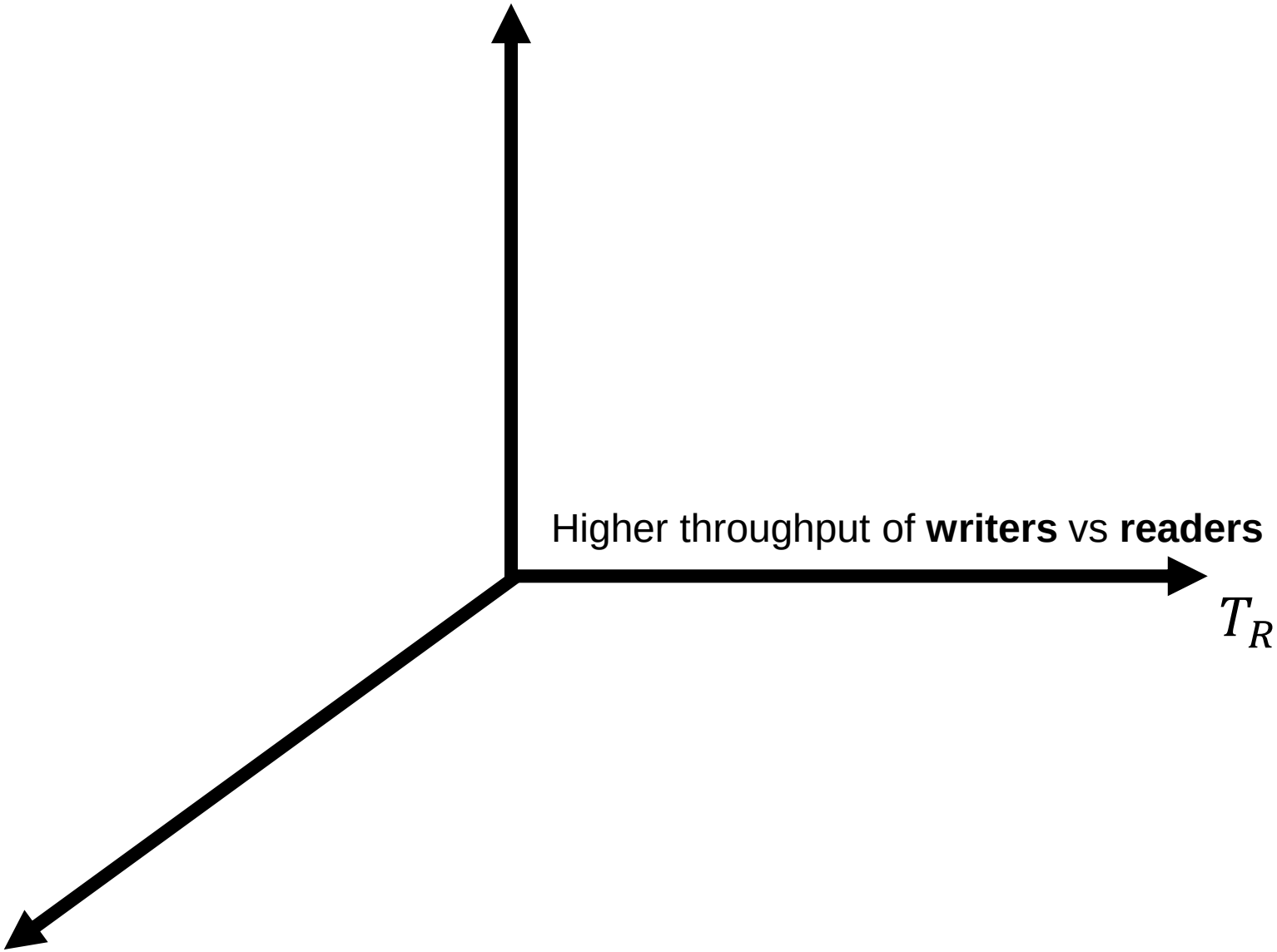

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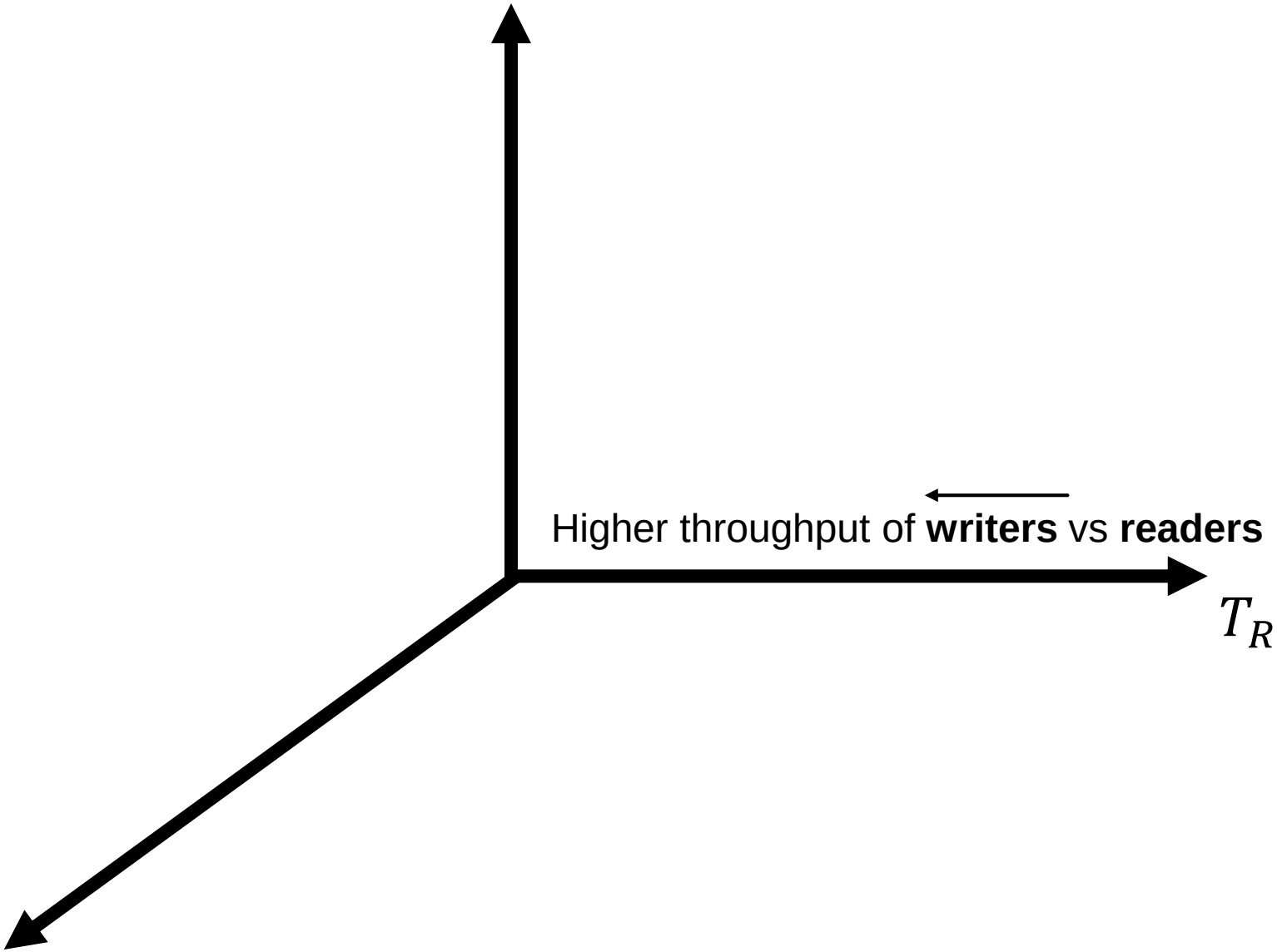

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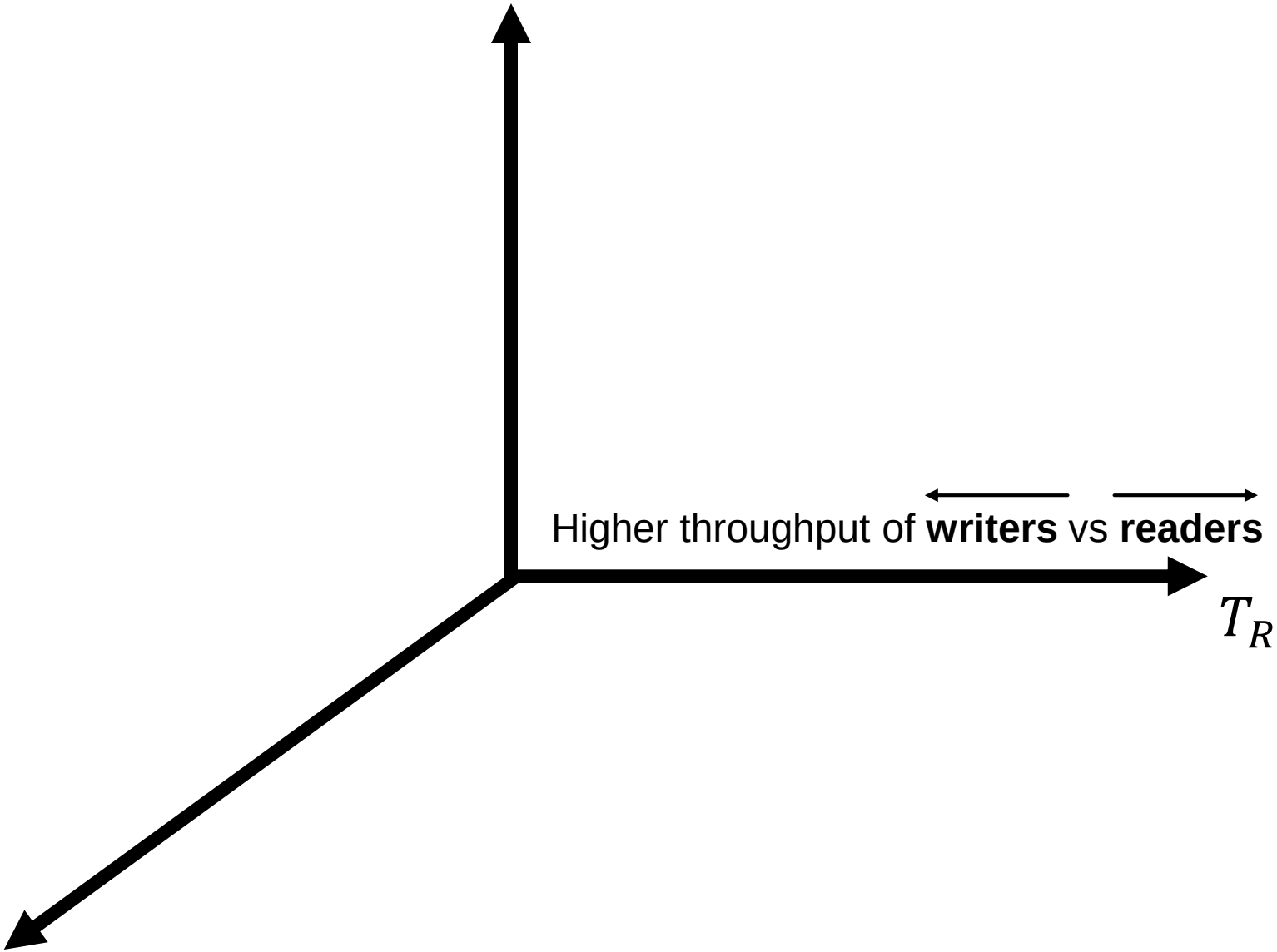

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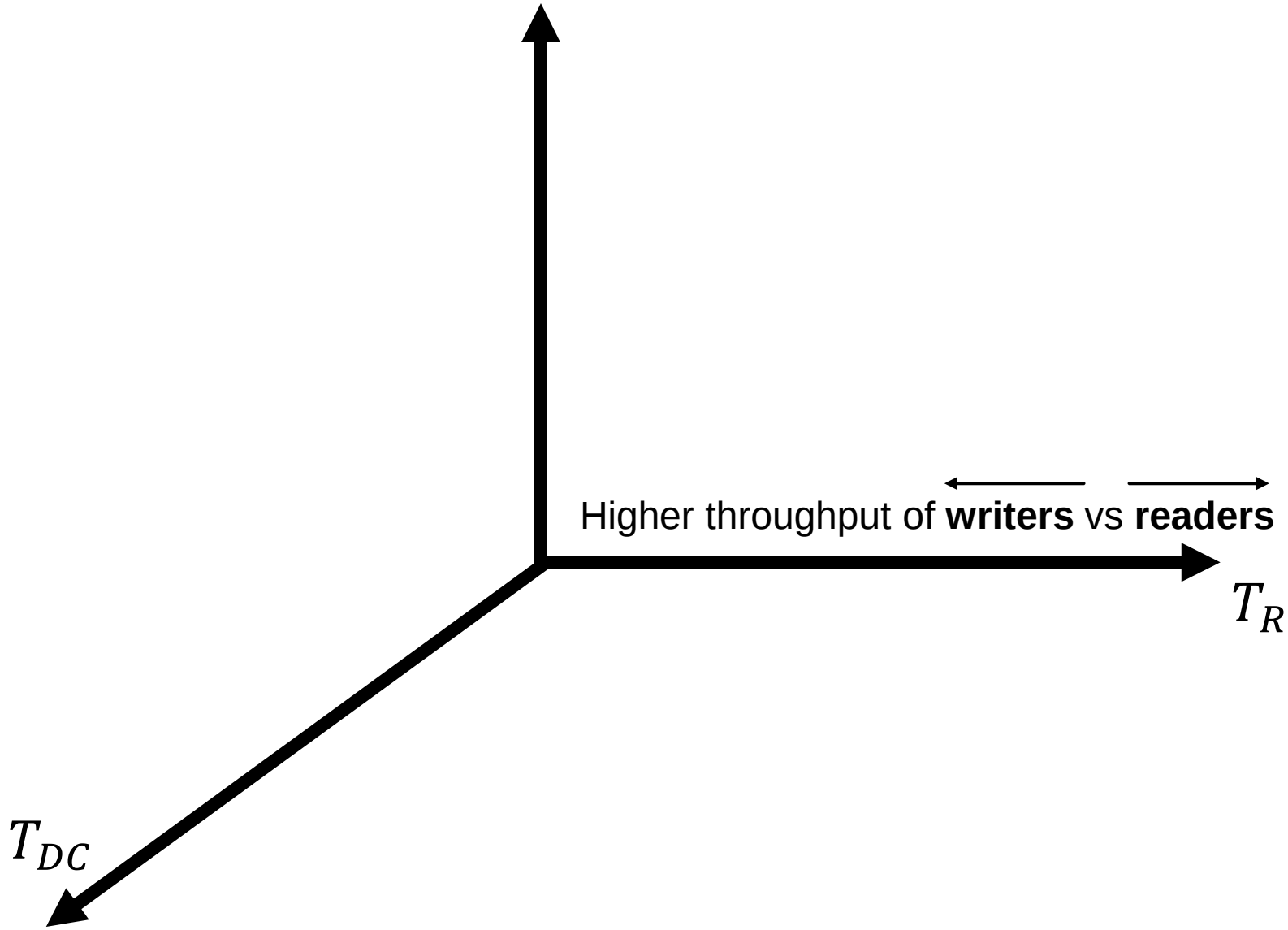

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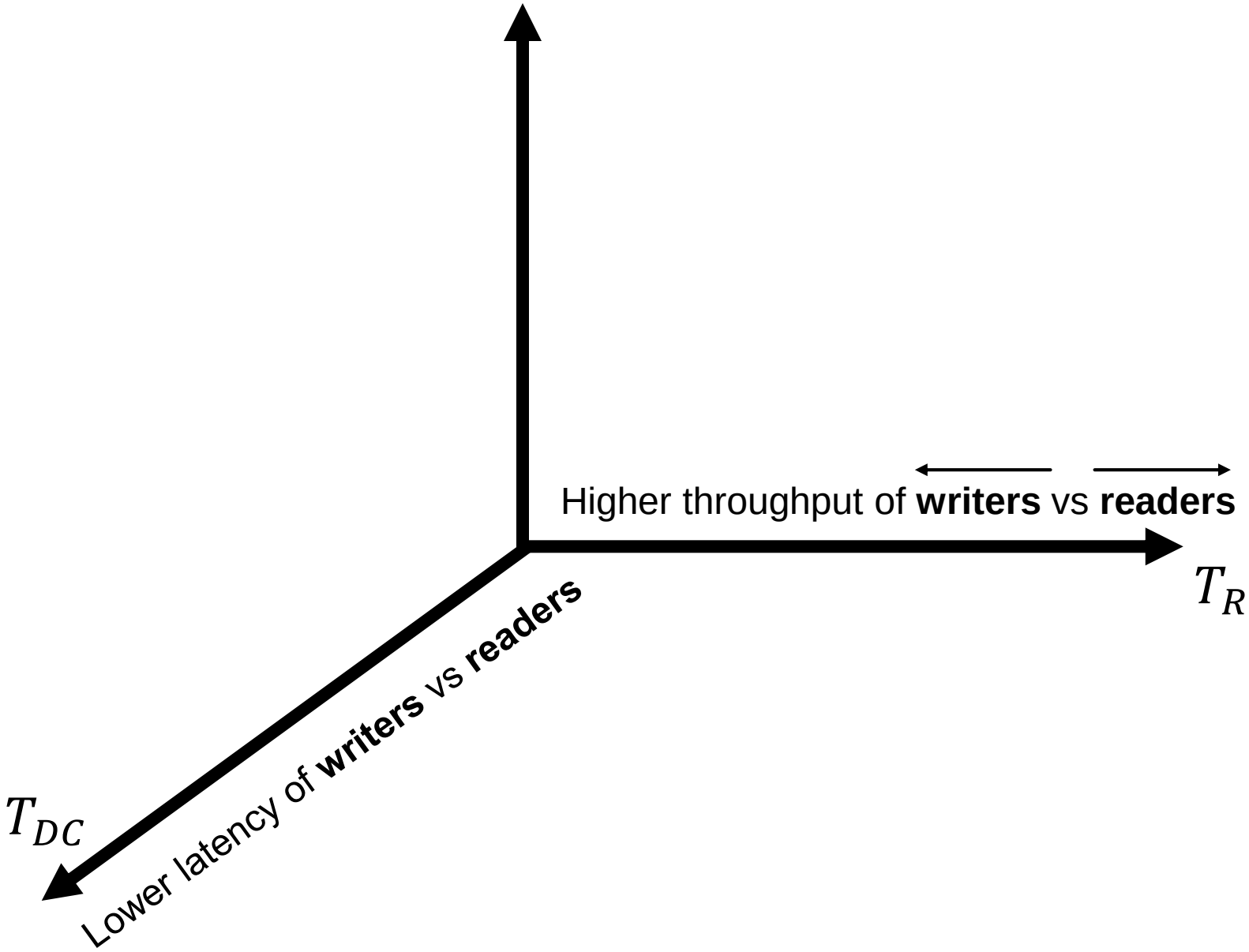

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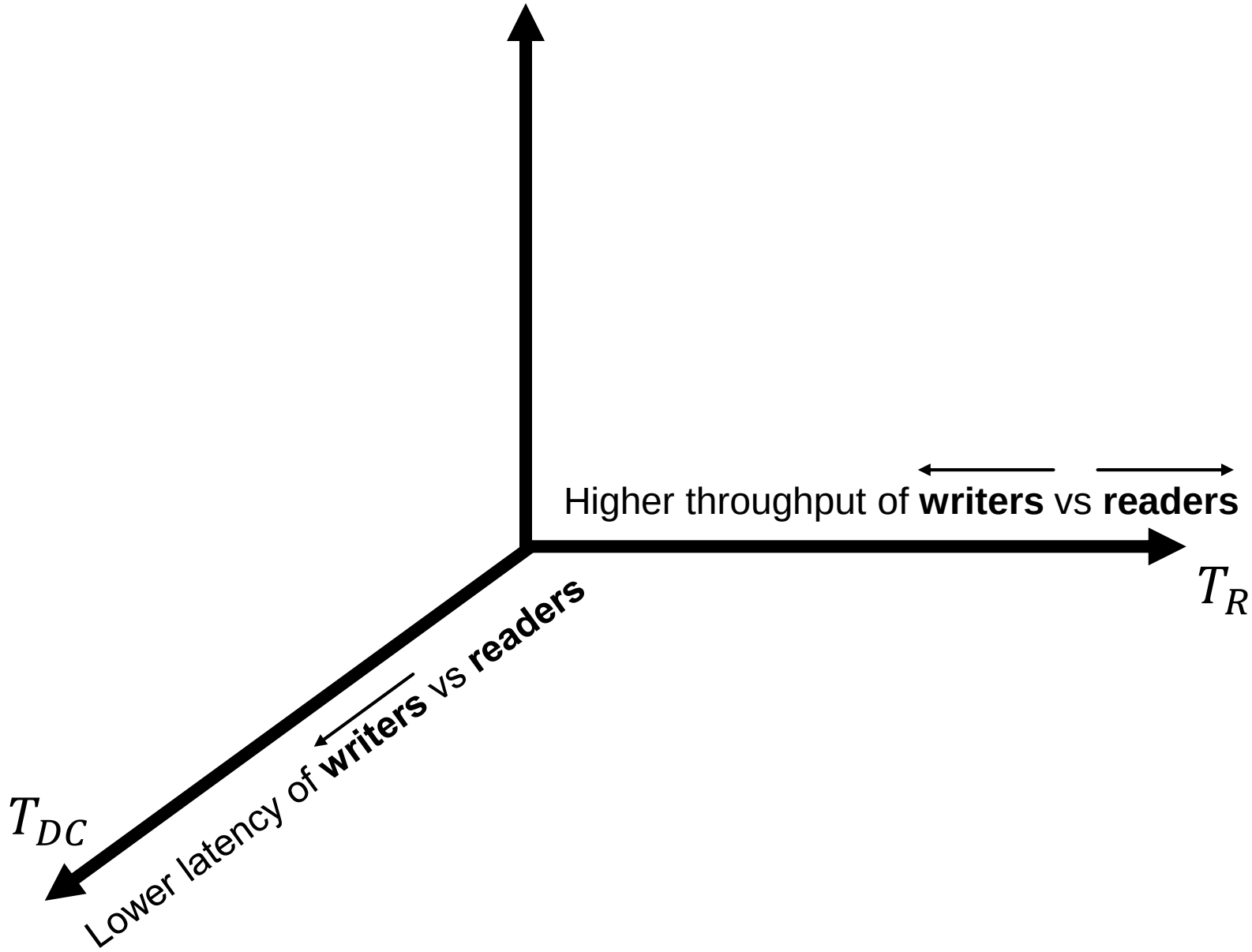

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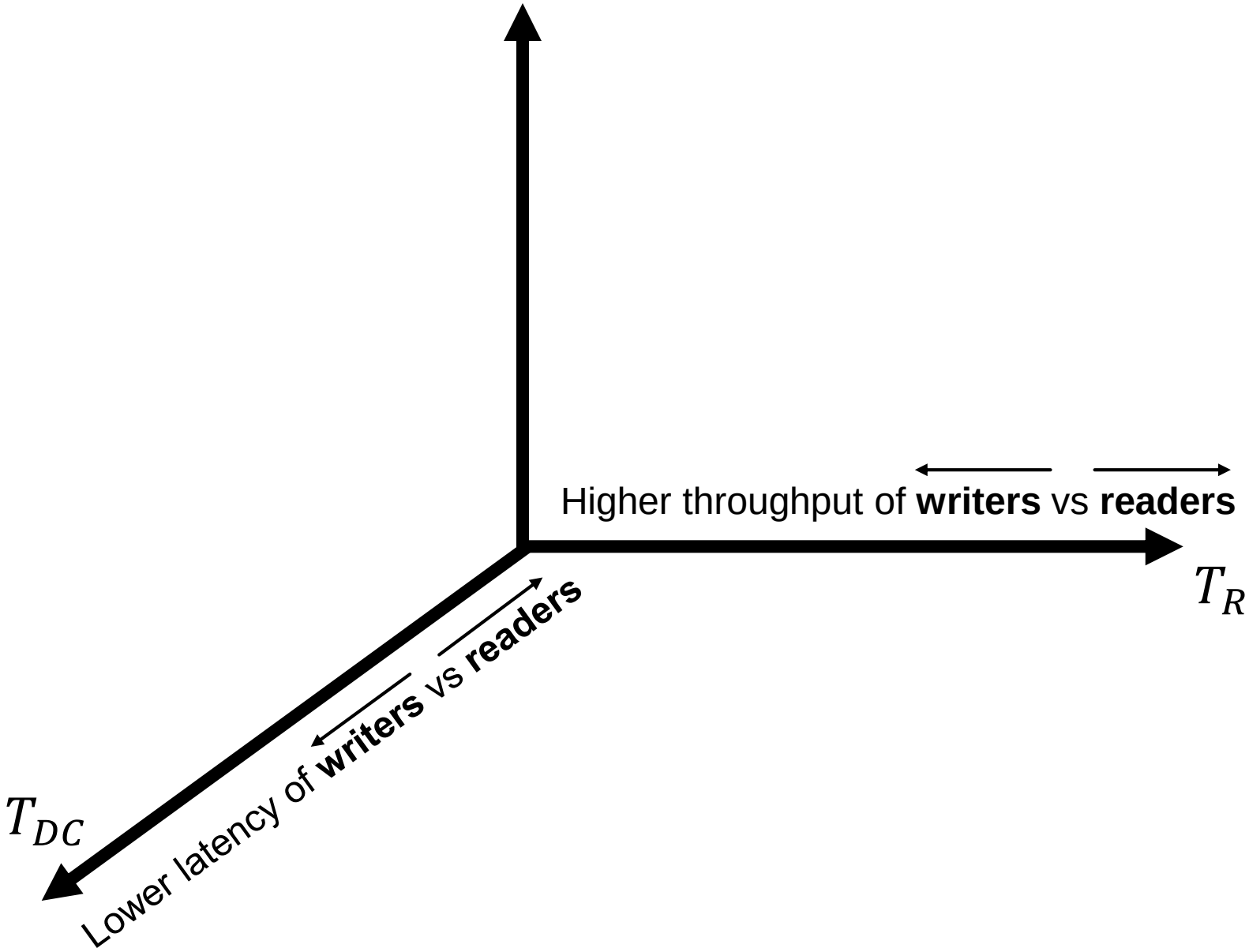

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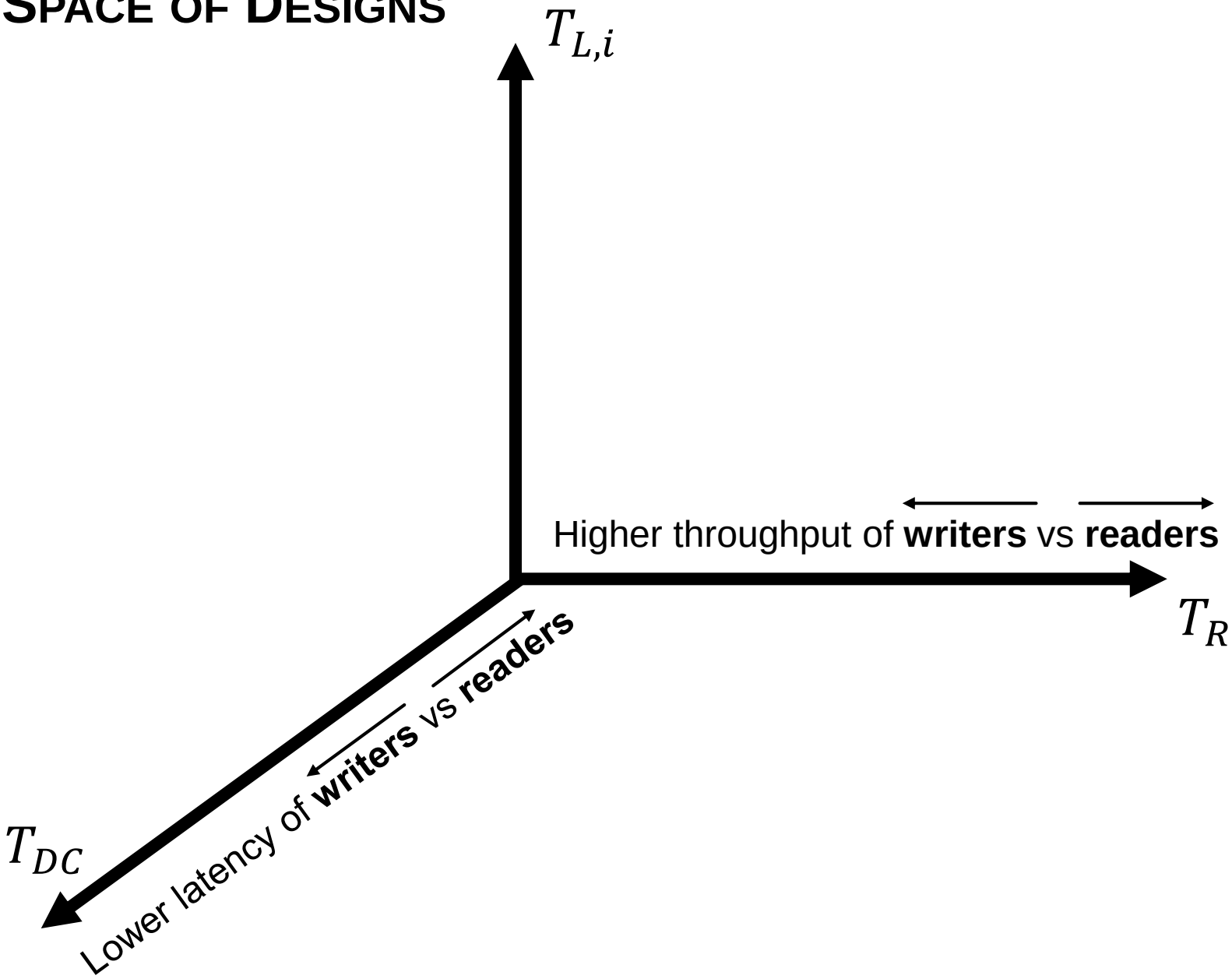

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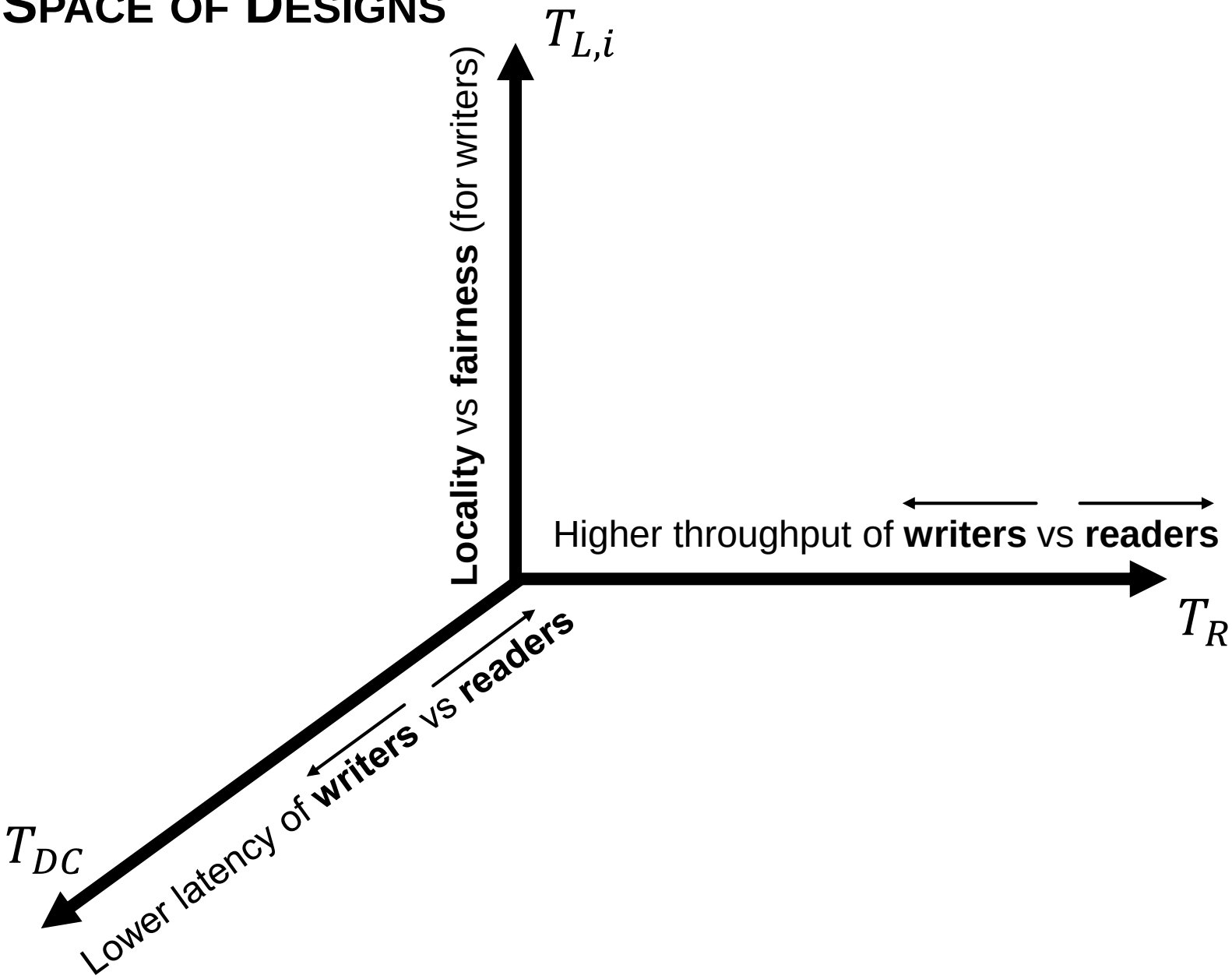

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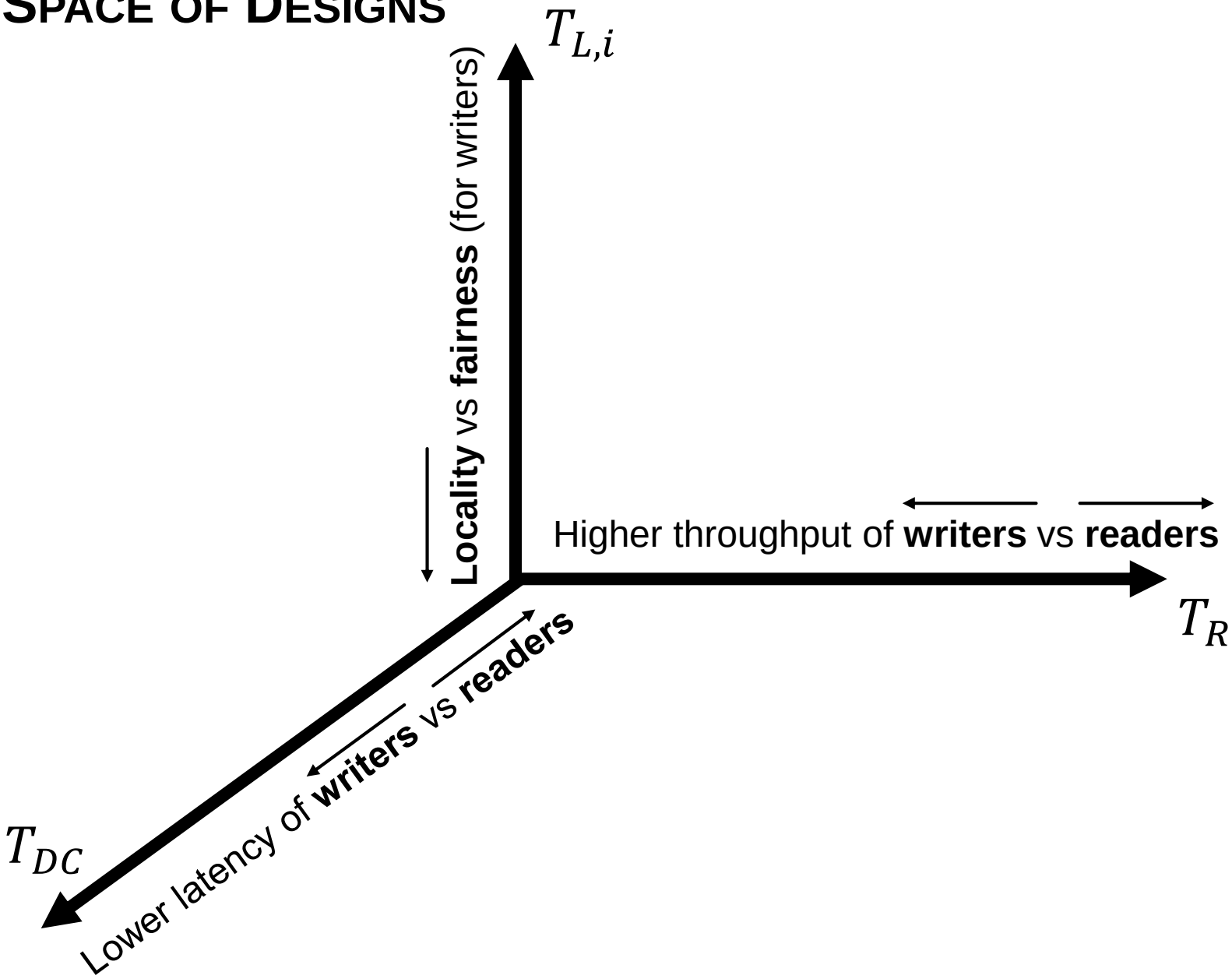

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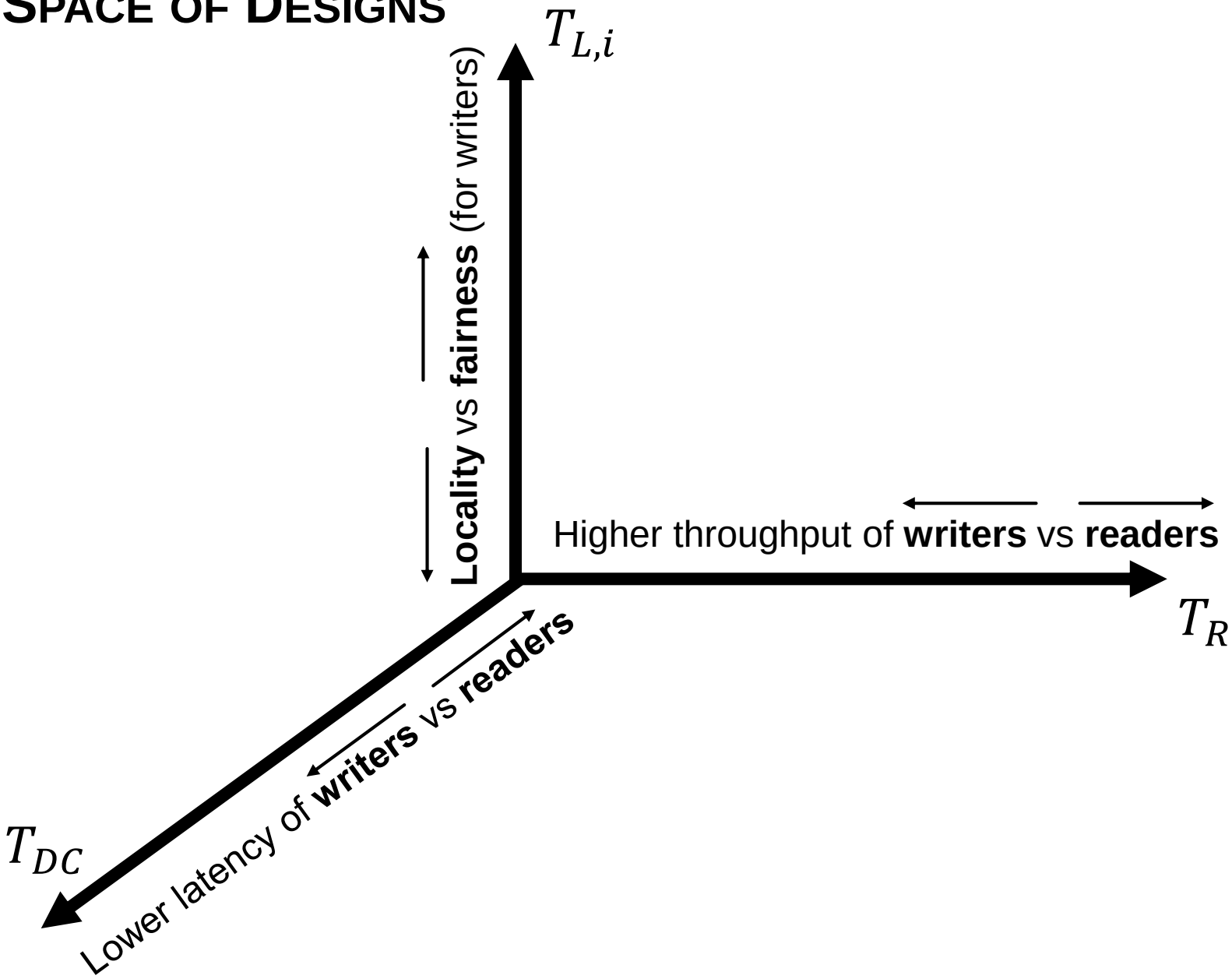
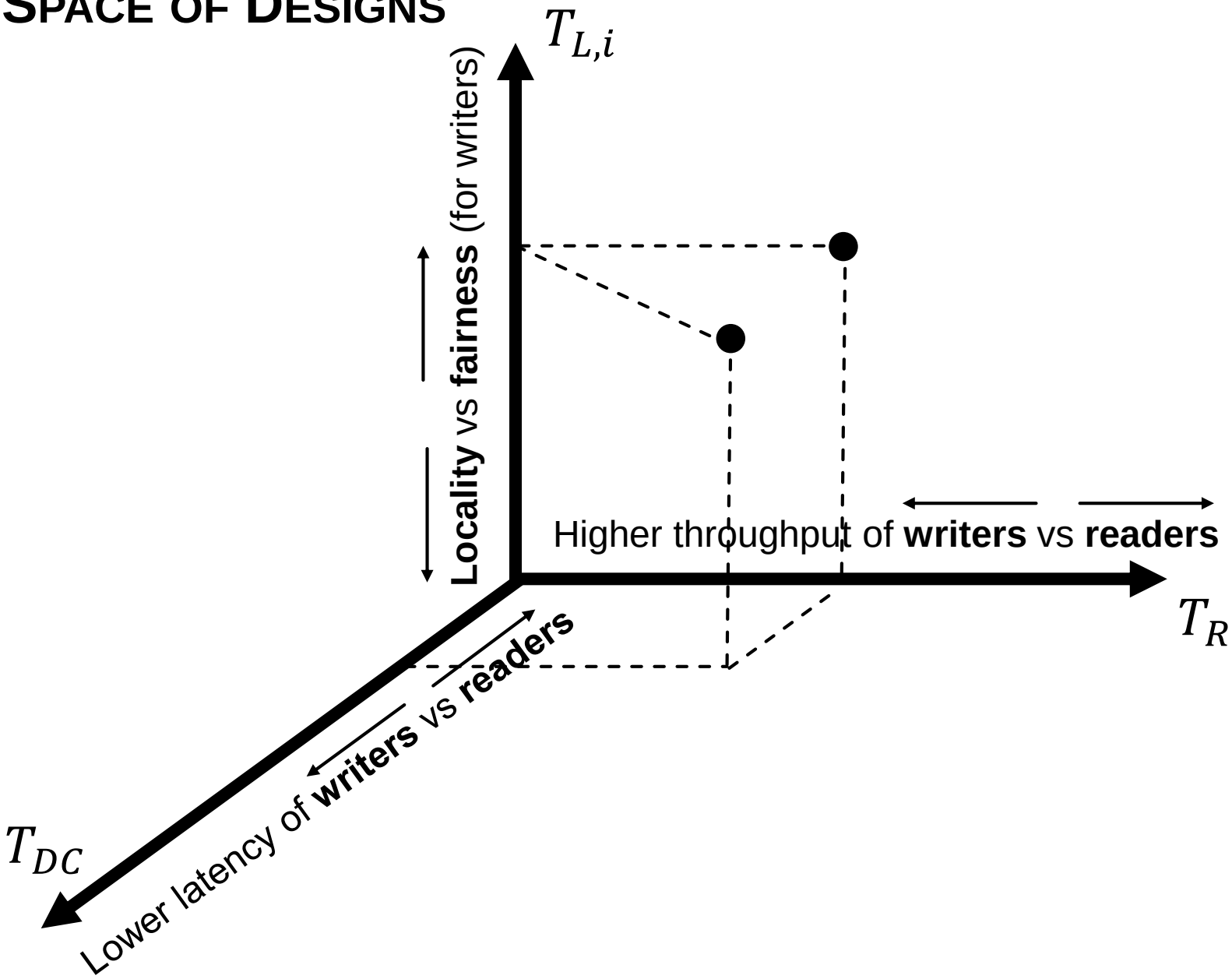
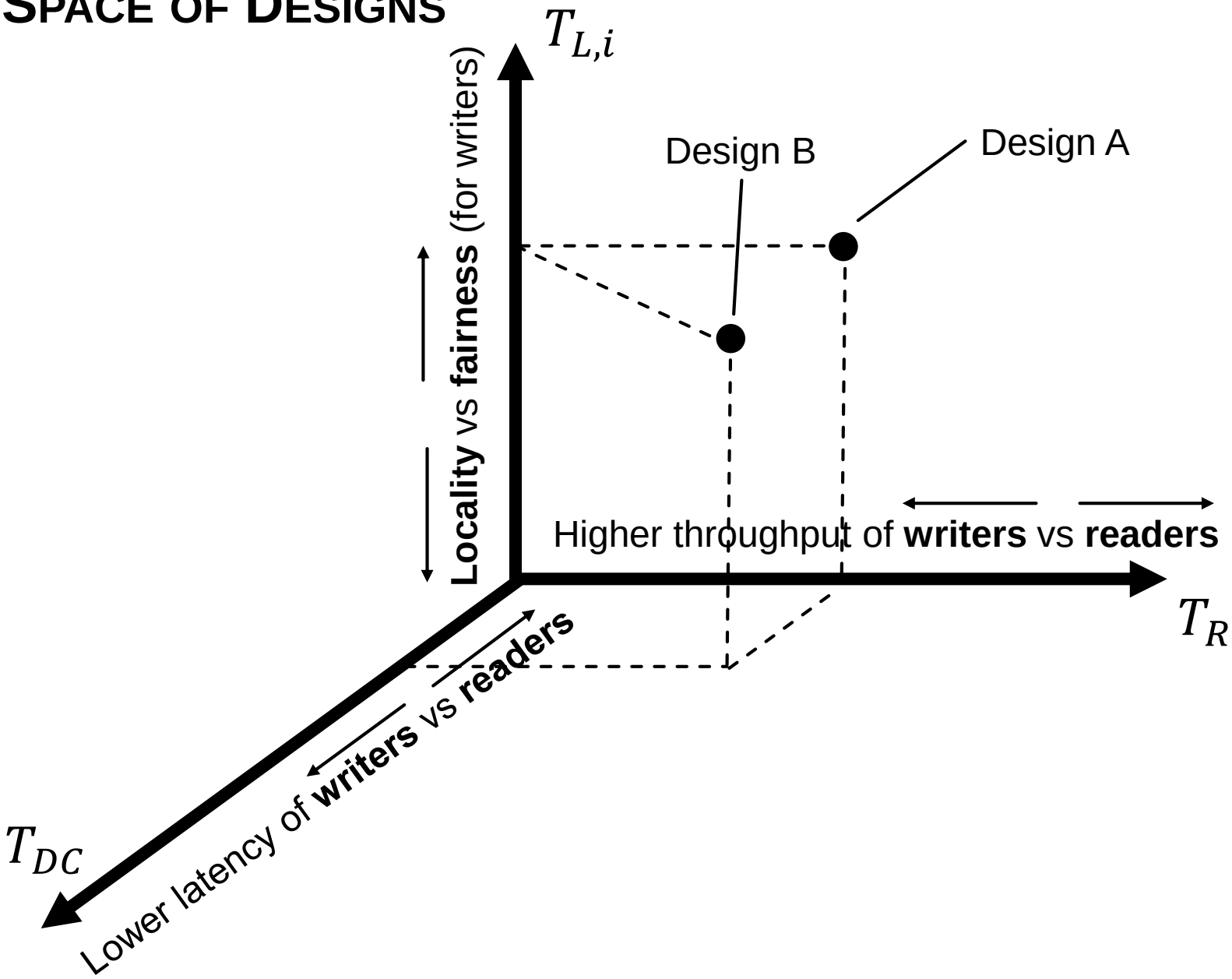


The Space of Designs

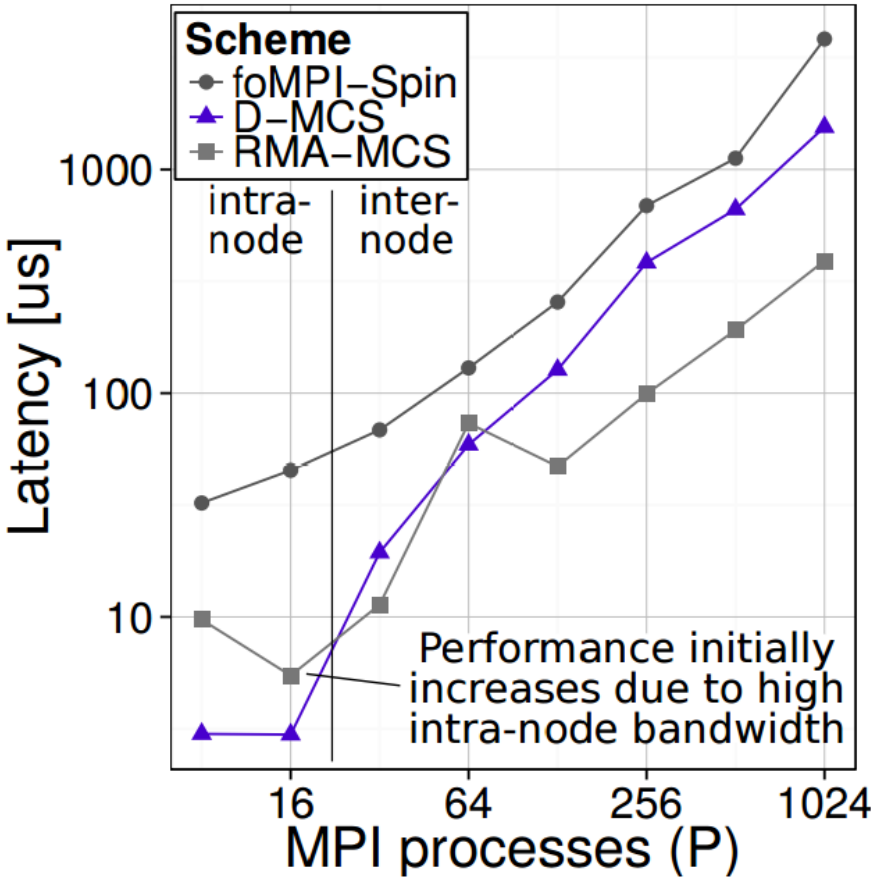


THE SPACE OF DESIGNS

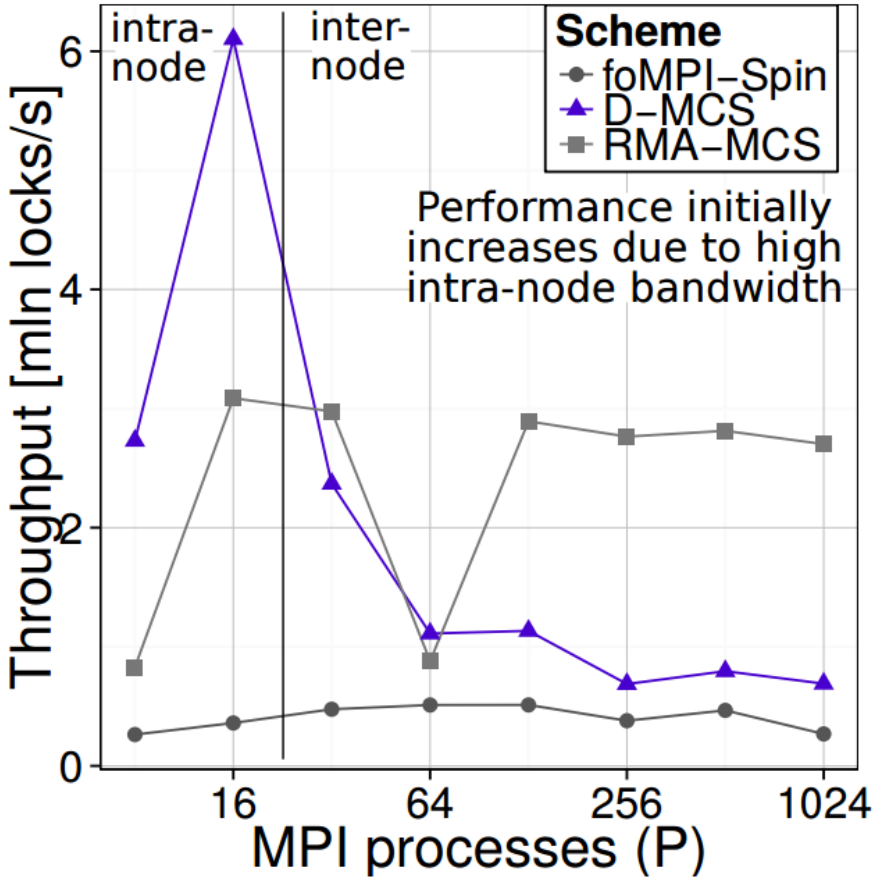


EVALUATION
D-MCS VS OTHERS

Latency (LB)



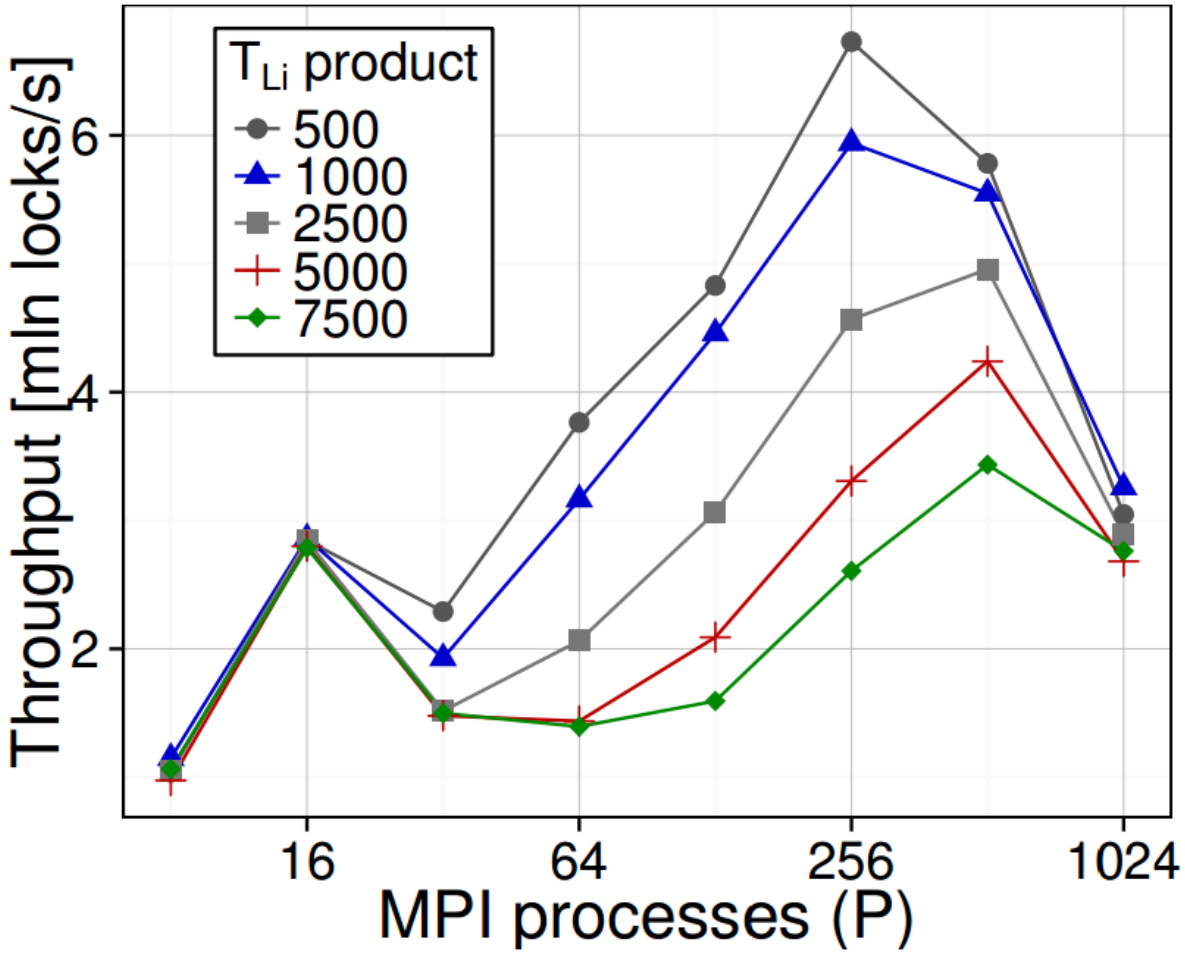
Throughput (ECSB)



EVALUATION
WRITER THRESHOLD ANALYSIS

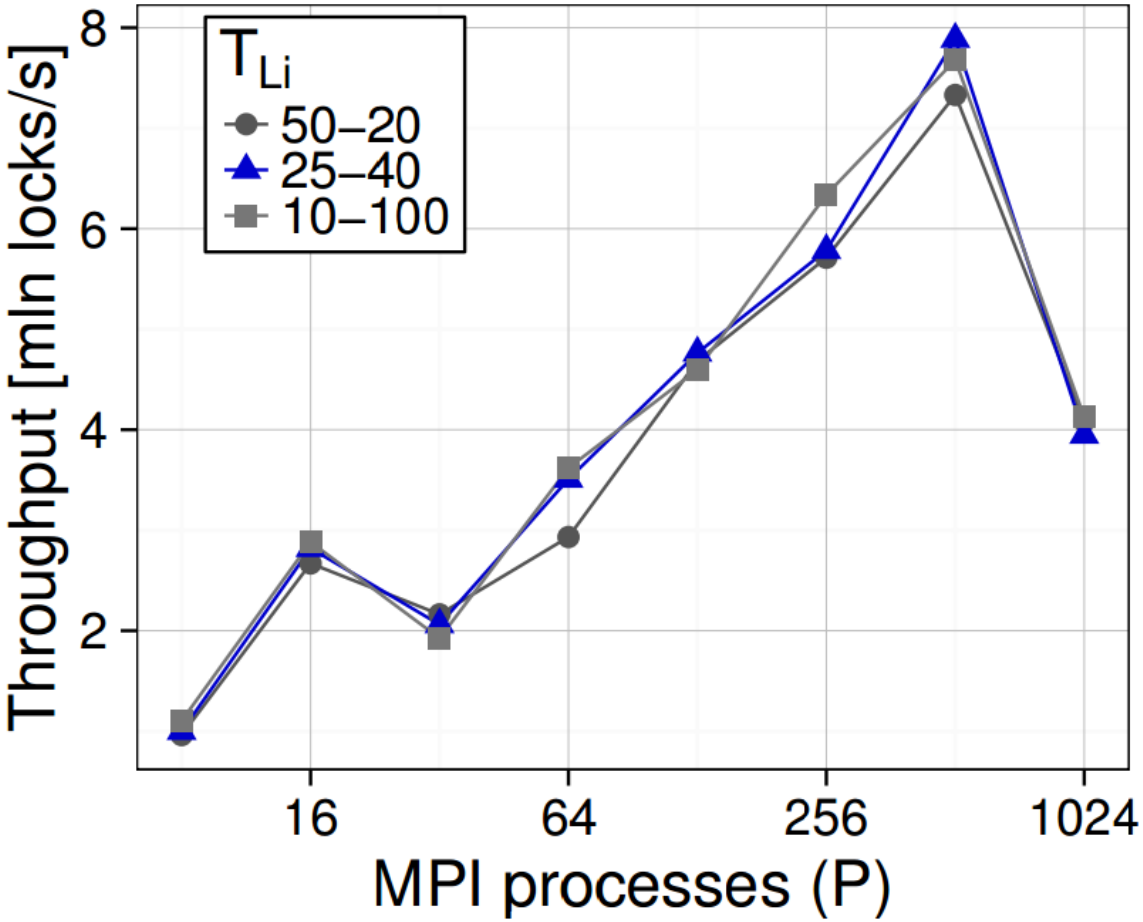
Throughput, 25% of writers

Single-operation benchmark



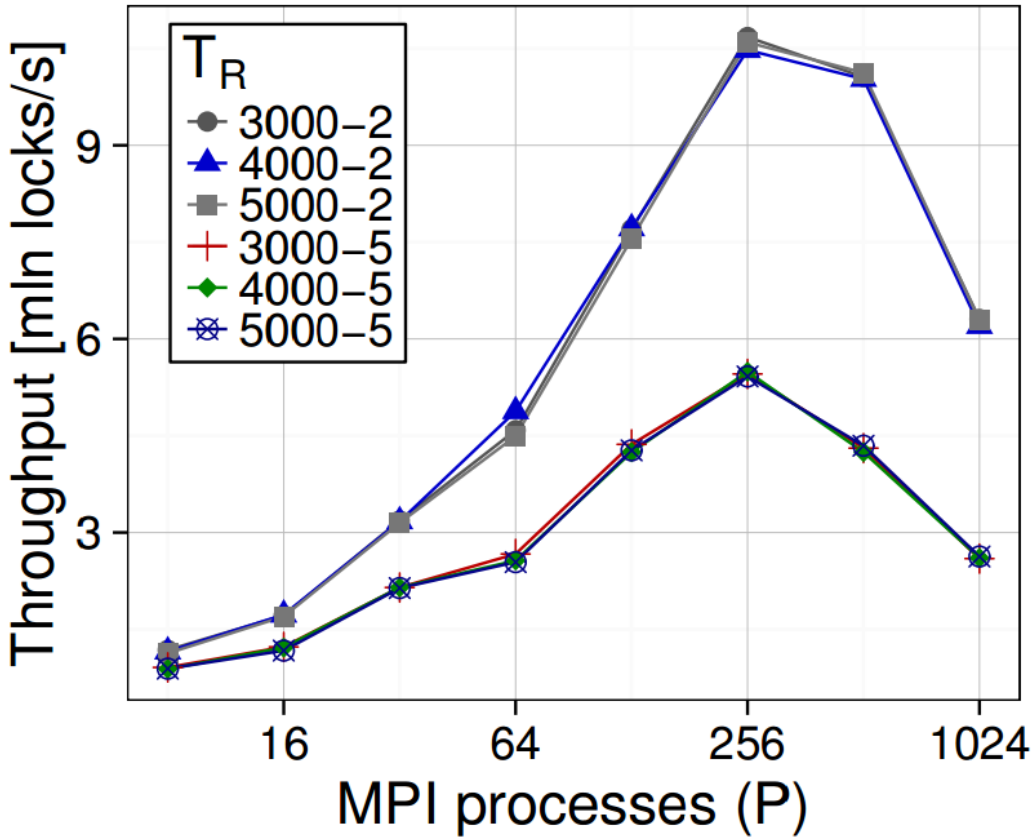
EVALUATION
FAIRNESS VS THROUGHPUT ANALYSIS

Throughput, 25% of writers,
Single-operation benchmark



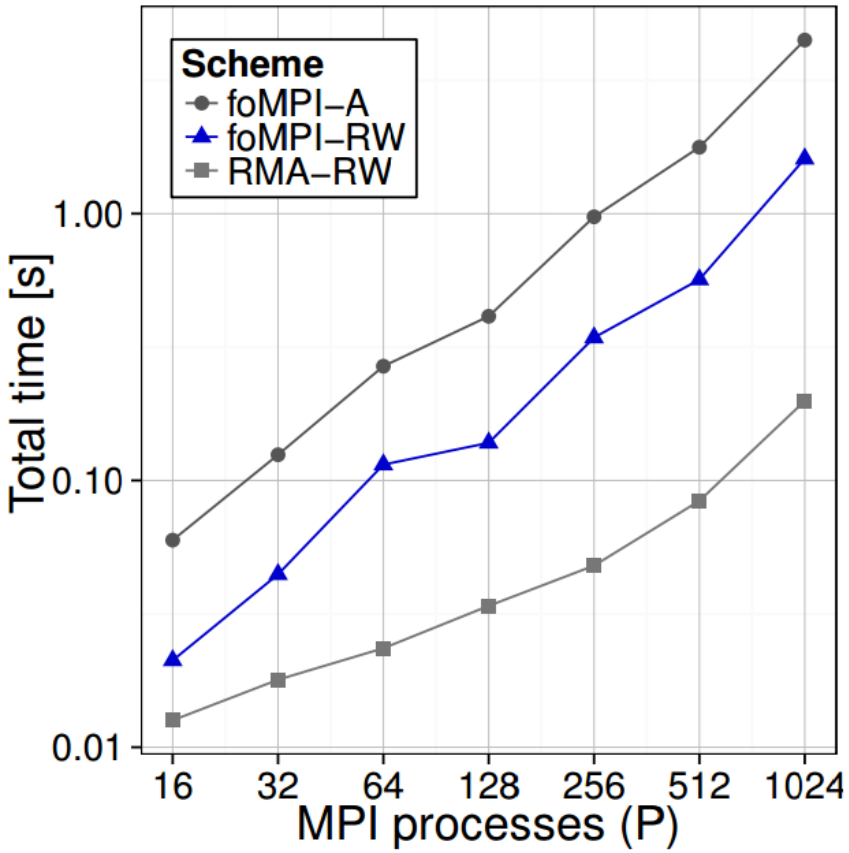
EVALUATION
READER THRESHOLD ANALYSIS

Throughput, 2% and 5% writers,
Empty-critical-section benchmark

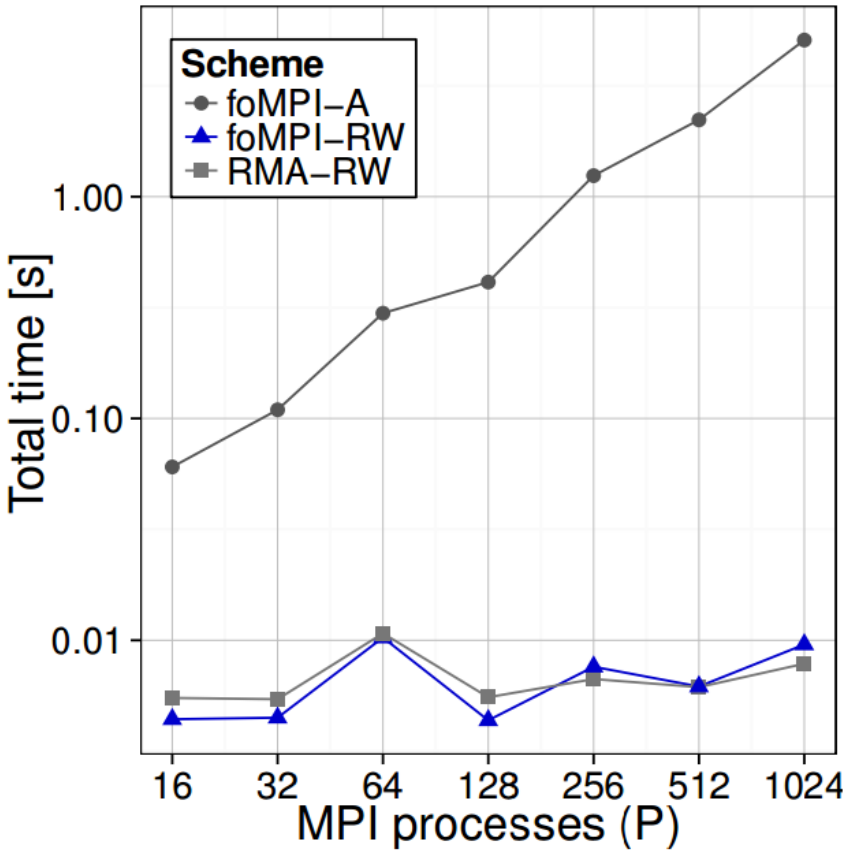


EVALUATION
DISTRIBUTED HASHTABLE

2% of writers



0% of writers



[1] R. Gerstenberger et al. Enabling Highly-scalable Remote Memory Access Programming with MPI-3 One Sided. ACM/IEEE Supercomputing 2013.

FEASIBILITY ANALYSIS

Feasibility Analysis

	UPC (standard) [44]	Berkeley UPC [1]	SHMEM [4]
Put	UPC_SET	bupc_atomicX_set_RS	shmem_swap
Get	UPC_GET	bupc_atomicX_read_RS	shmem_mswap
Accumulate	UPC_INC	bupc_atomicX_fetchadd_RS	shmem_fadd
FAO (SUM)	UPC_INC, UPC_DEC	bupc_atomicX_fetchadd_RS	shmem_fadd
FAO (REPLACE)	UPC_SET	bupc_atomicX_swap_RS	shmem_swap
CAS	UPC_CSWAP	bupc_atomicX_cswap_RS	shmem_cswap

FEASIBILITY ANALYSIS

	UPC (standard) [44]	Berkeley UPC [1]	SHMEM [4]
Put	UPC_SET	bupc_atomicX_set_RS	shmem_swap
Get	UPC_GET	bupc_atomicX_read_RS	shmem_mswap
Accumulate	UPC_INC	bupc_atomicX_fetchadd_RS	shmem_fadd
FAO (SUM)	UPC_INC, UPC_DEC	bupc_atomicX_fetchadd_RS	shmem_fadd
FAO (REPLACE)	UPC_SET	bupc_atomicX_swap_RS	shmem_swap
CAS	UPC_CSWAP	bupc_atomicX_cswap_RS	shmem_cswap

	Fortran 2008 [27]	Linux RDMA/IB [33, 43]	iWARP [18, 41]
Put	atomic_define	MskCmpSwap	masked CmpSwap
Get	atomic_ref	MskCmpSwap	masked CmpSwap
Accumulate	atomic_add	FetchAdd	FetchAdd
FAO (SUM)	atomic_add	FetchAdd	FetchAdd
FAO (REPLACE)	atomic_define*	MskCmpSwap	masked CmpSwap
CAS	atomic_cas	CmpSwap	CmpSwap

RMA-RW
Required Operations

Process p

Memory

Process q

Memory

3

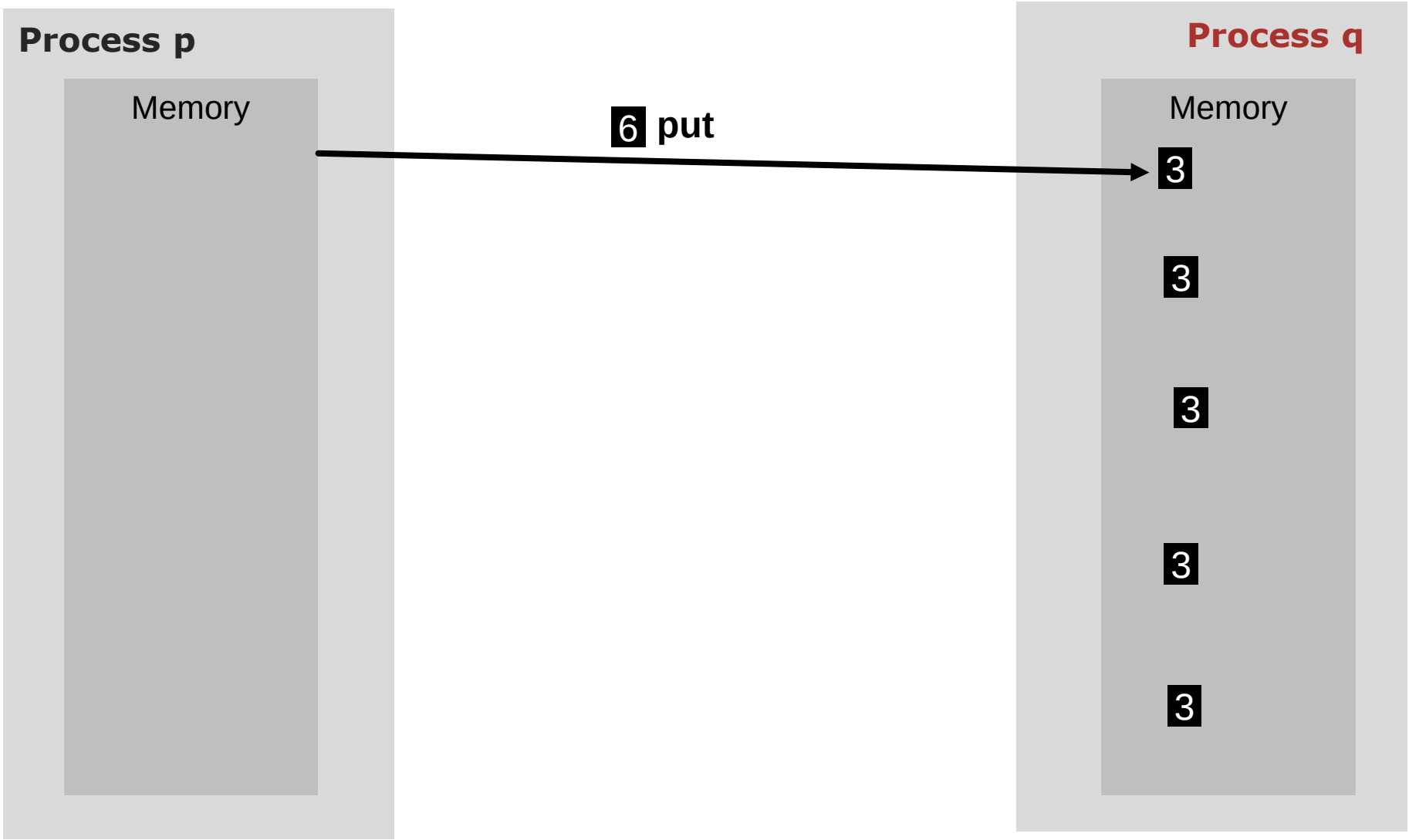
3

3

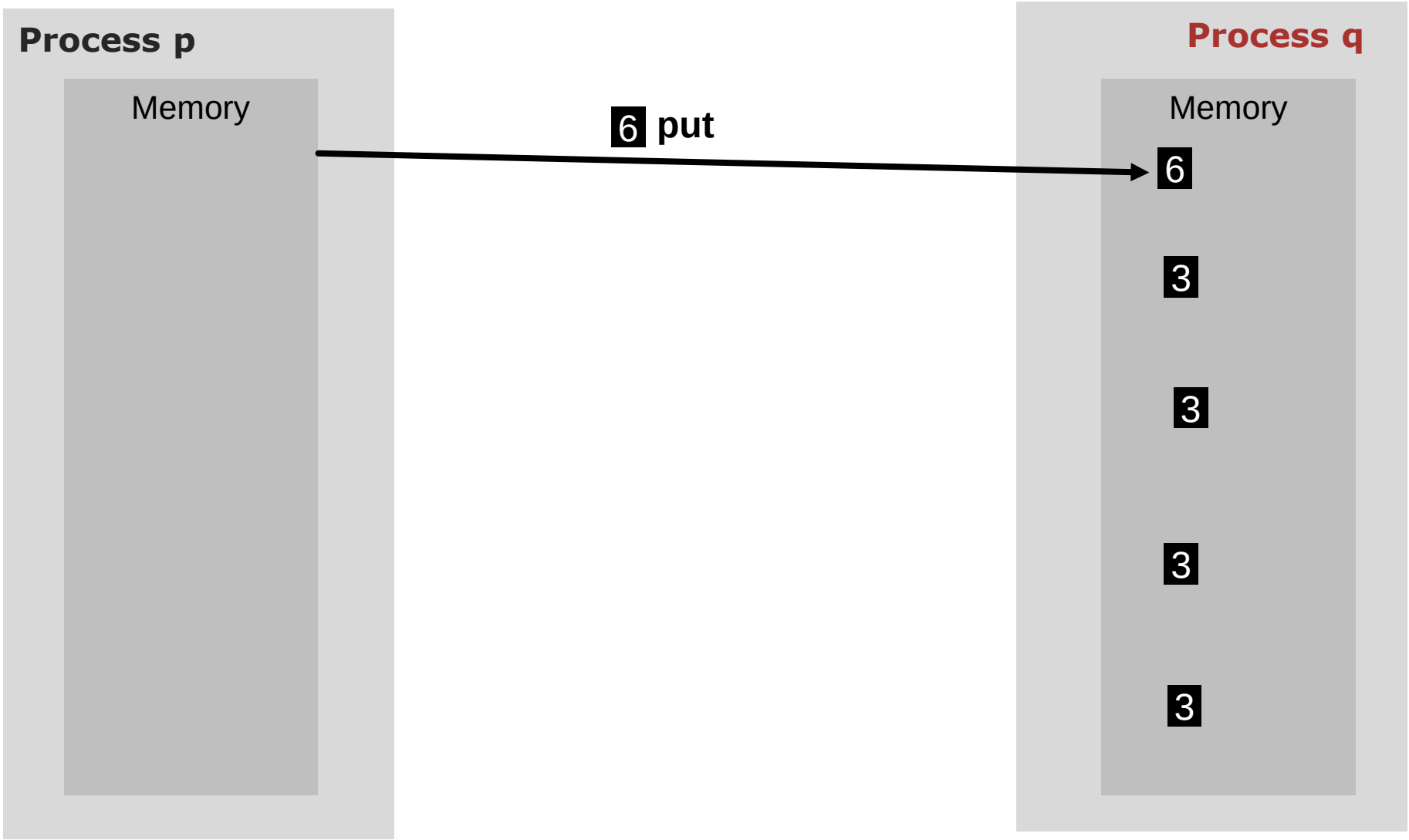
3

3

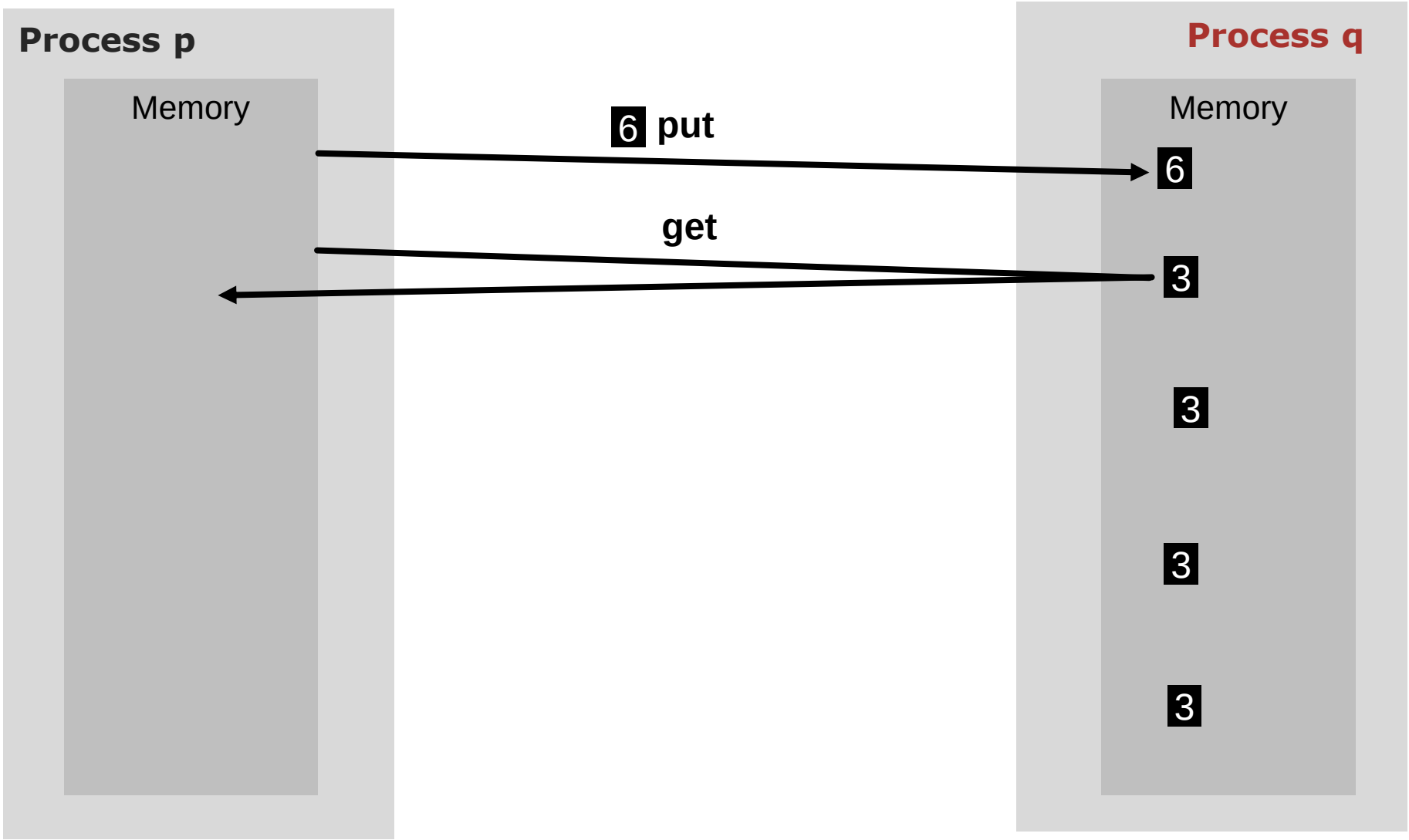
RMA-RW
Required Operations



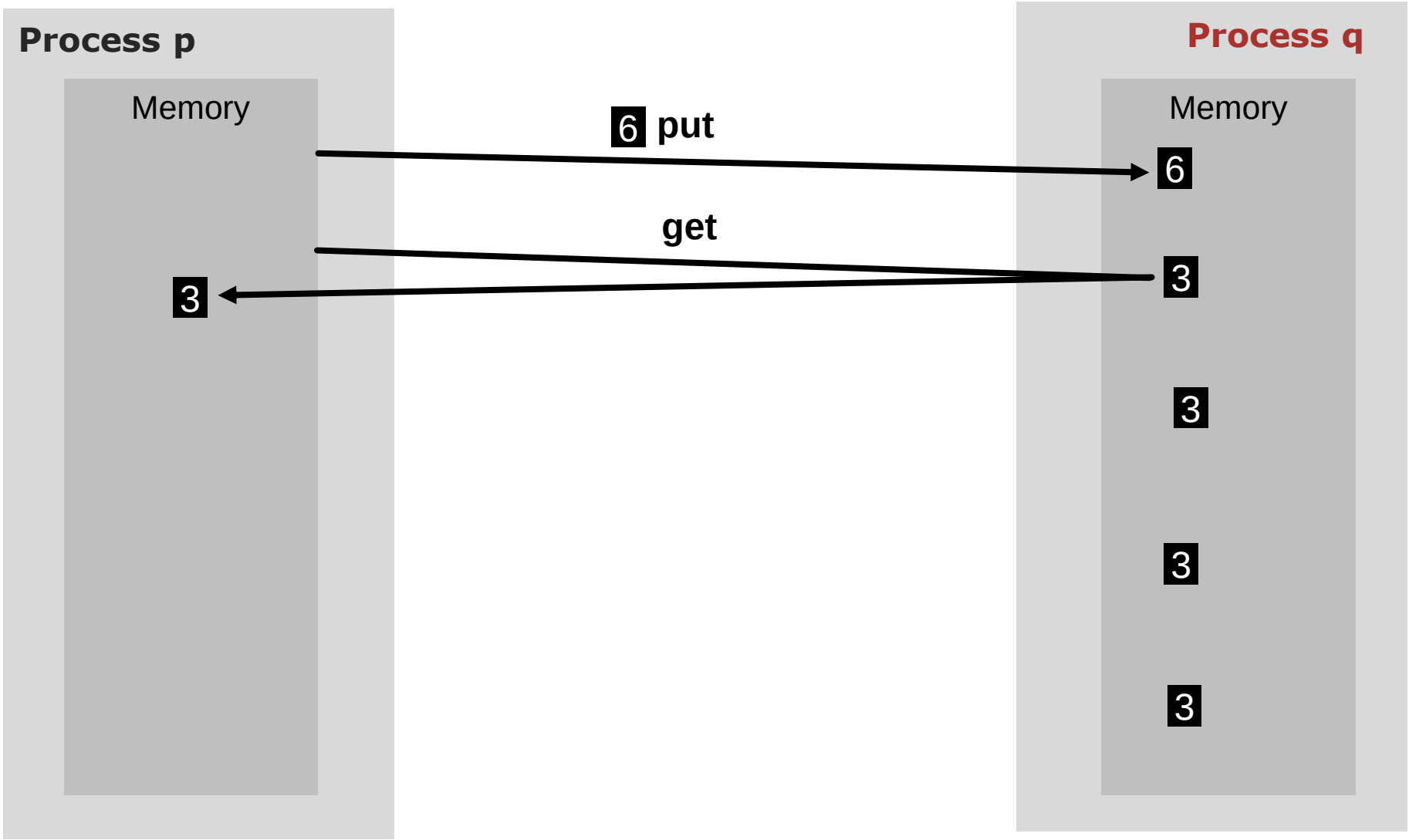
RMA-RW
Required Operations



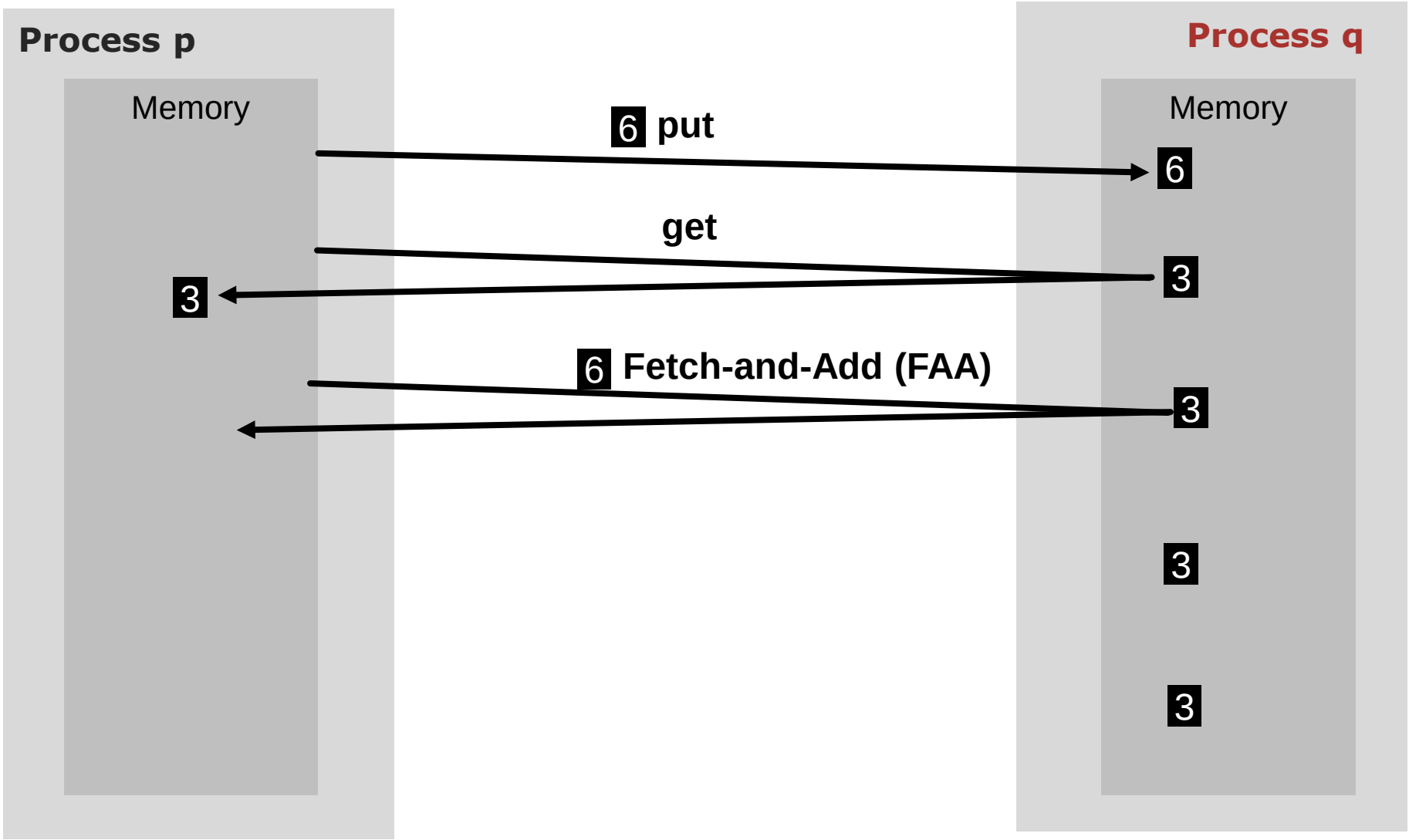
RMA-RW
Required Operations



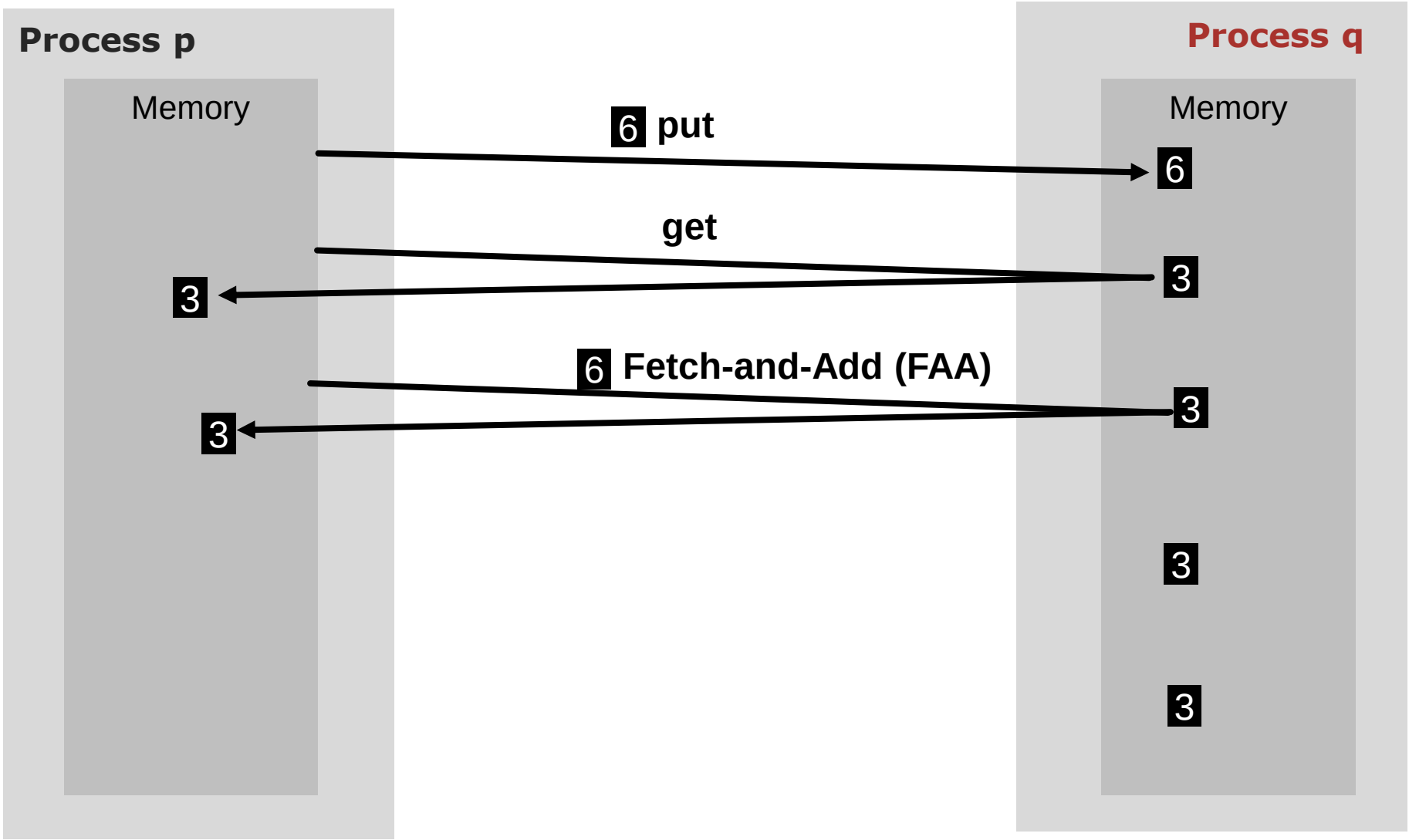
RMA-RW
Required Operations



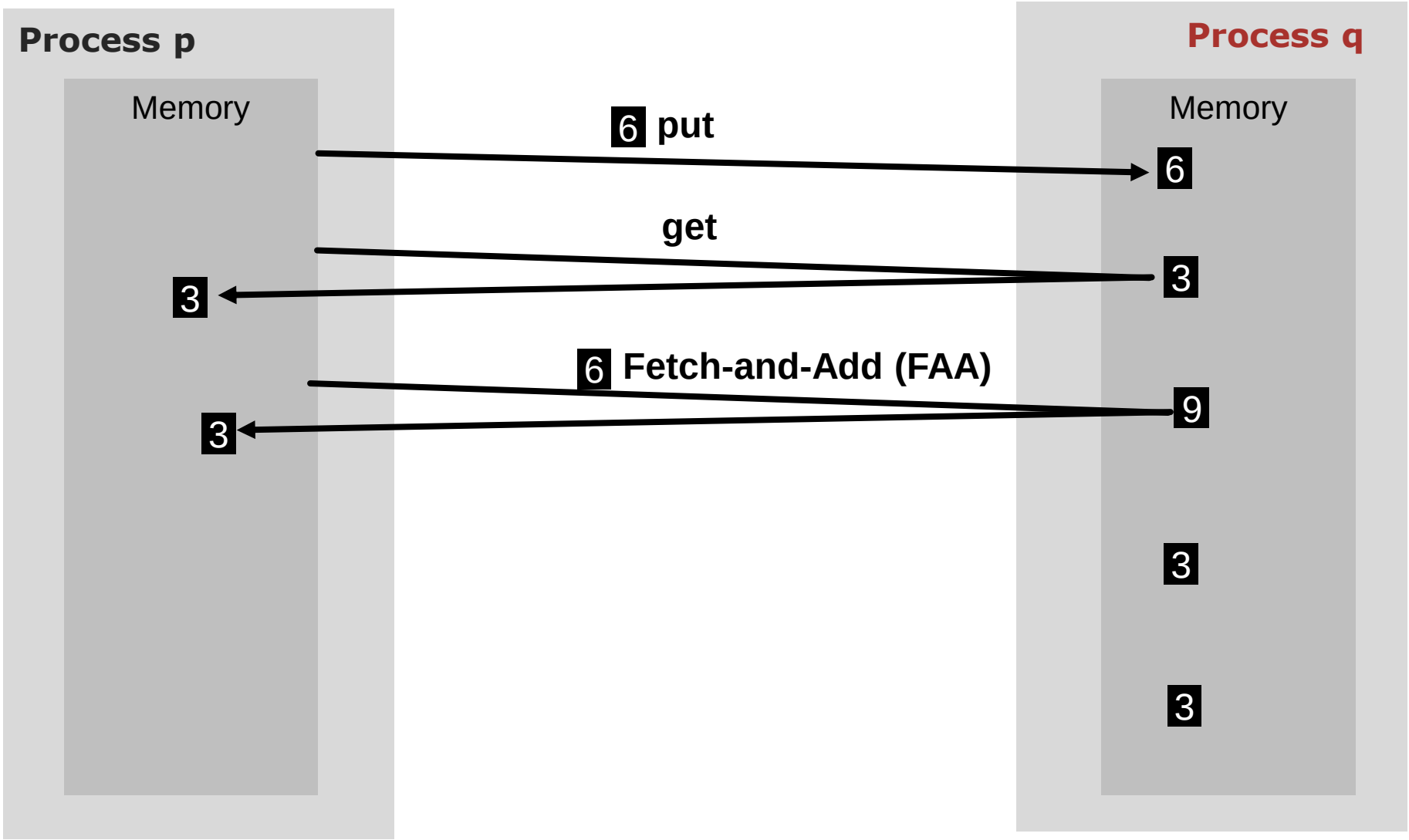
RMA-RW
Required Operations



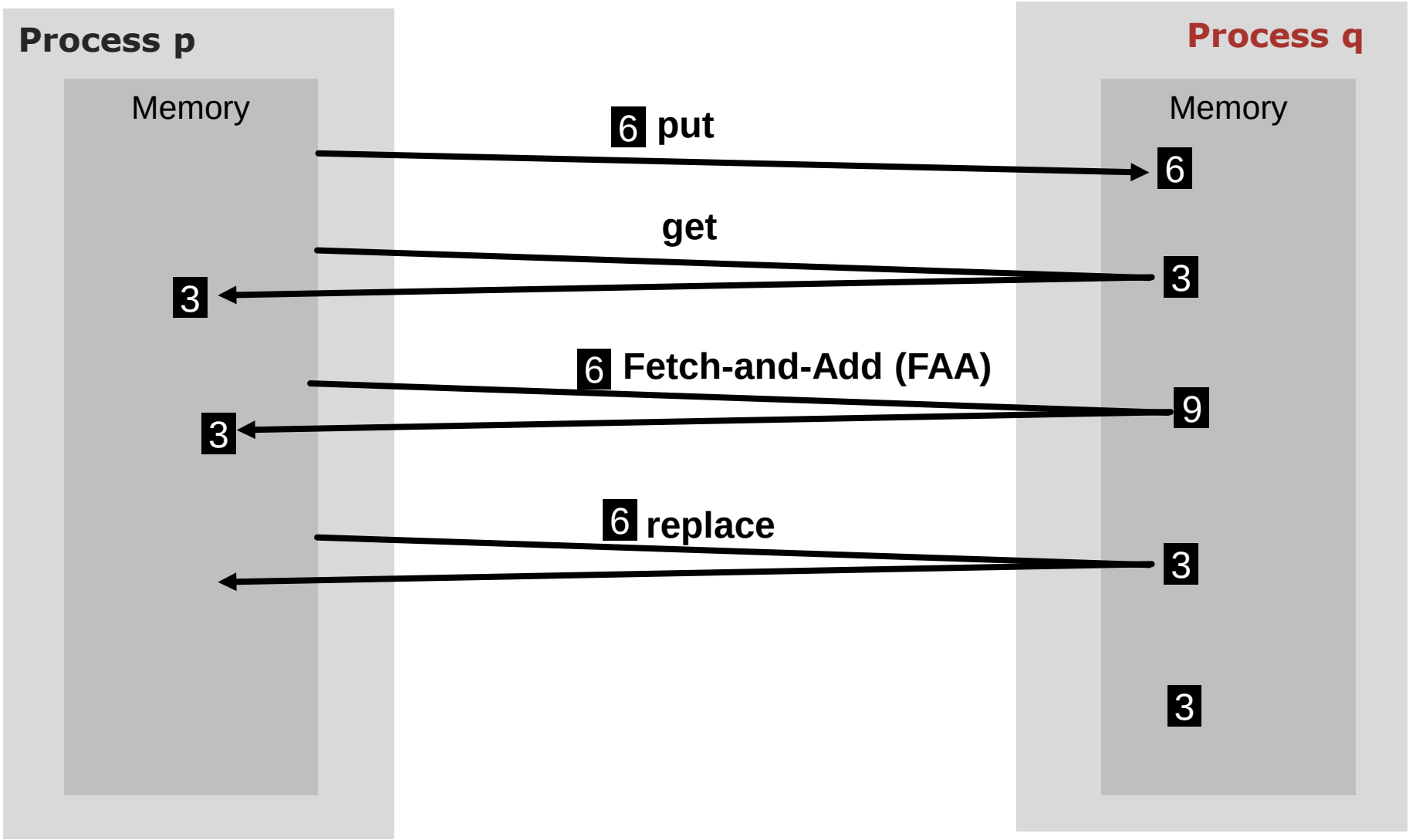
RMA-RW
Required Operations



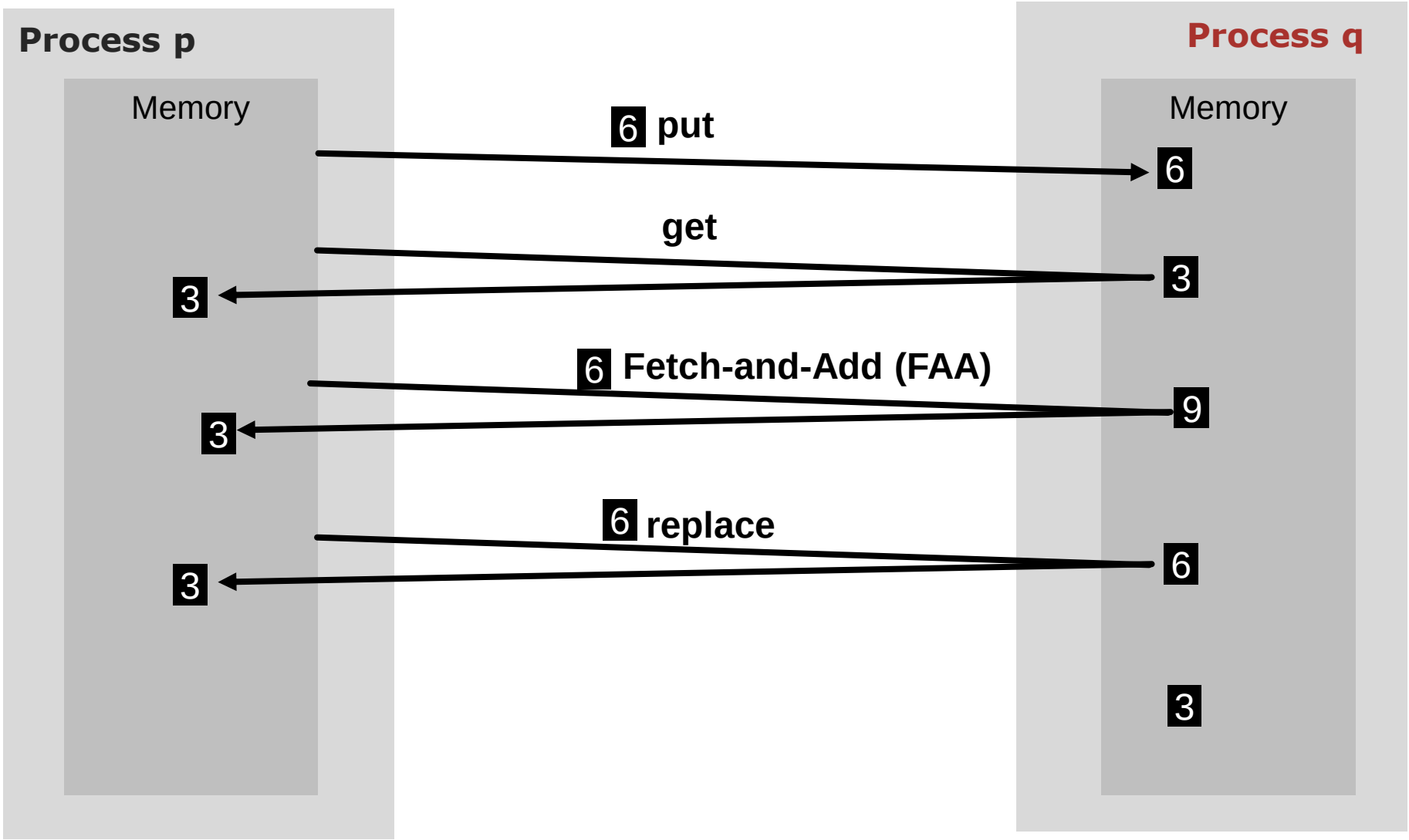
RMA-RW
Required Operations



RMA-RW
Required Operations



RMA-RW
Required Operations



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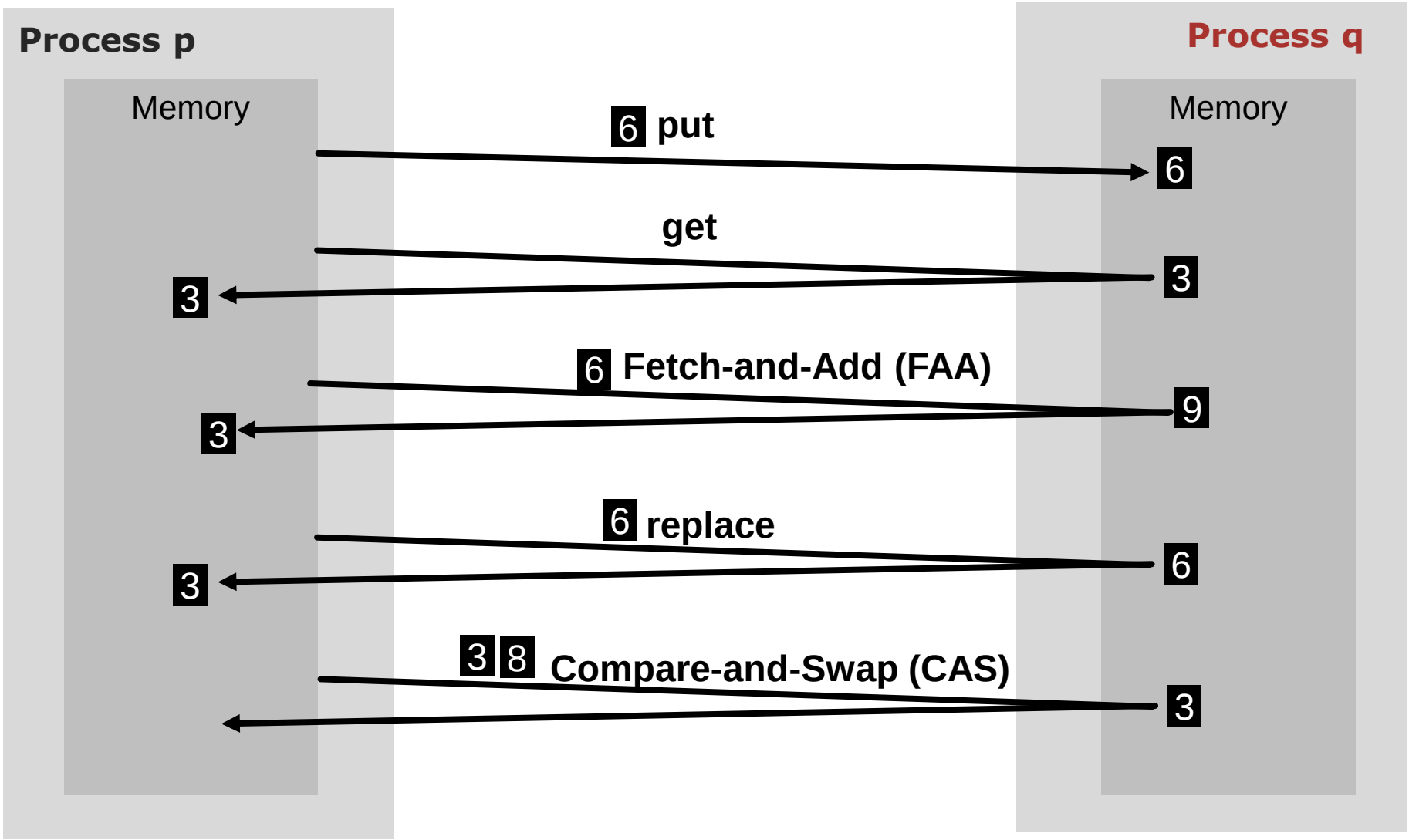
Required Operations



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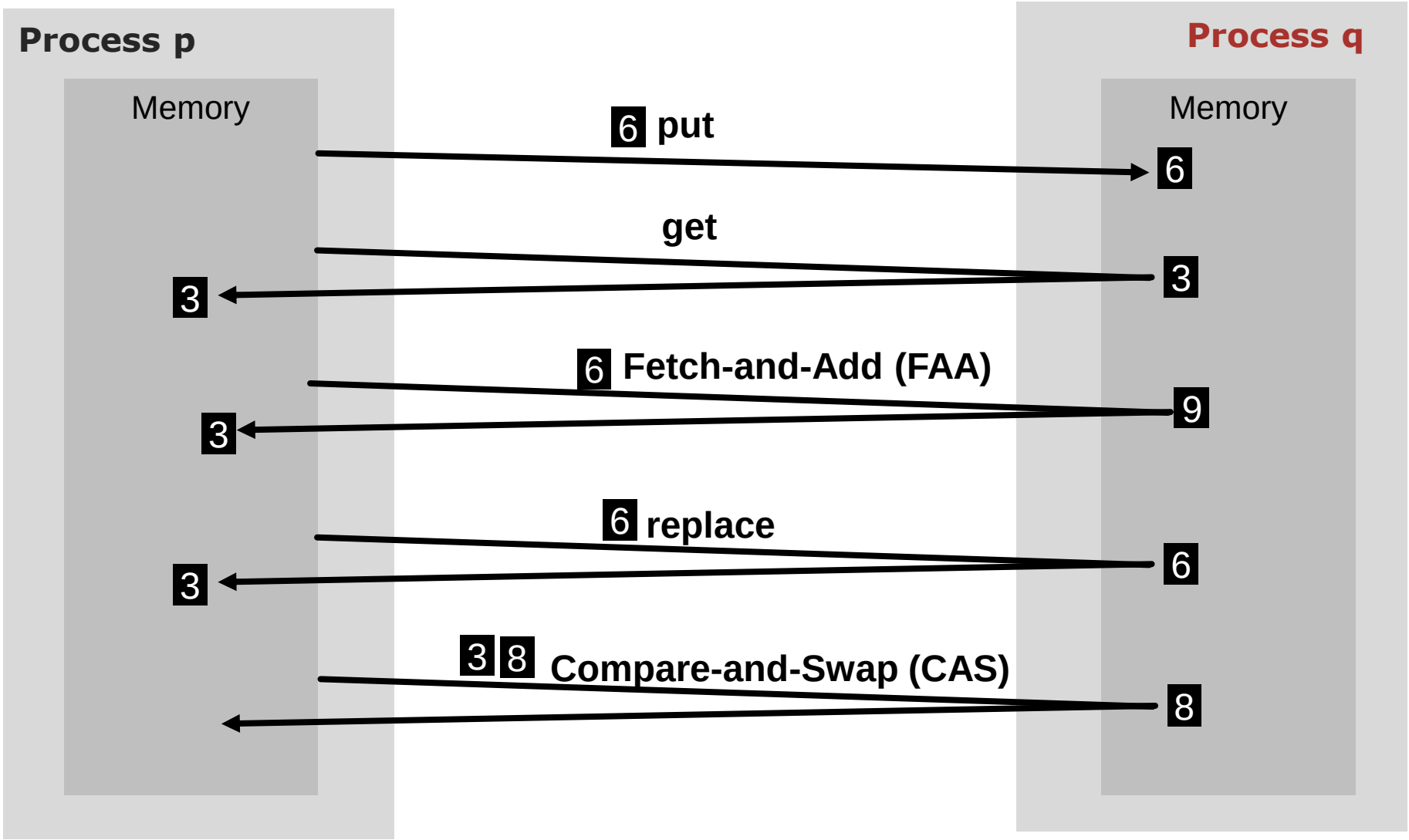
Required Operations



RMA-RW
Required Operations