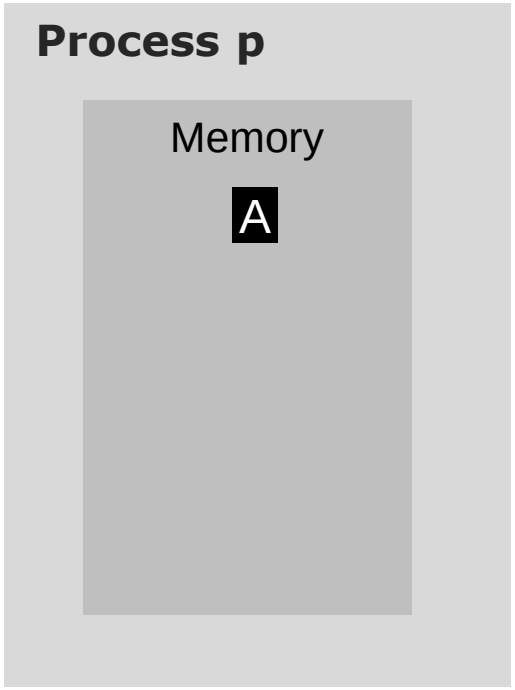
Fault Tolerance for Remote Memory Access Programming Models

MACIEJ BESTA, TORSTEN HOEFLER

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Remote Memory Access (RMA) Programming



Remote Memory Access (RMA) Programming

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Process p

Memory

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Process q

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Cray BlueWaters

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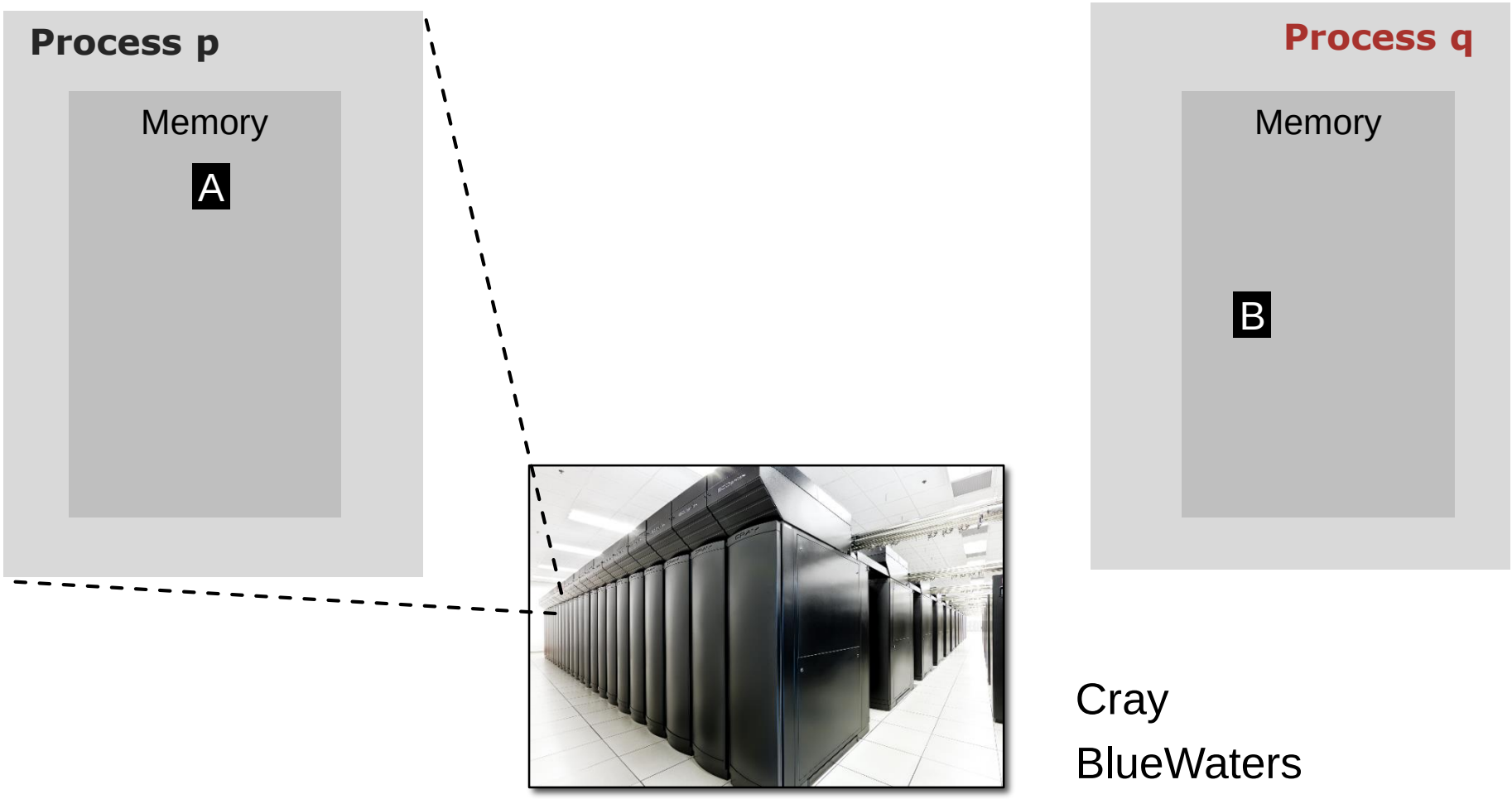

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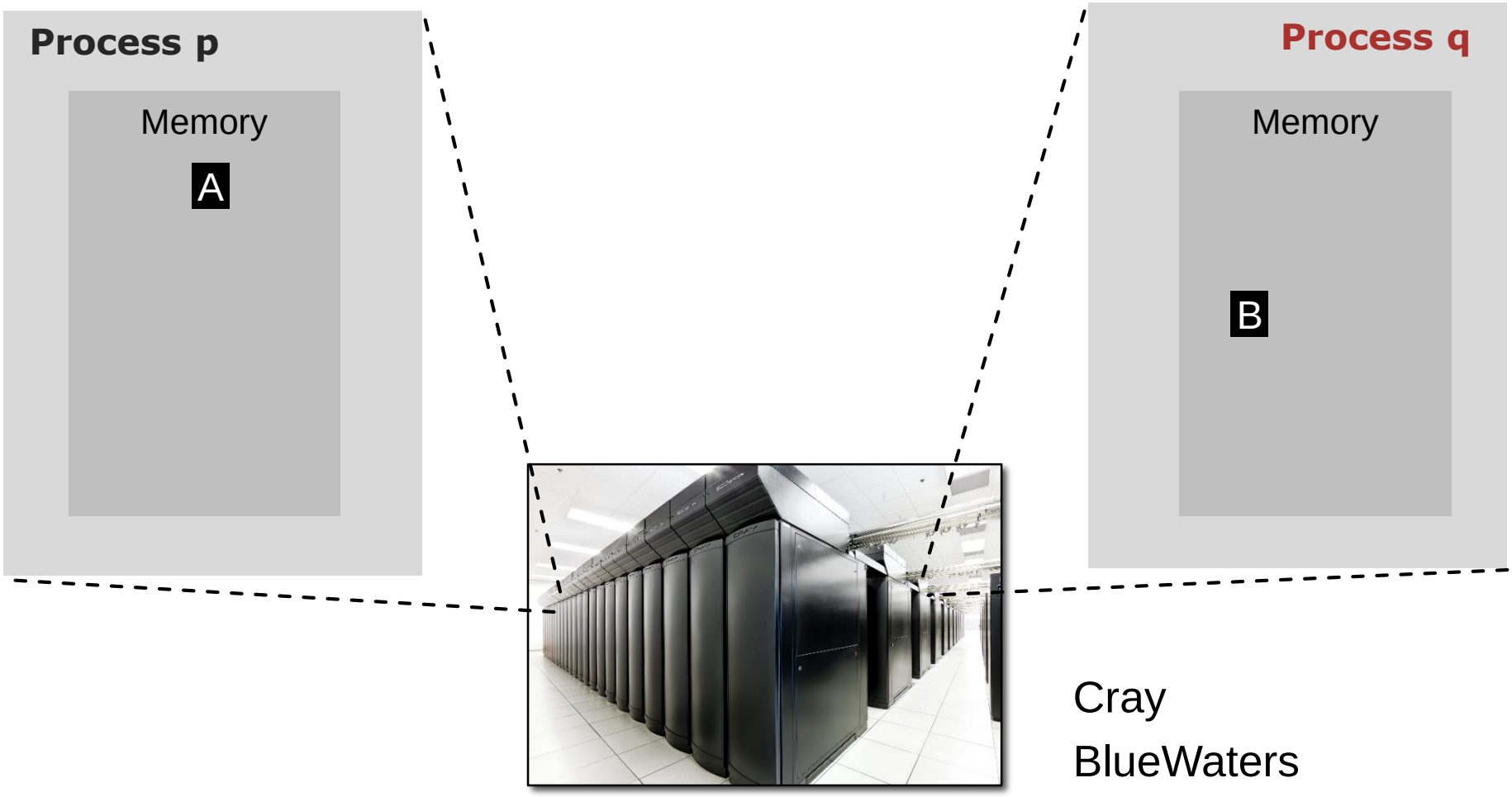

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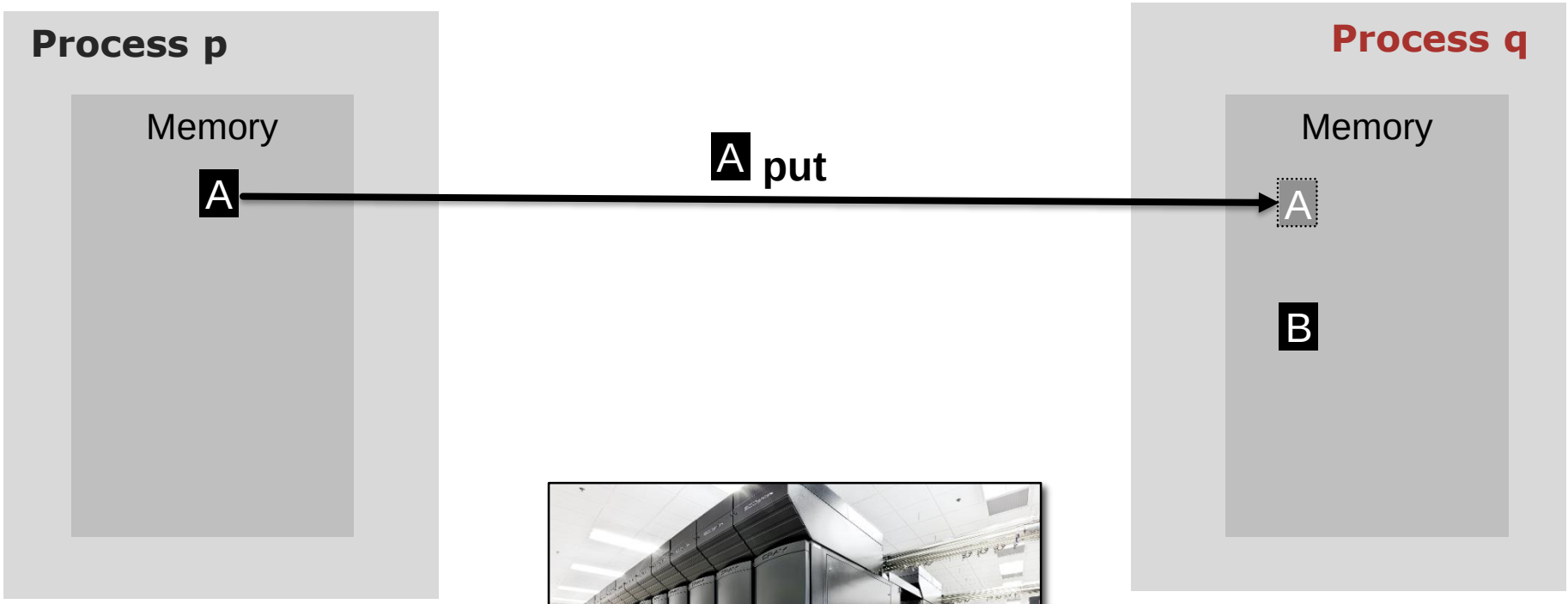

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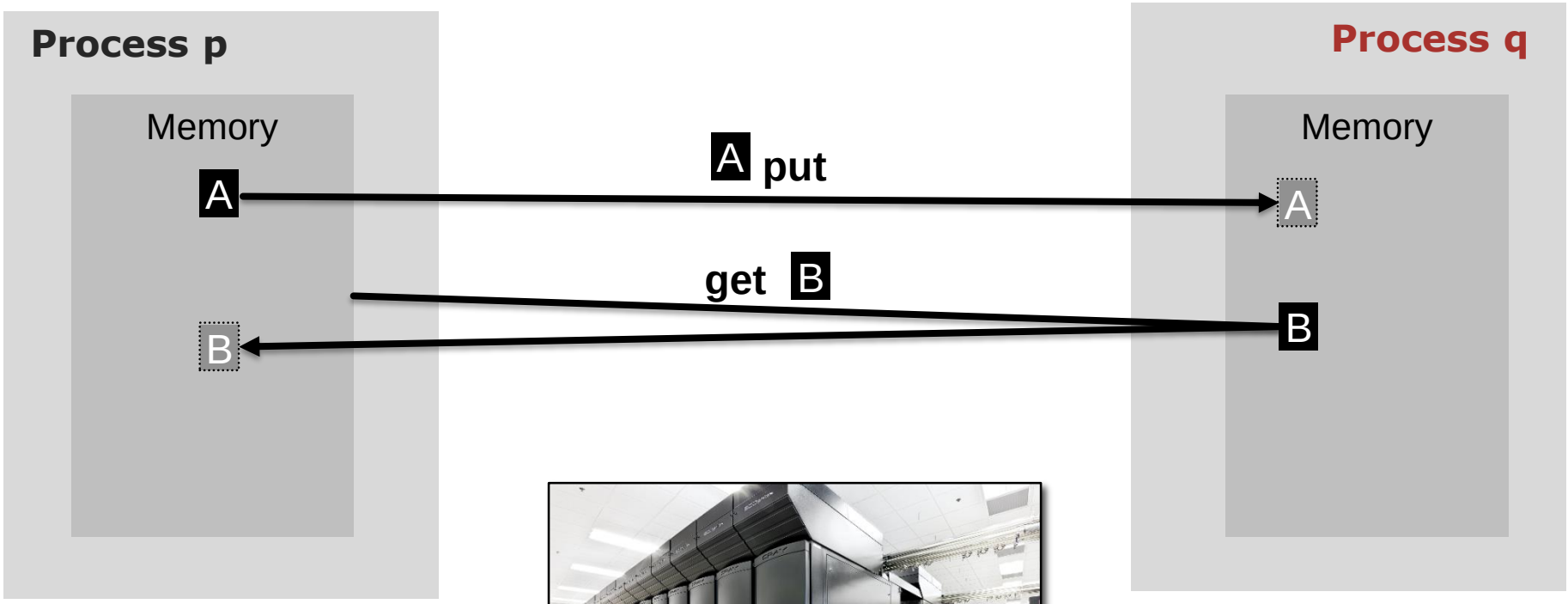

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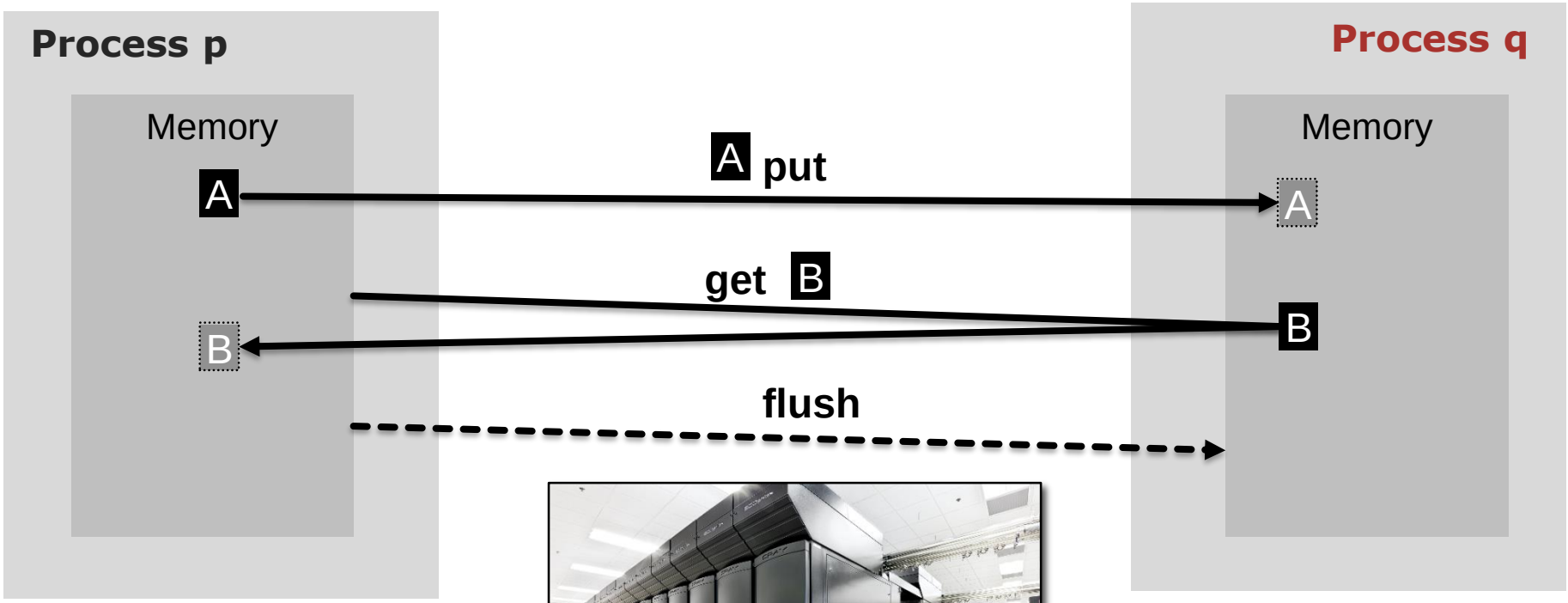

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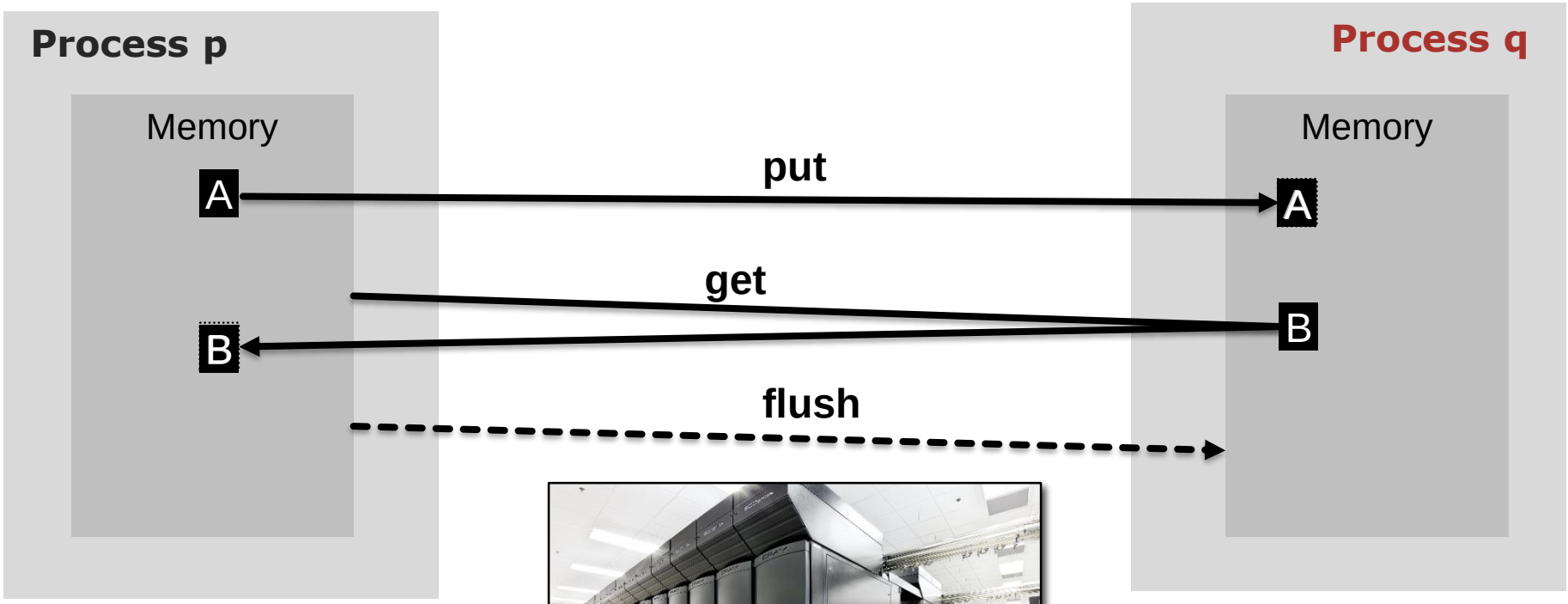

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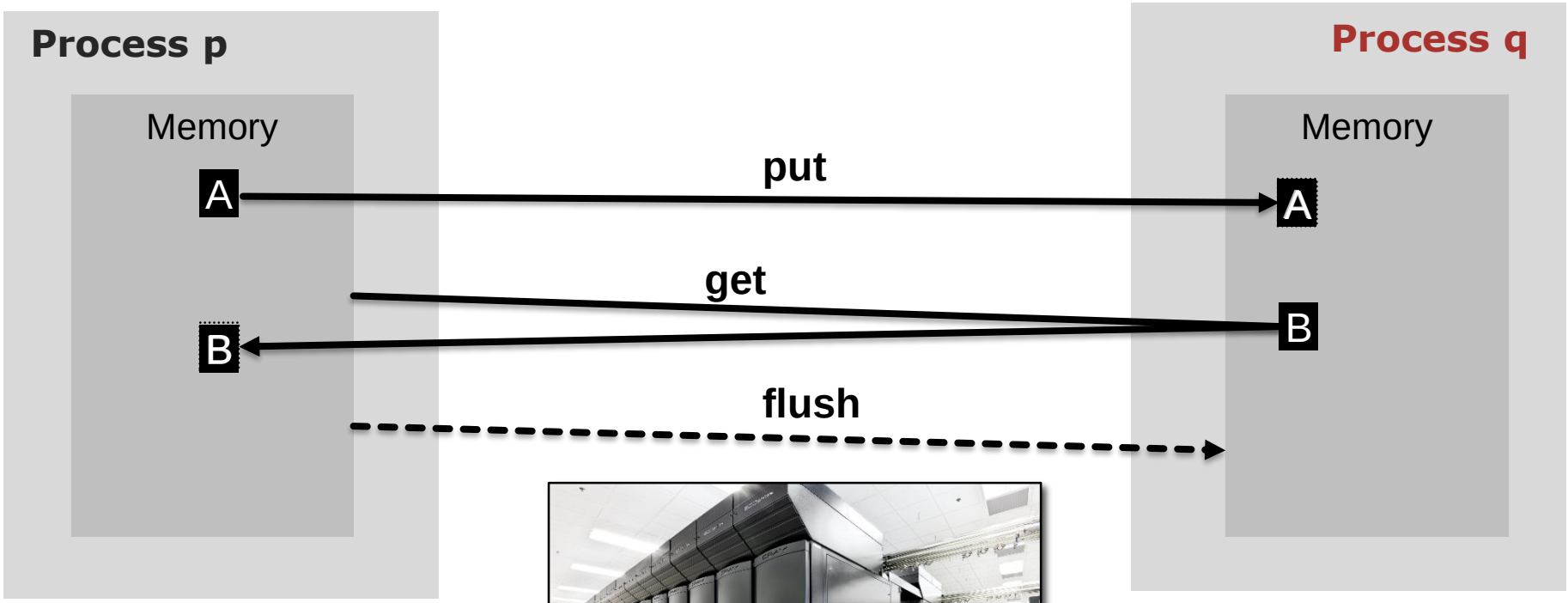

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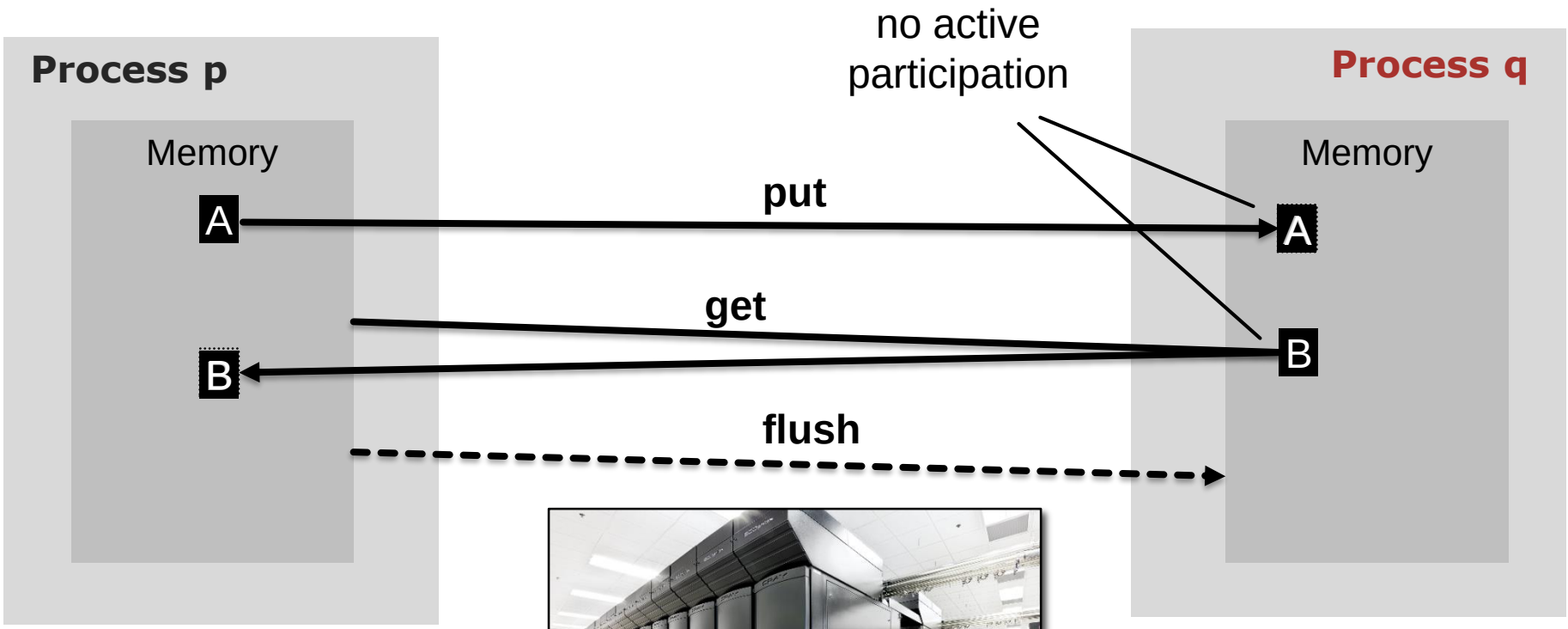

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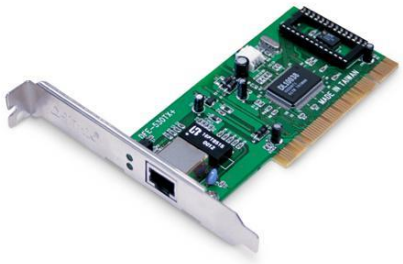
- Implemented in hardware in NICs in the majority of HPC networks support RDMA



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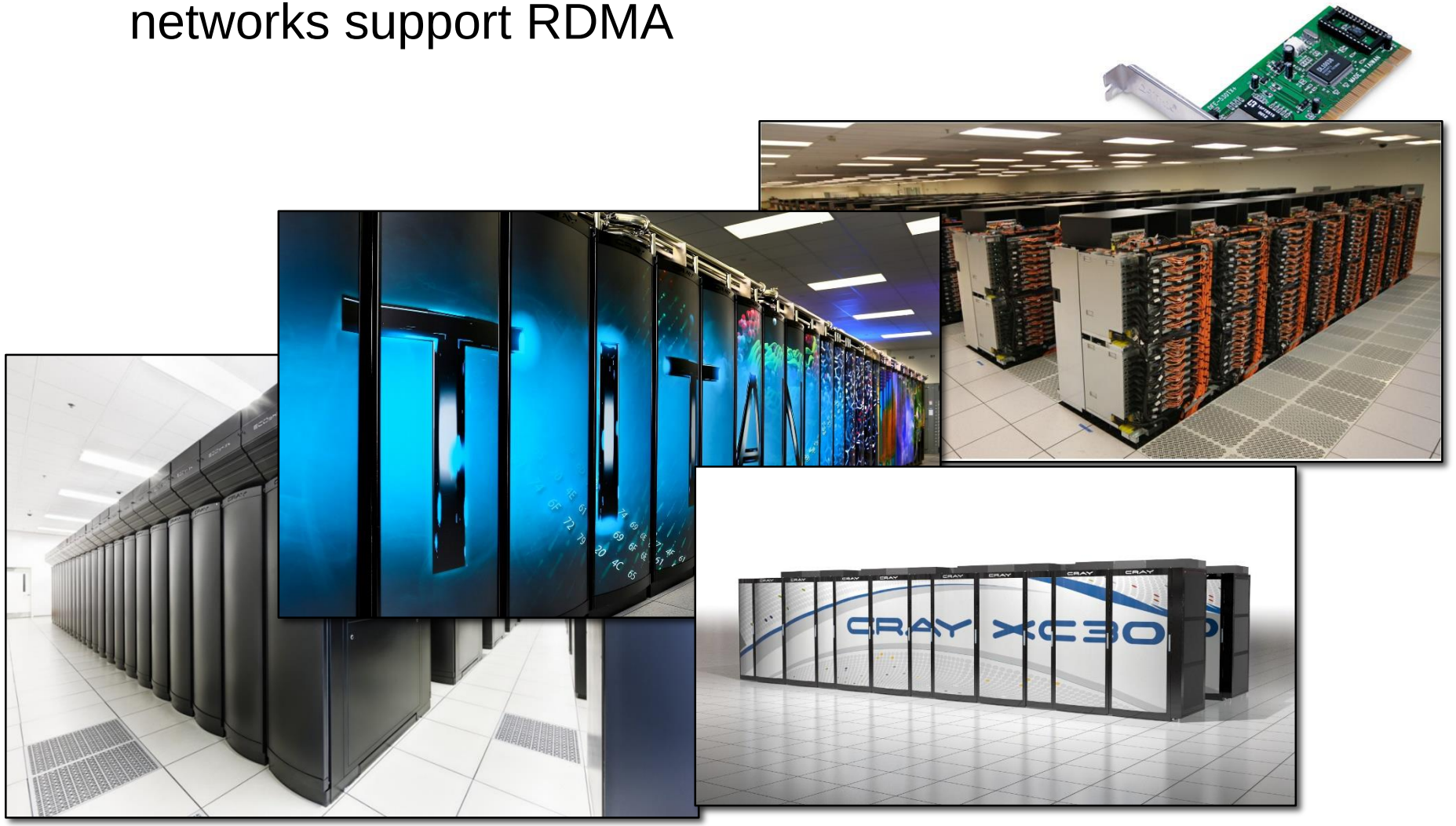

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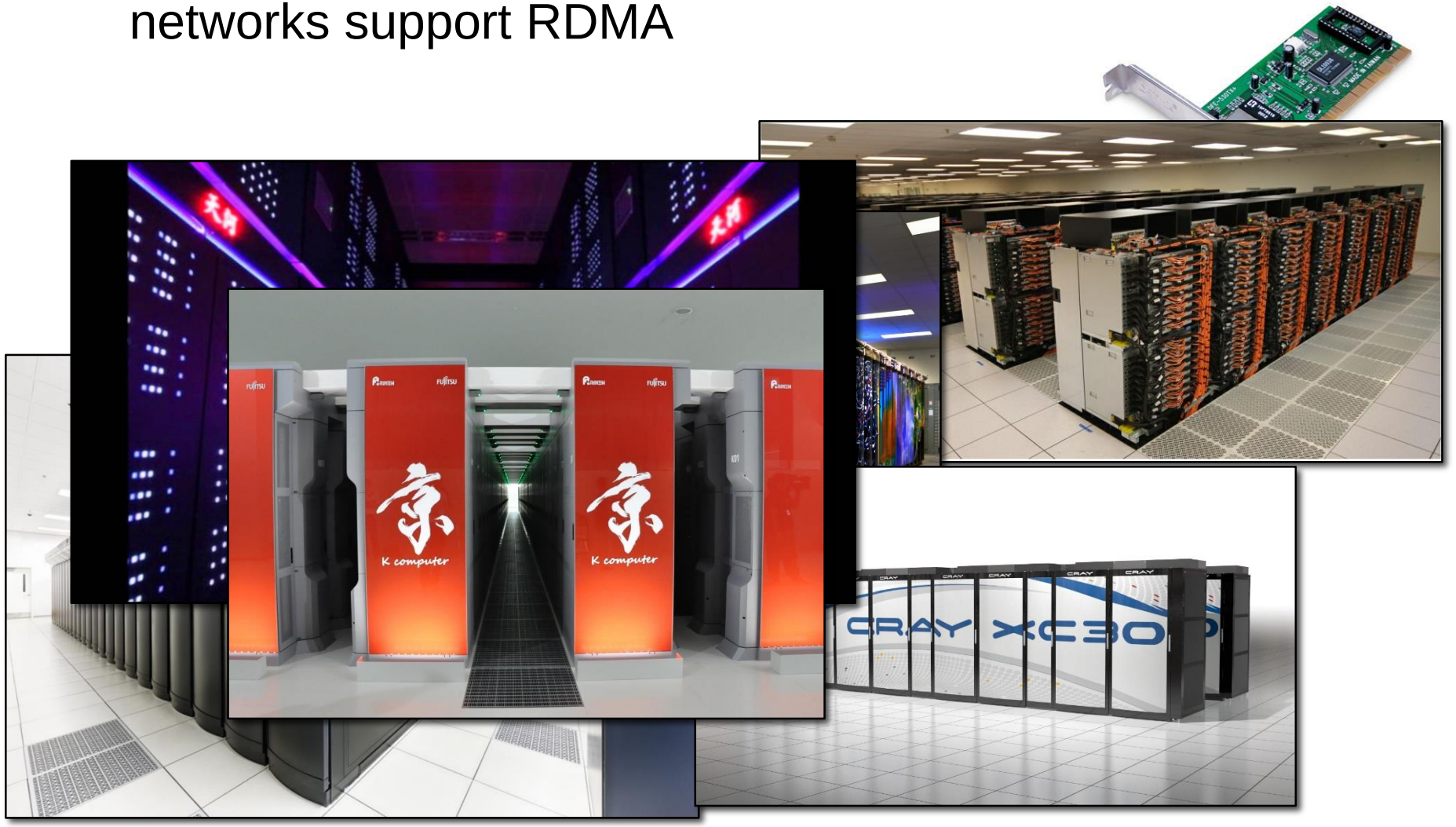

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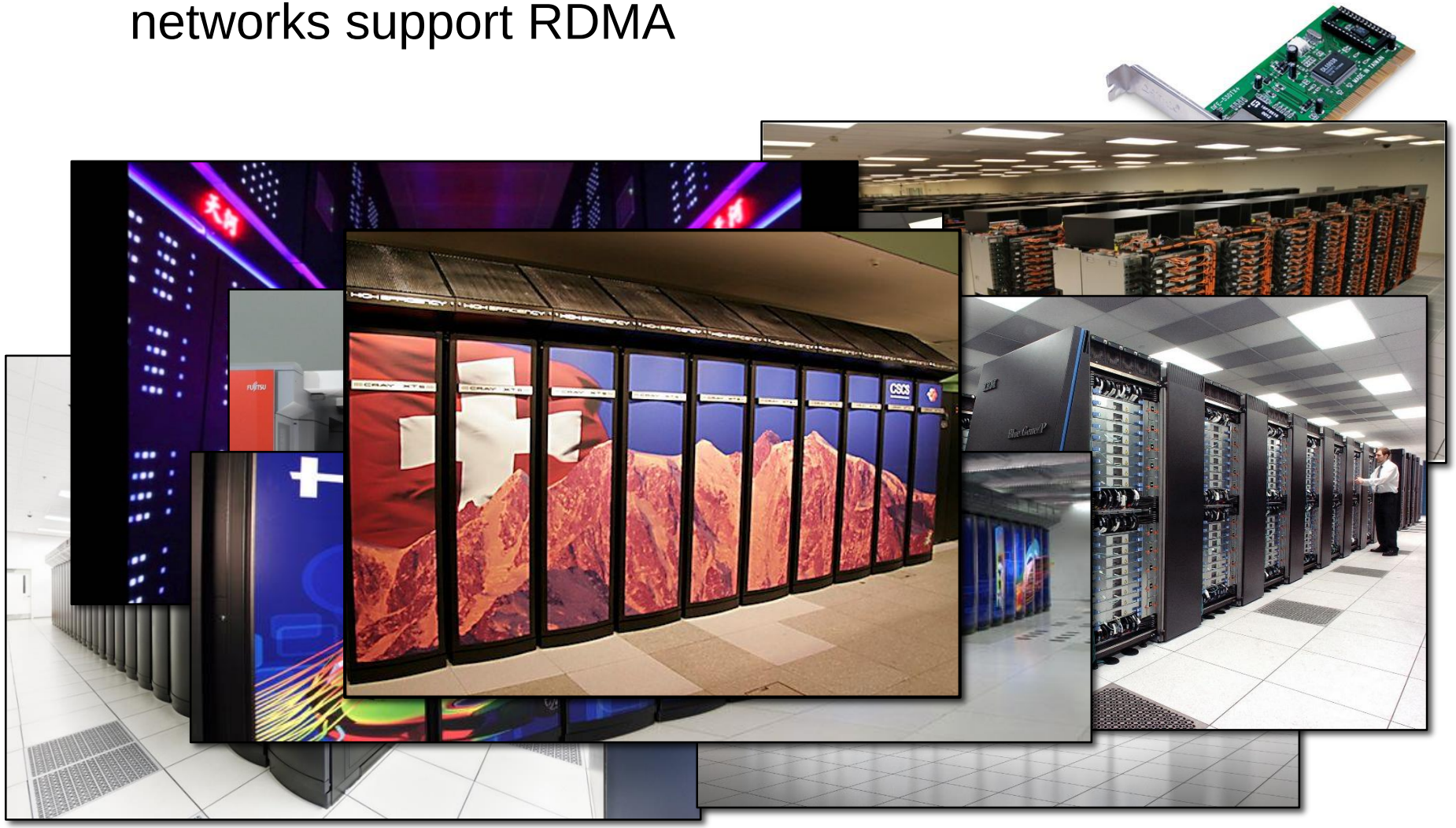

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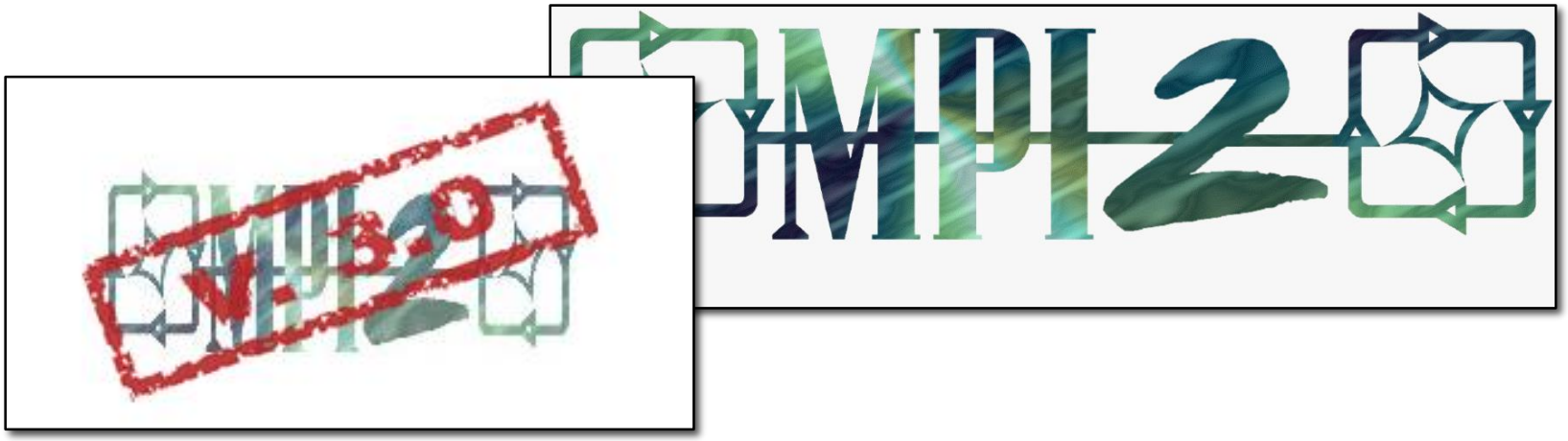

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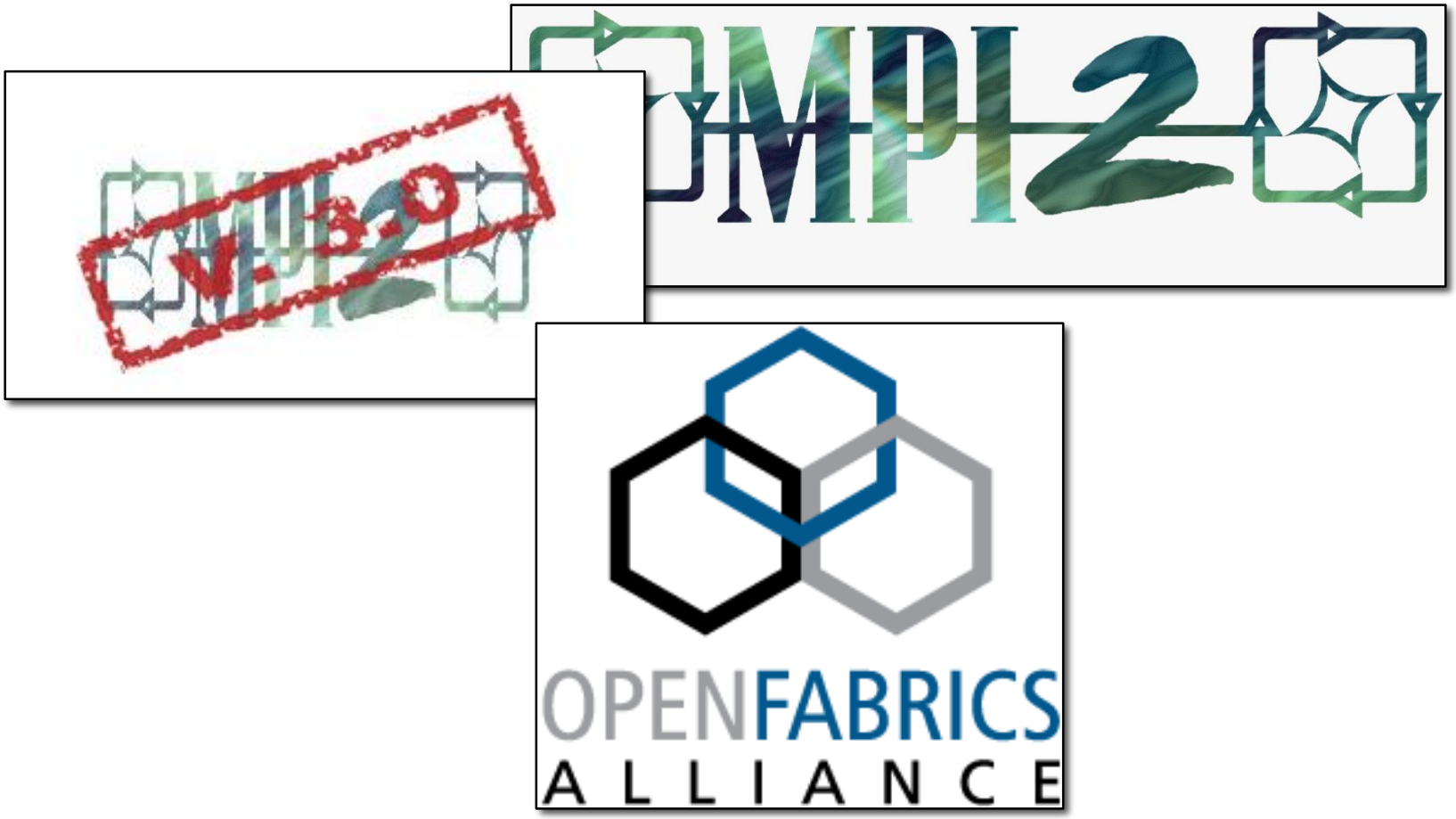

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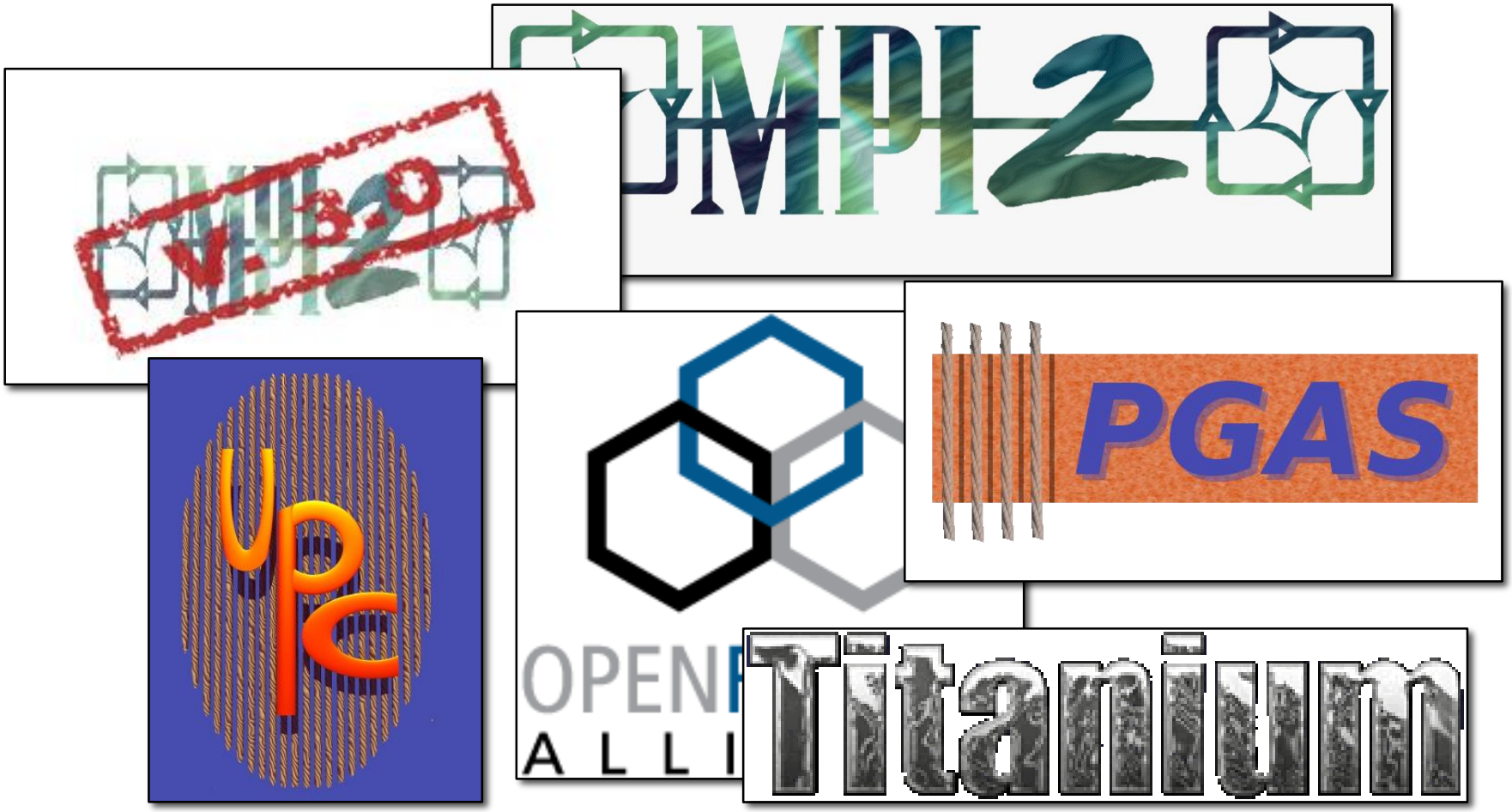

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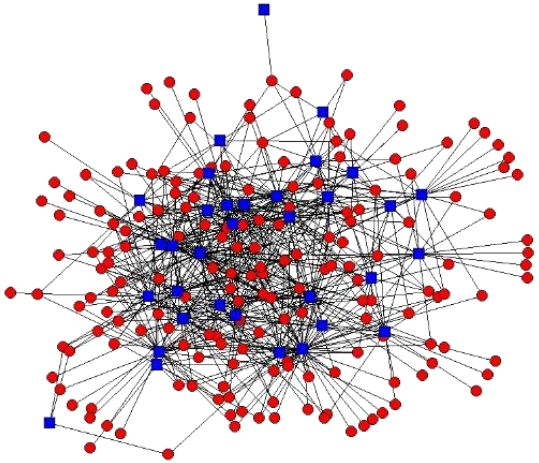

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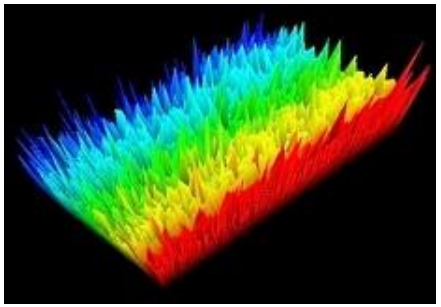

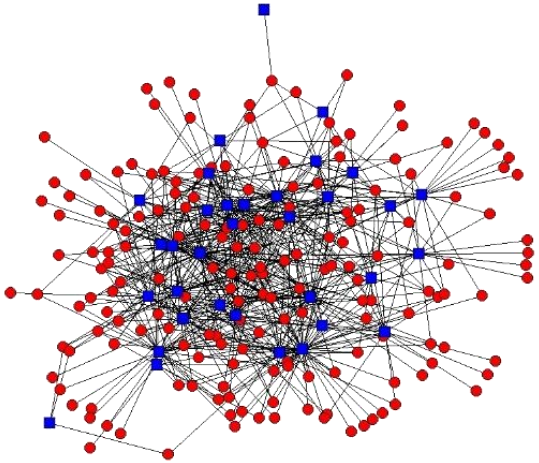

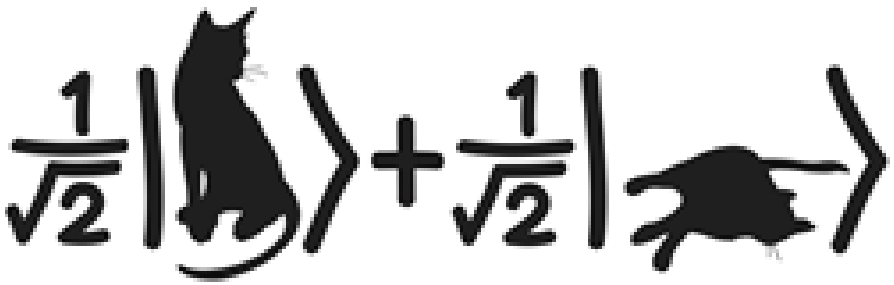

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FAULT TOLERANCE + RMA

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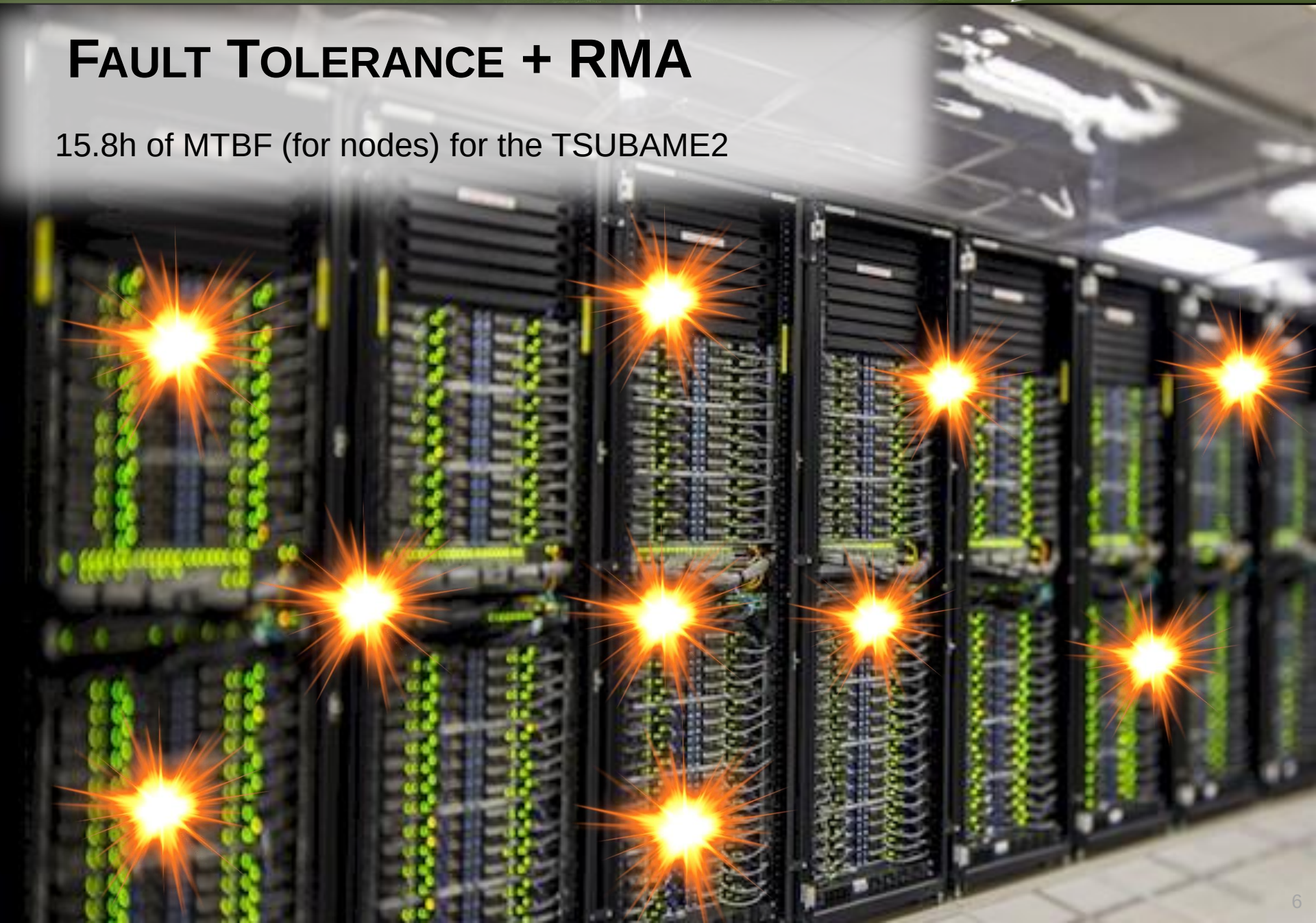
15.8h of MTBF (for nodes) for the TSUBAME2



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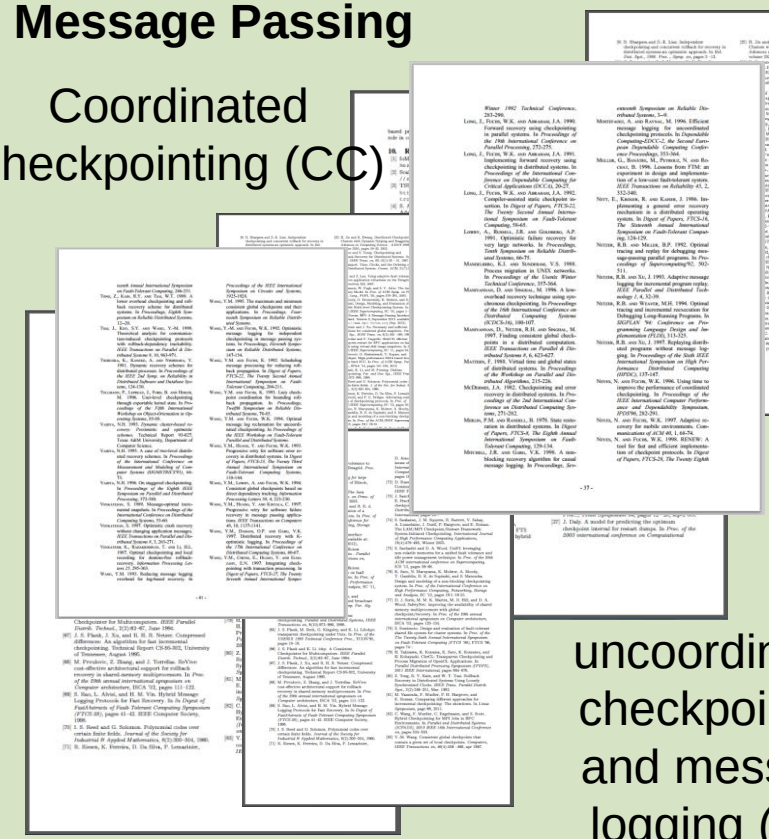

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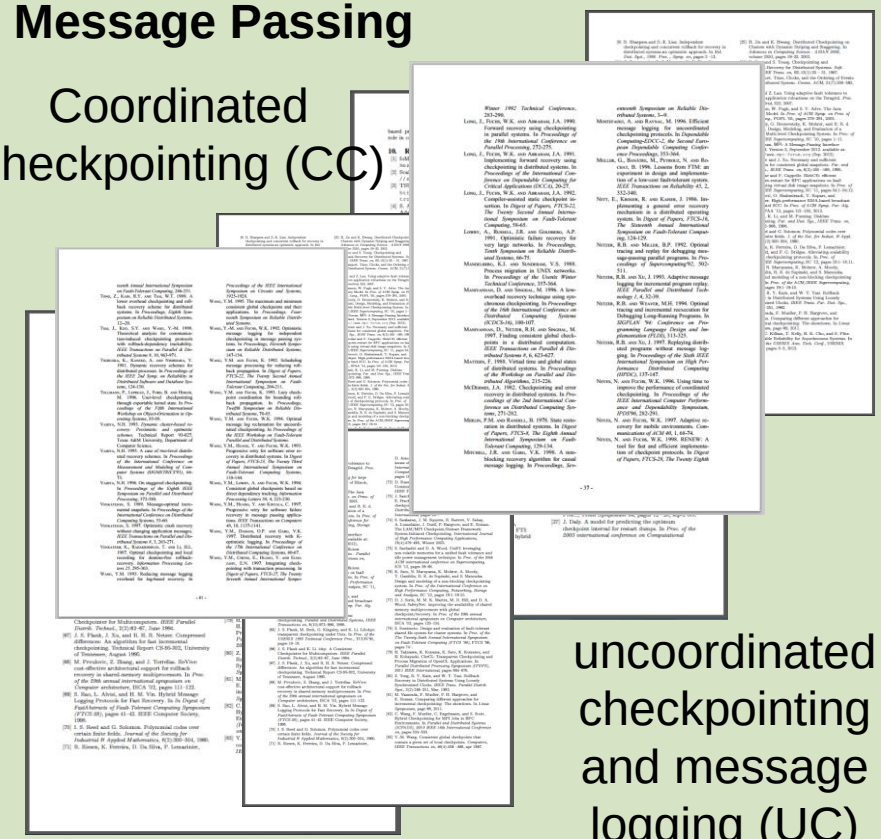

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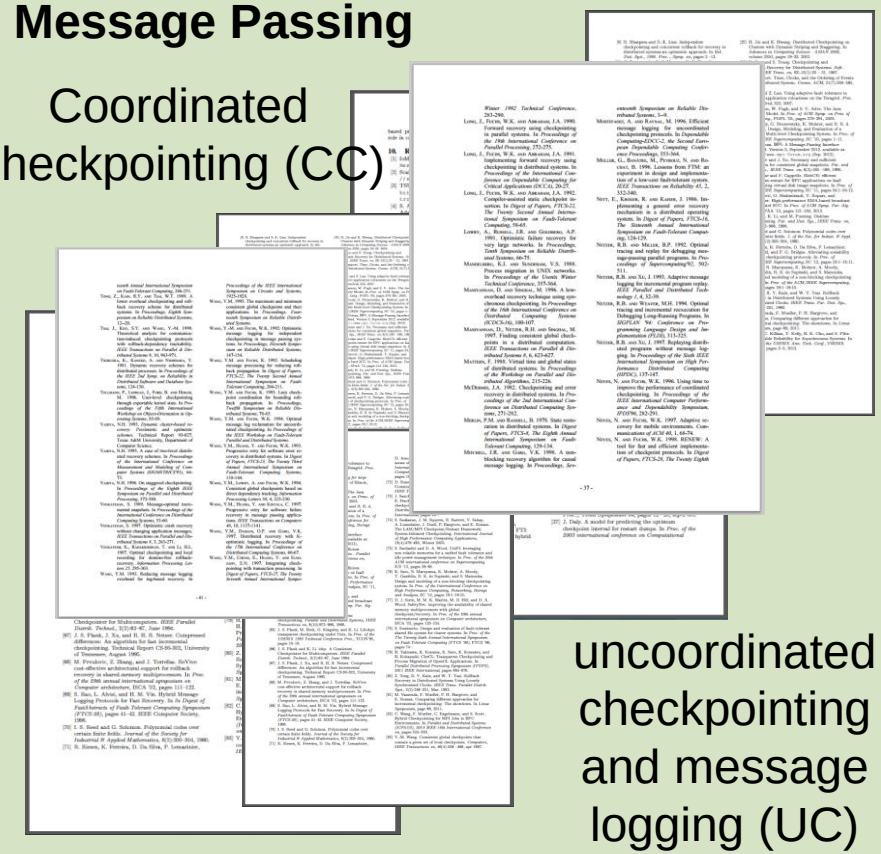

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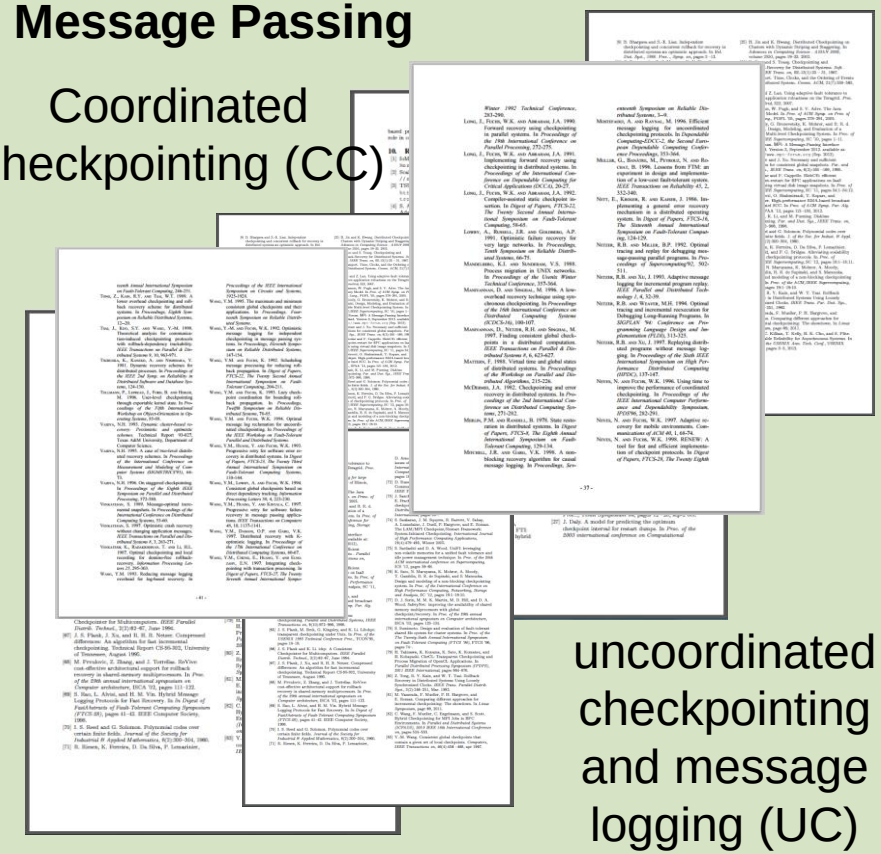

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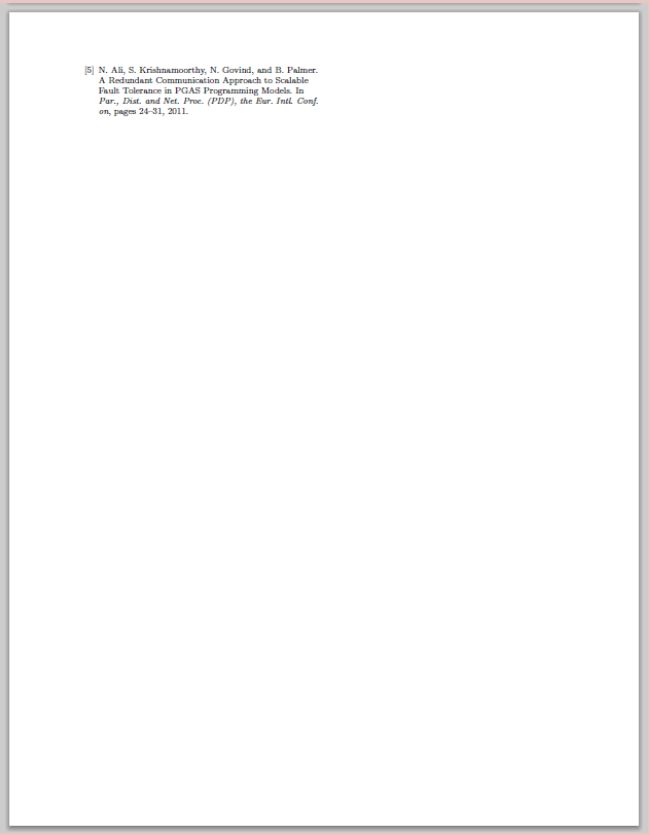

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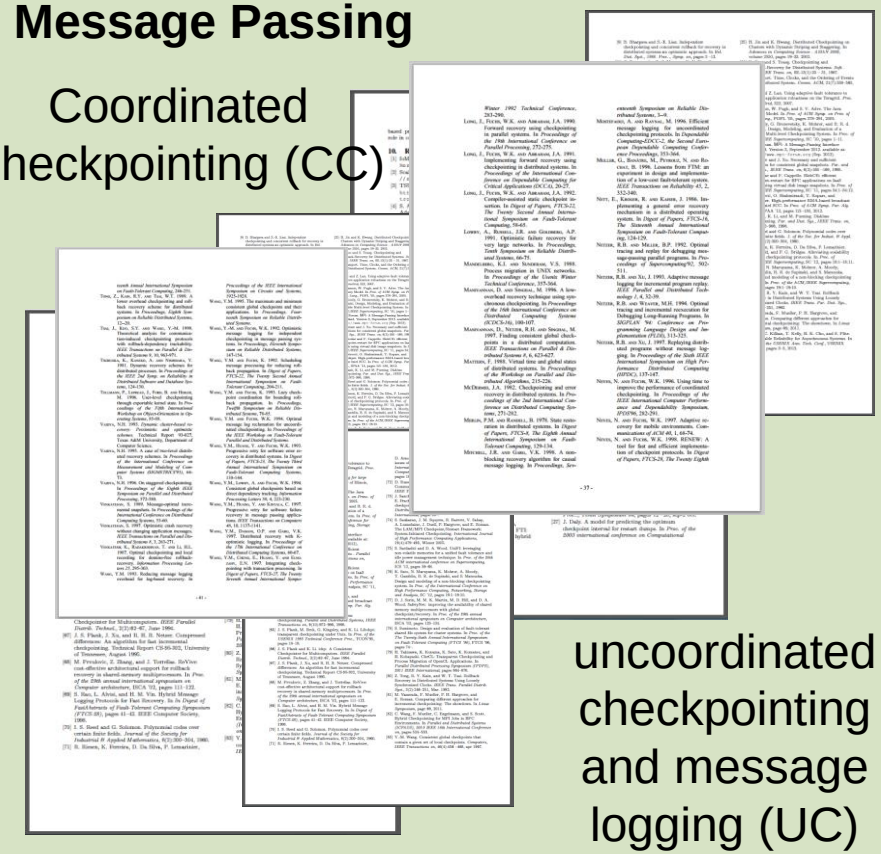

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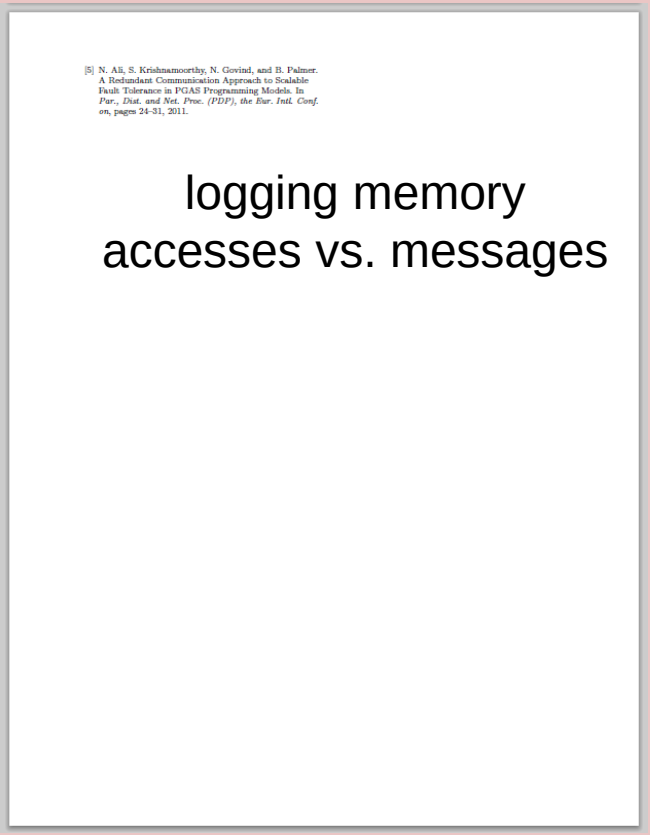

logging memory accesses vs. messages

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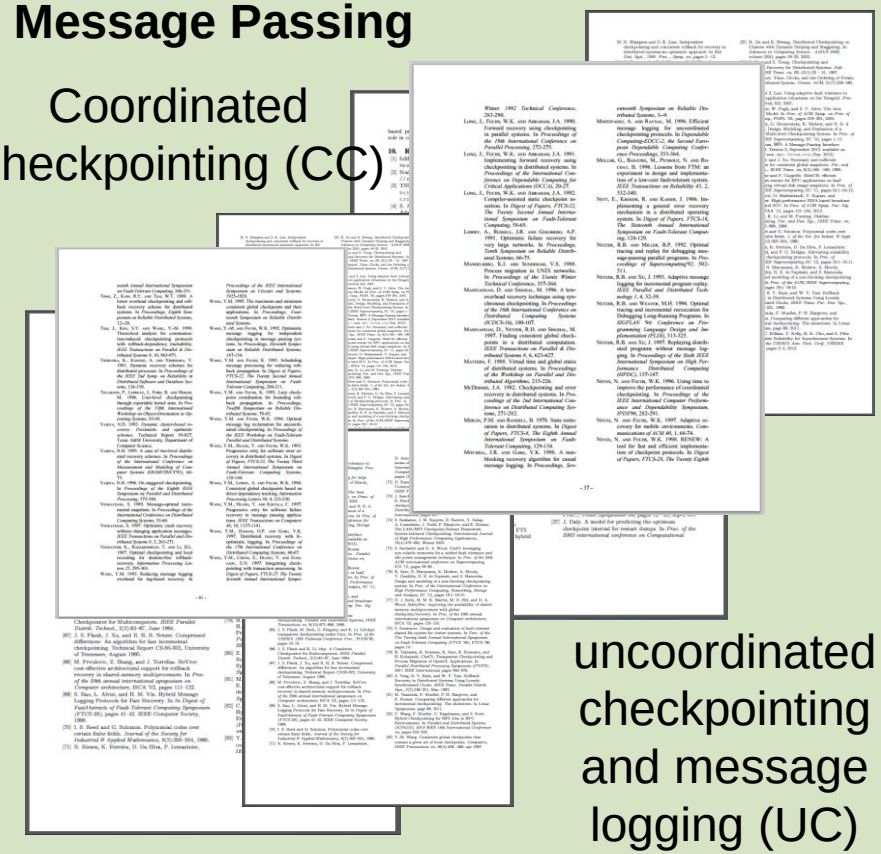

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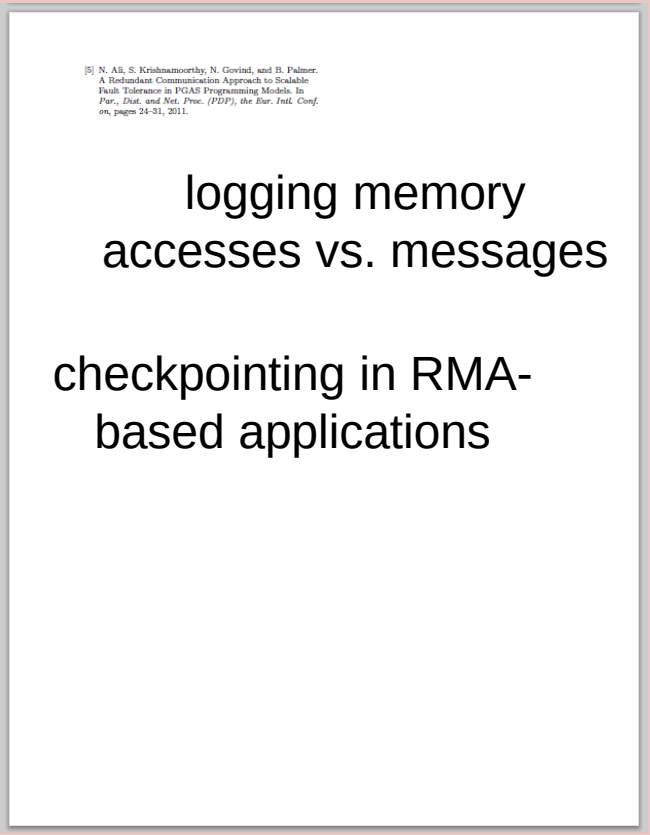

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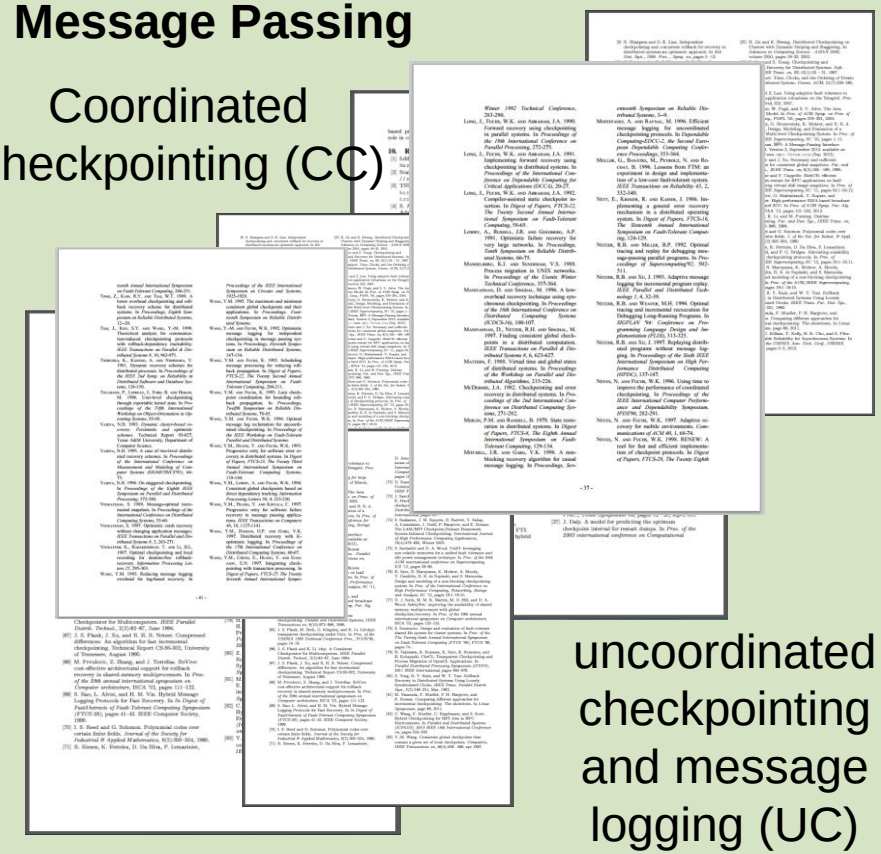

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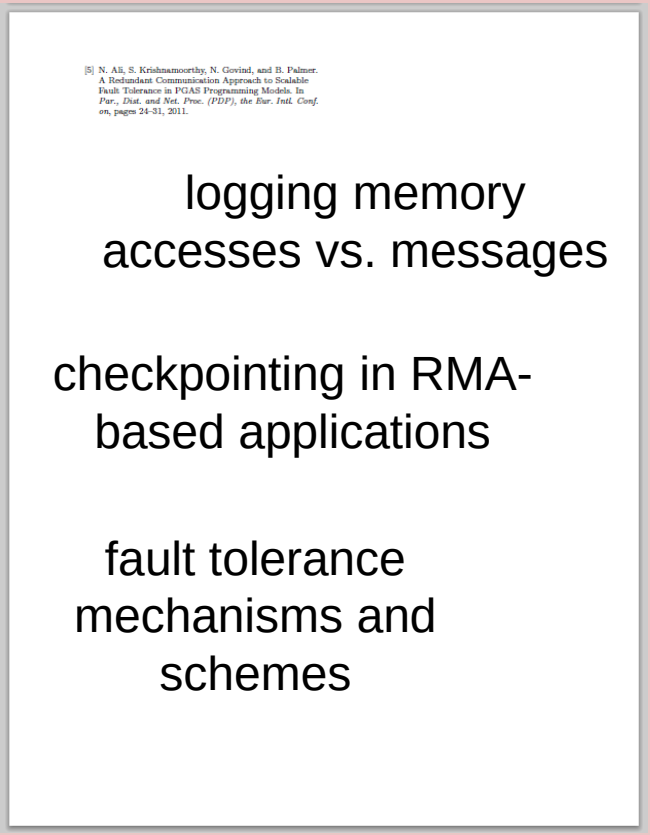

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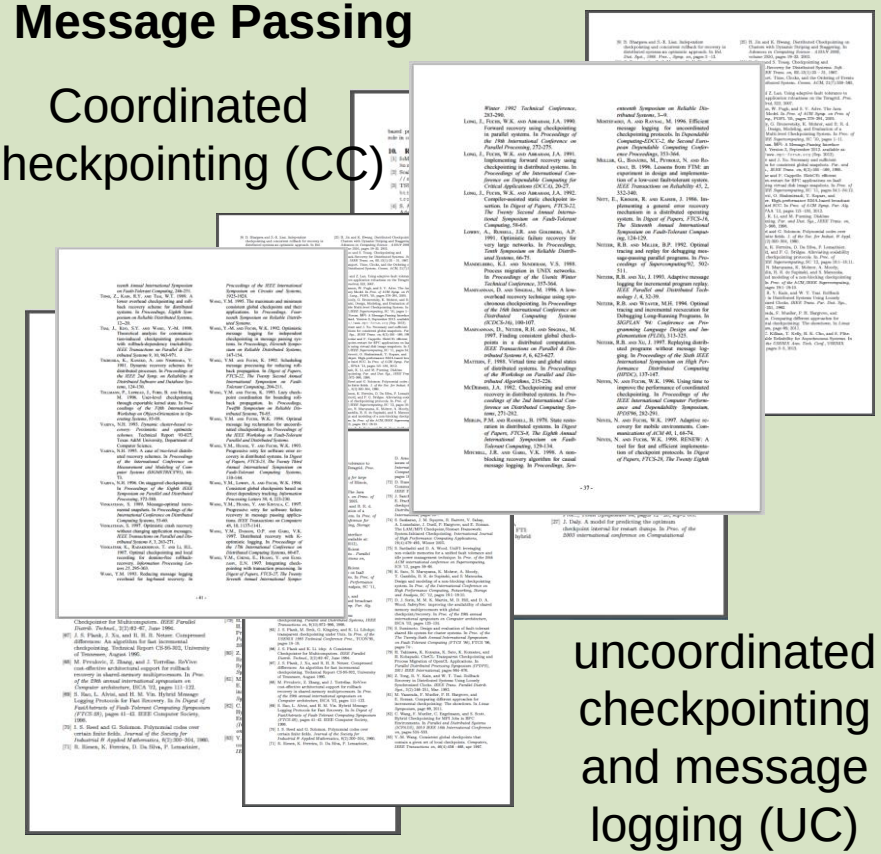

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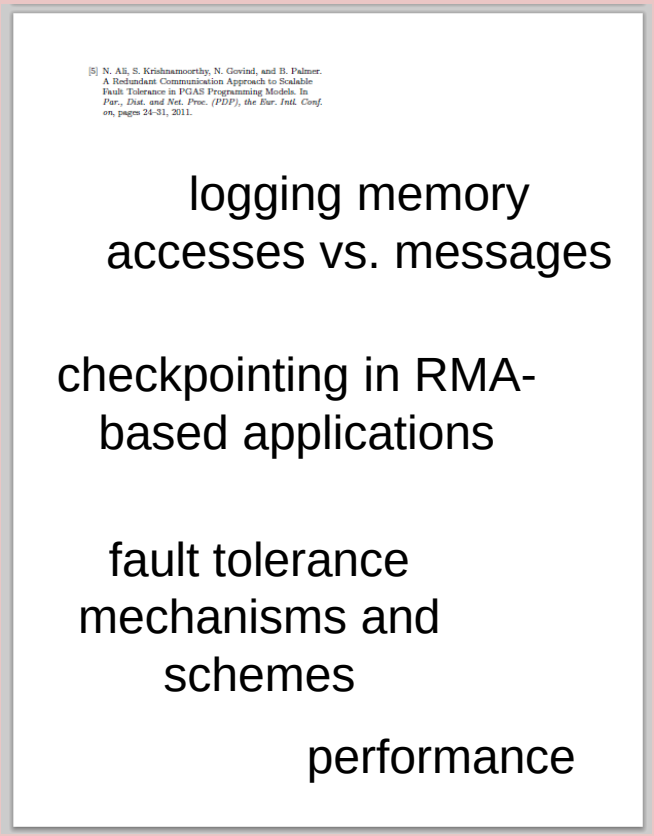

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Overview of our Research

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Generic model

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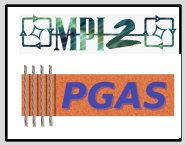

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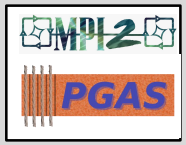

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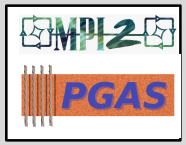

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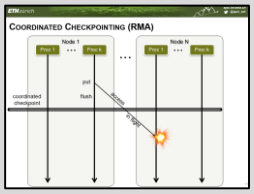

MP vs. RMA

Overview of our Research

Generic model

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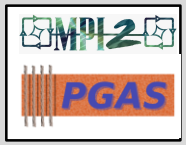

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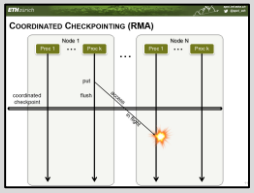

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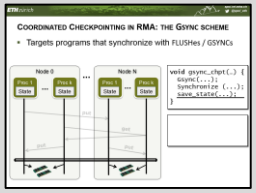

Schemes

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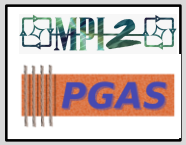

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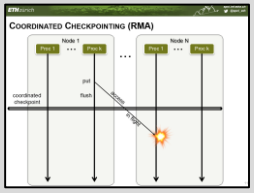

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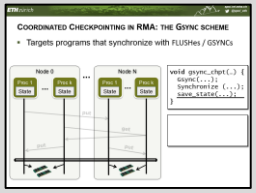

Schemes

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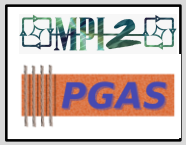

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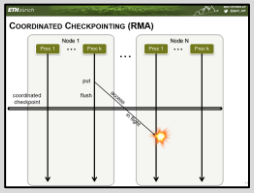

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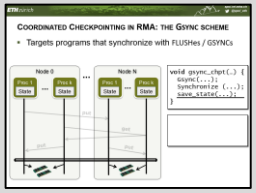

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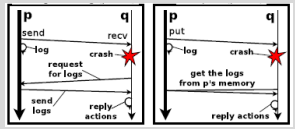

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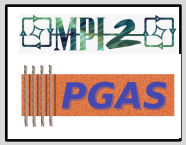

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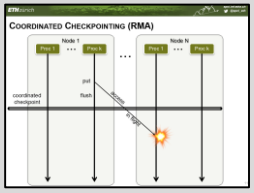

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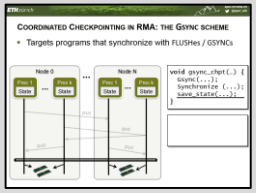

Schemes

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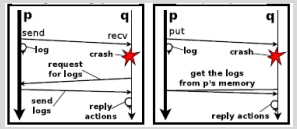

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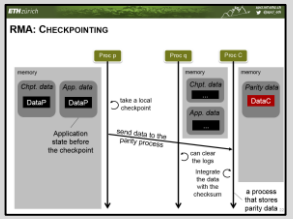

Checkpointing schemes

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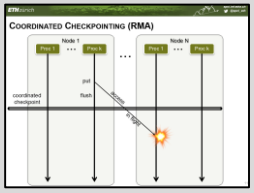
MPI-2
PGAS

CC in RMA



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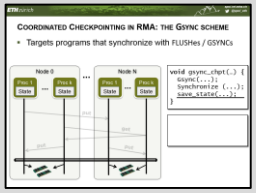
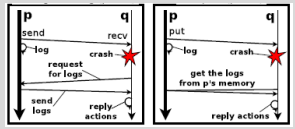
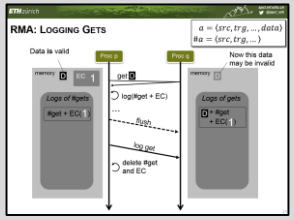


Schemes

UC in RMA



MP vs. RMA



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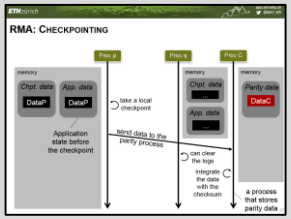

Checkpointing schemes

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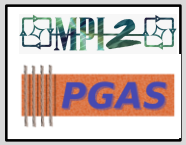

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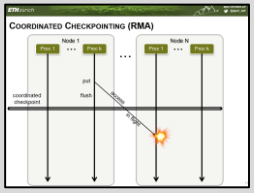
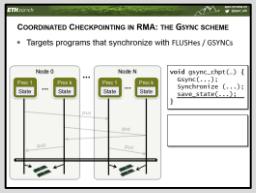


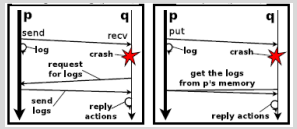
MP vs. RMA



Schemes

Recovery in RMA

UC in RMA



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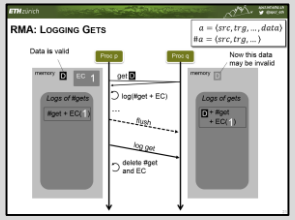
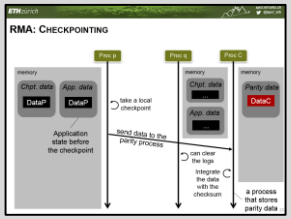


Logging accesses



Checkpointing schemes

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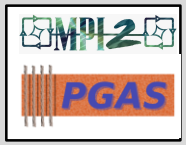

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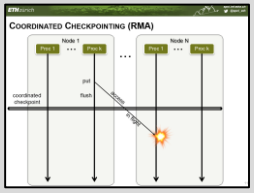

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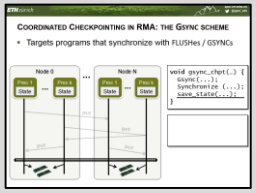

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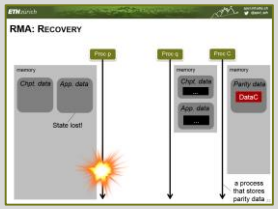
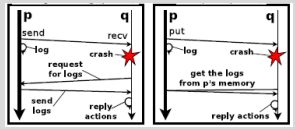


Basic scheme

UC in RMA



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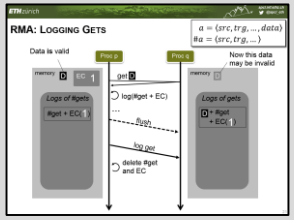

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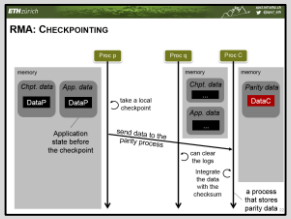

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MPI-2
PGAS

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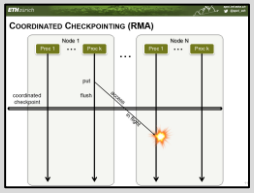

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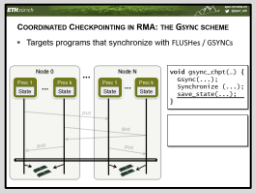

Schemes

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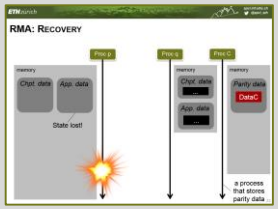
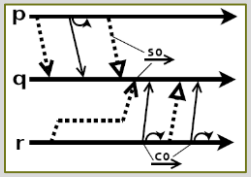


Basic scheme

Extended RMA semantics



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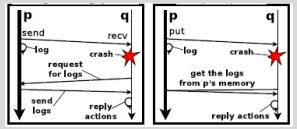

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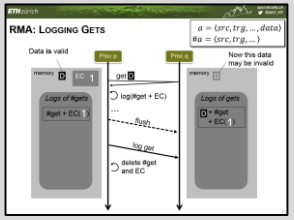

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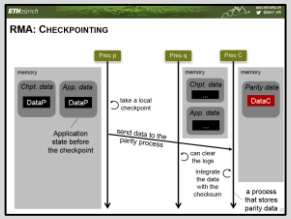

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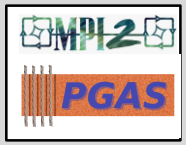

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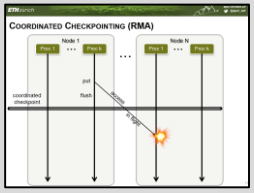
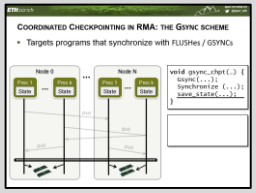


MP vs. RMA



Schemes

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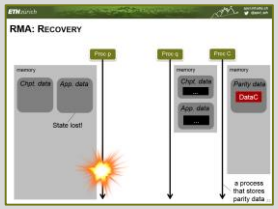

Basic scheme

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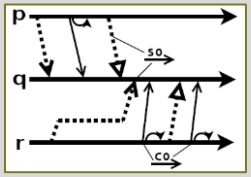

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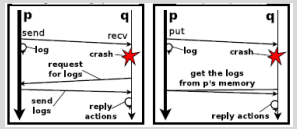

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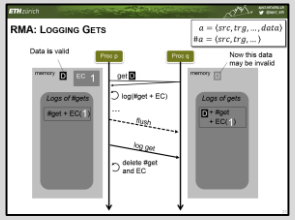
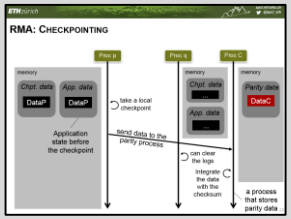


Logging accesses



Checkpointing schemes

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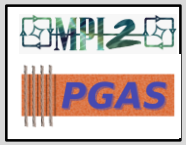
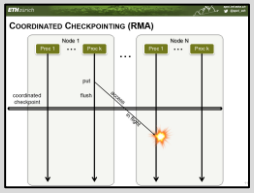


CC in RMA



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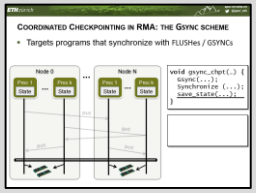

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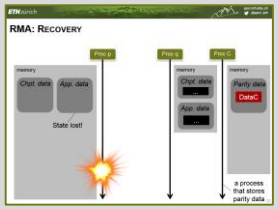

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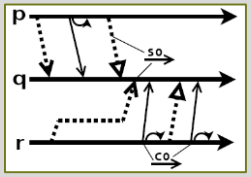
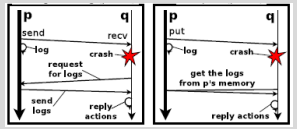


UC in RMA



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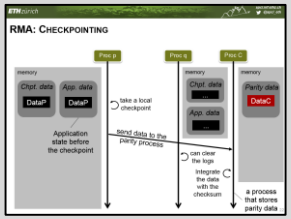
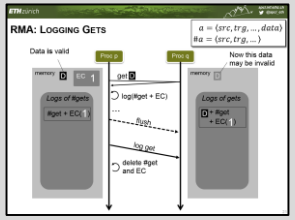


Checkpointing schemes



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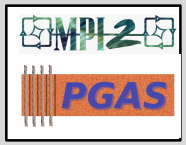
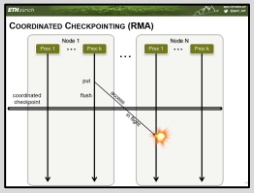


CC in RMA



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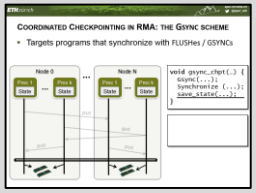

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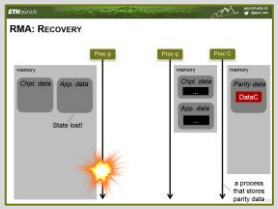
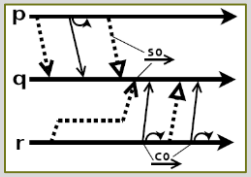


Basic scheme

Extended RMA semantics



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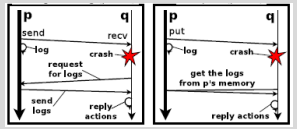

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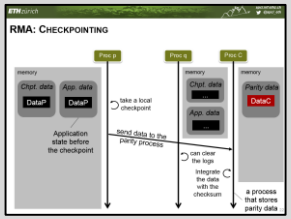
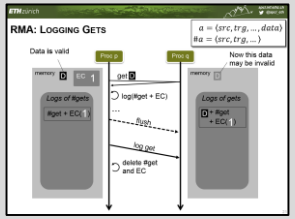


Checkpointing schemes



Logging accesses

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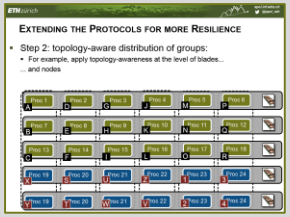
Model extensions



Distribution of processes

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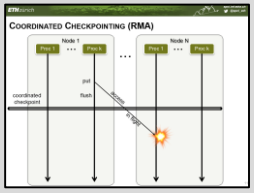
MPI-2 PGAS

CC in RMA



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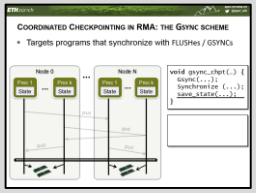

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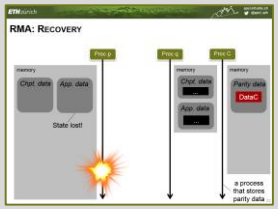

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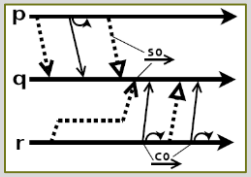
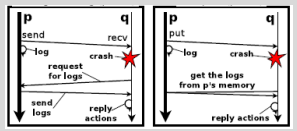


UC in RMA



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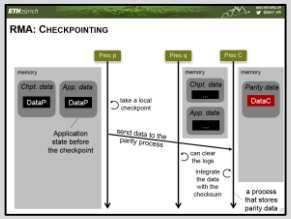

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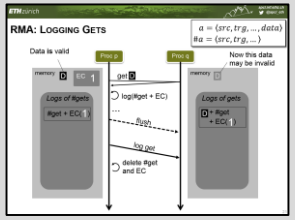

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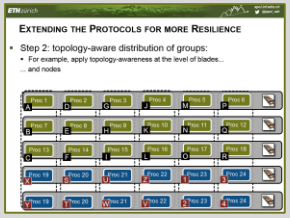
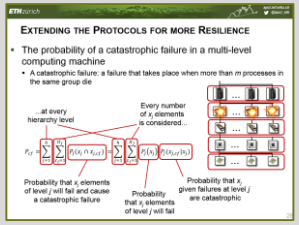
Model extensions



Distribution of processes



Decreasing failure prob.

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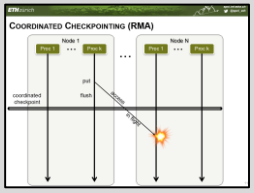
MPI-2 PGAS

CC in RMA



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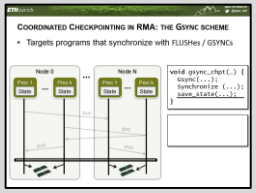

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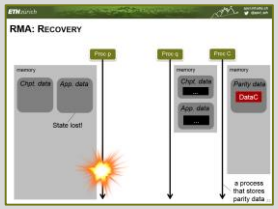

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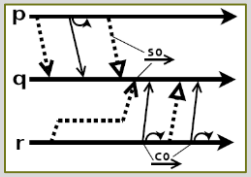
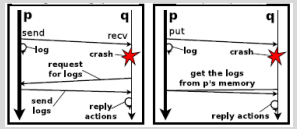


Holistic fault-tolerance library

UC in RMA



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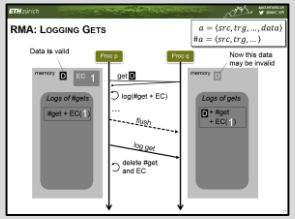

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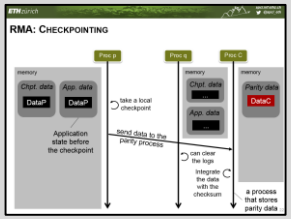

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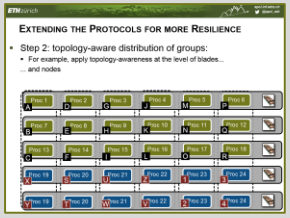

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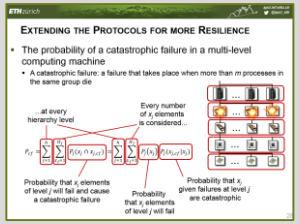

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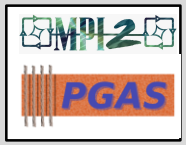
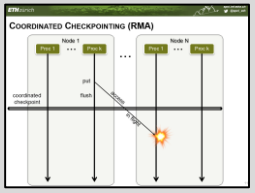


CC in RMA



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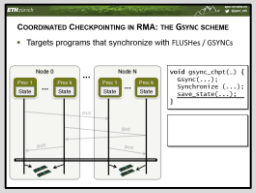

Schemes

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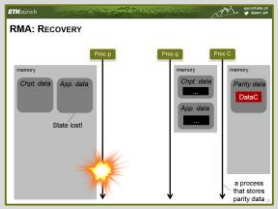

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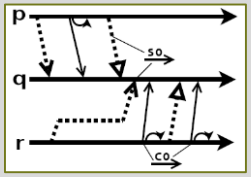

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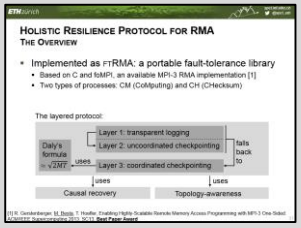

Design

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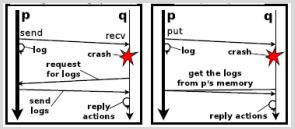

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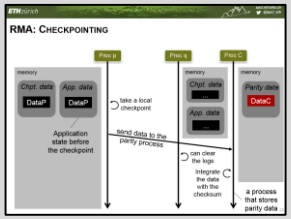

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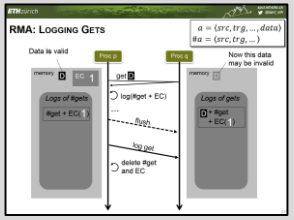

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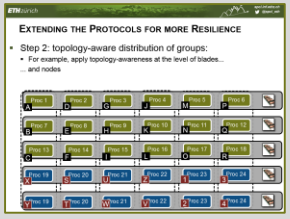
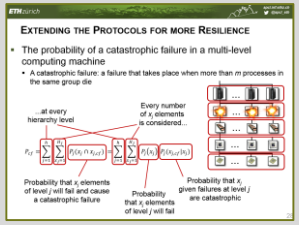
Model extensions



Distribution of processes



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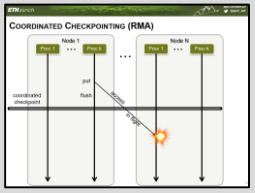

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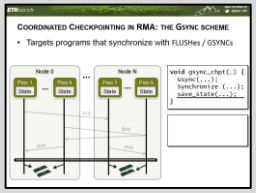

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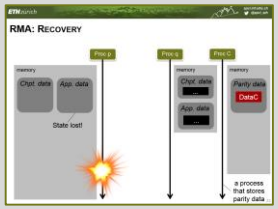

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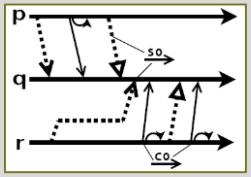

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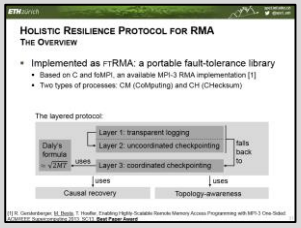

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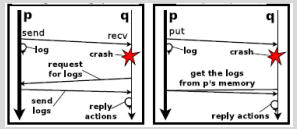

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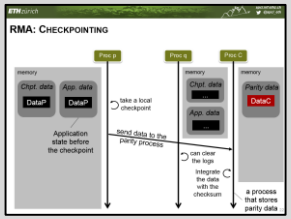

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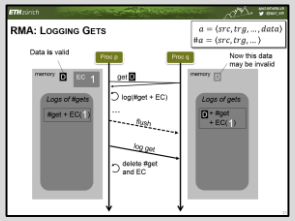

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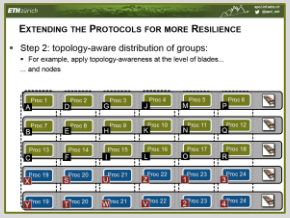

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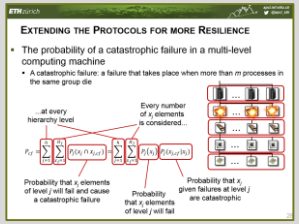

Decreasing failure prob.

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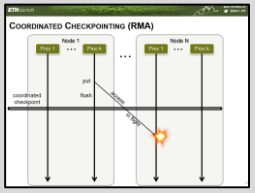

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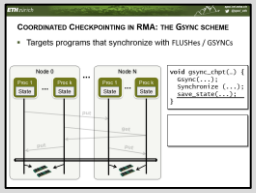

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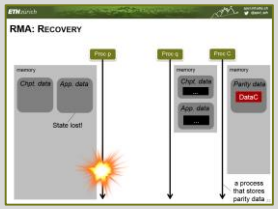

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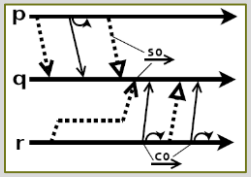

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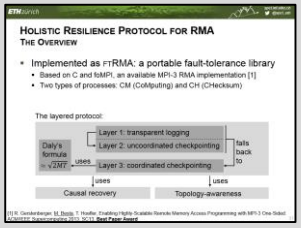

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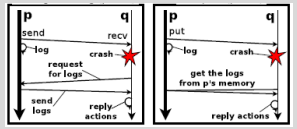

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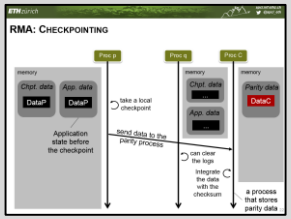

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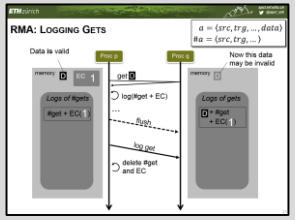

Logging accesses

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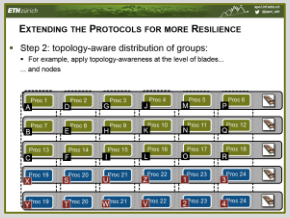
Model extensions



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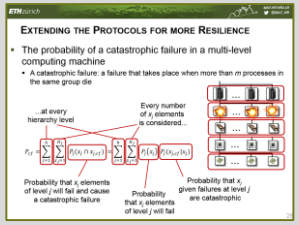

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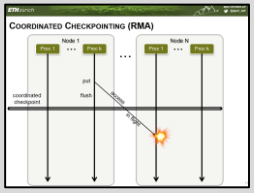

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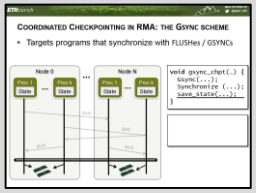

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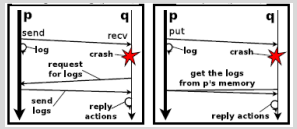

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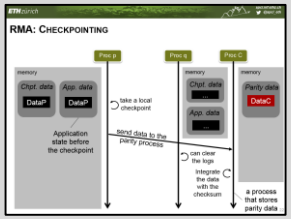

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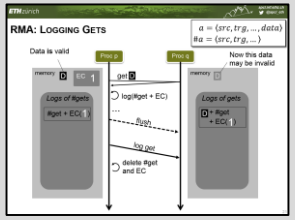

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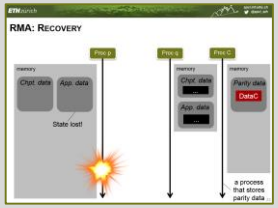

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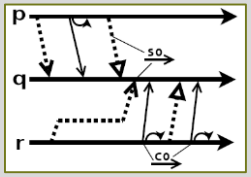

Proofs

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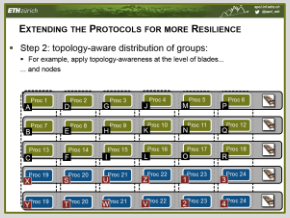

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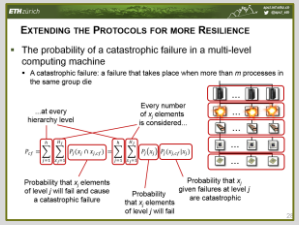

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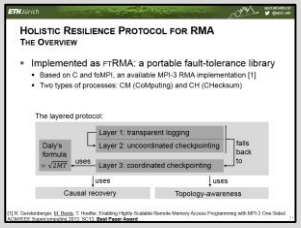

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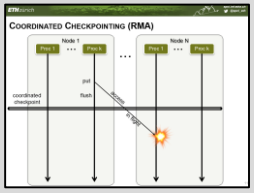

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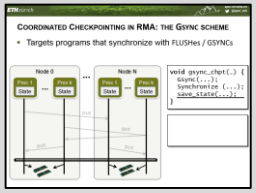

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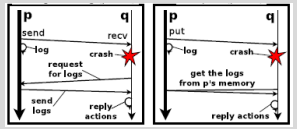

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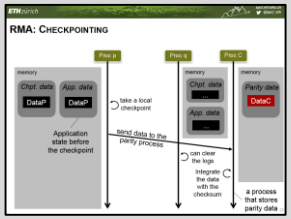

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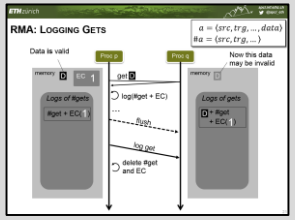
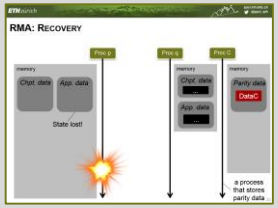


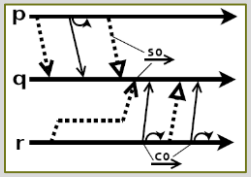
Logging accesses

Recovery in RMA



Basic scheme

Extended RMA semantics



Proofs

Theorem 4.2. *The recovery algorithm 2 preserves the* $\xrightarrow{cohb}$ *order (referred to as the* gsync order*).*

Deadlock freedom
Correct recovery

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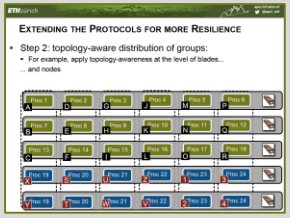
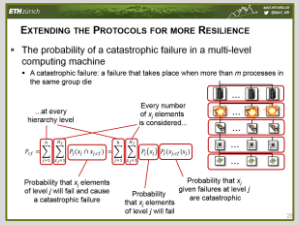
$$\langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \mathcal{H}, \mathcal{G}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co}, \mathcal{M} \rangle$$

Model extensions

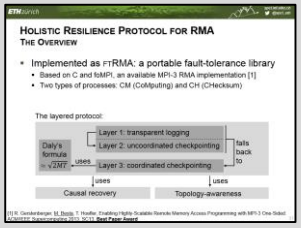


Distribution of processes



Decreasing failure prob.

Holistic fault-tolerance library



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$$\mathcal{D} = \langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co} \rangle,$$

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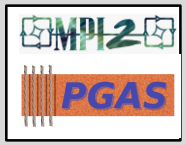

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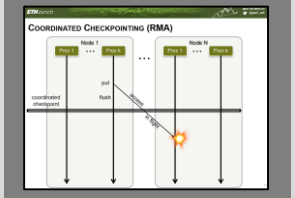
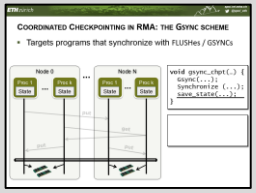
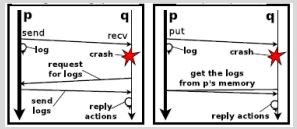


MP vs. RMA



Schemes

UC in RMA



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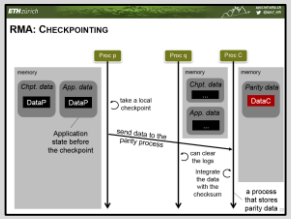

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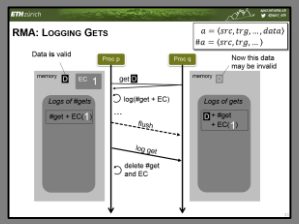

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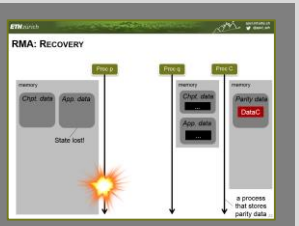

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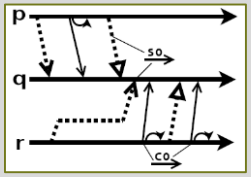

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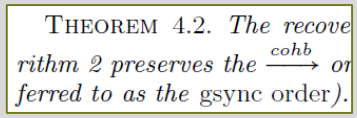

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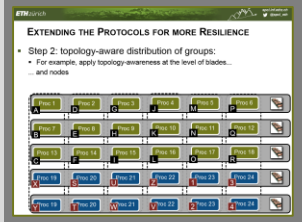

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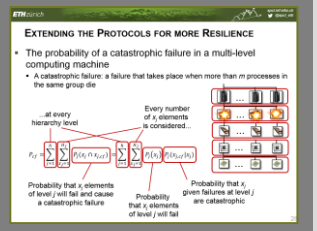

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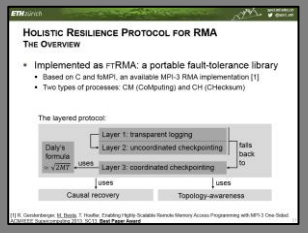

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MPI-2 PGAS

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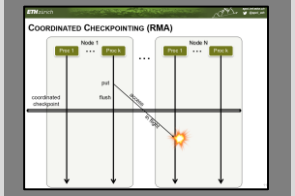

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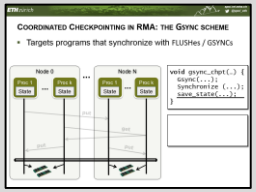

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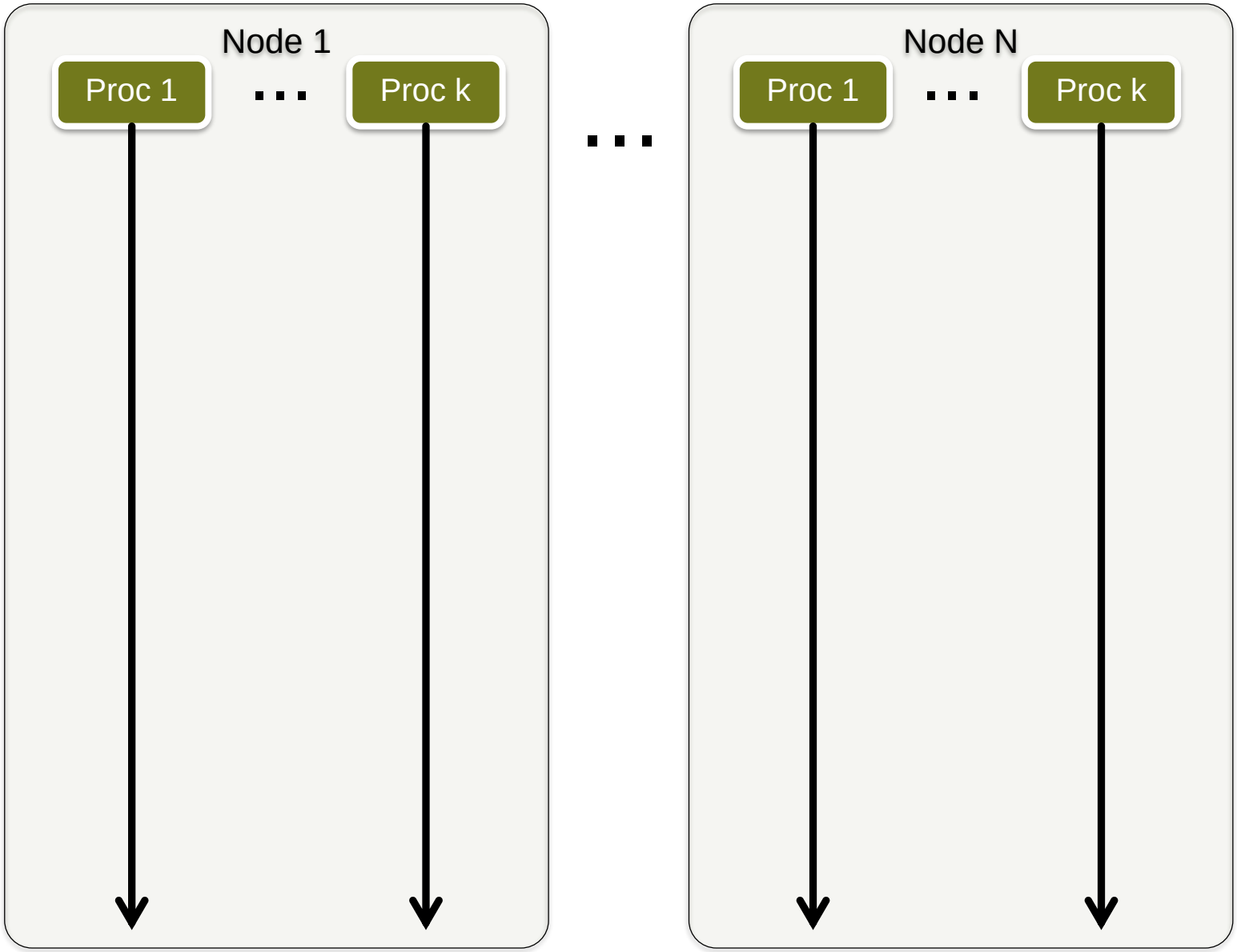

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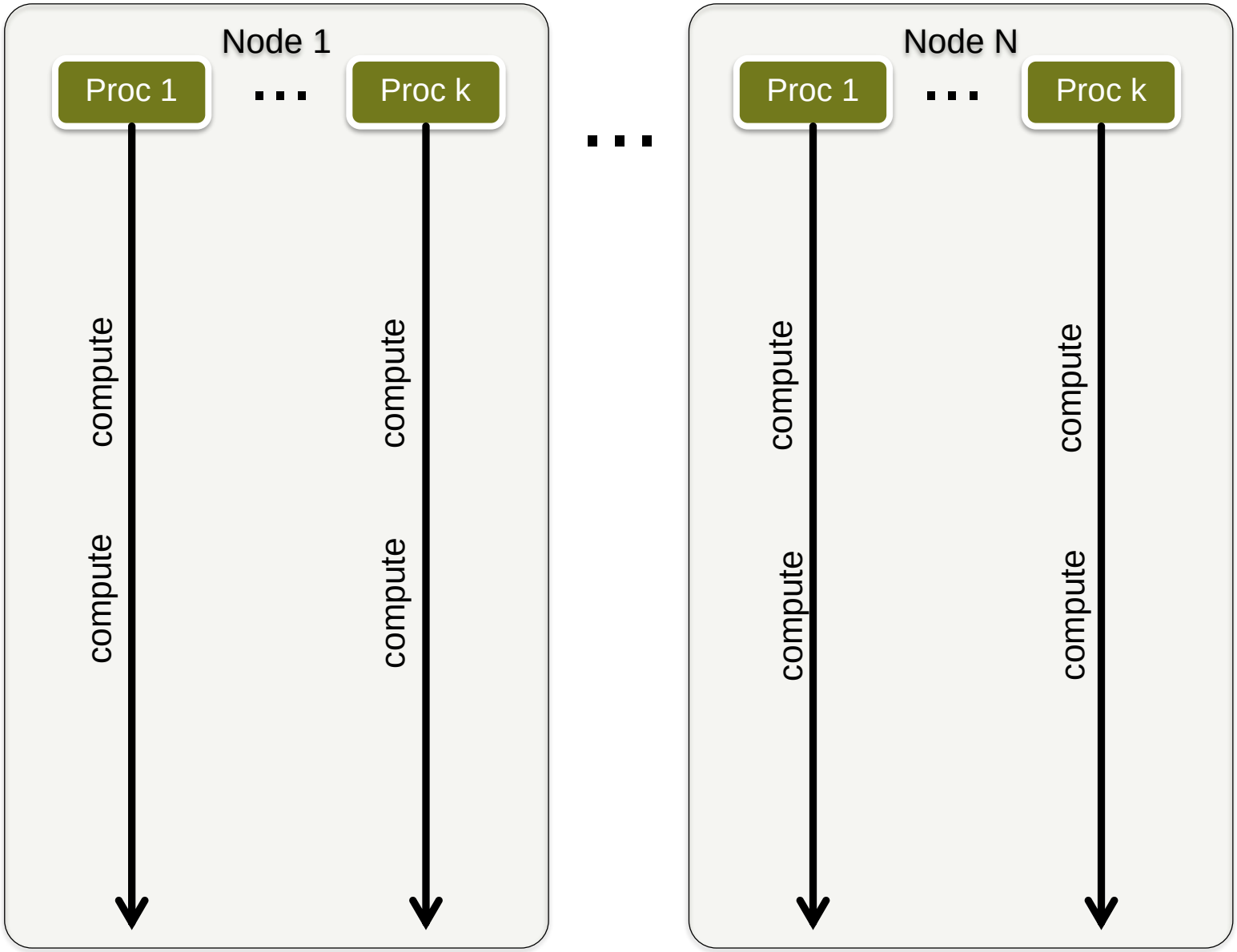

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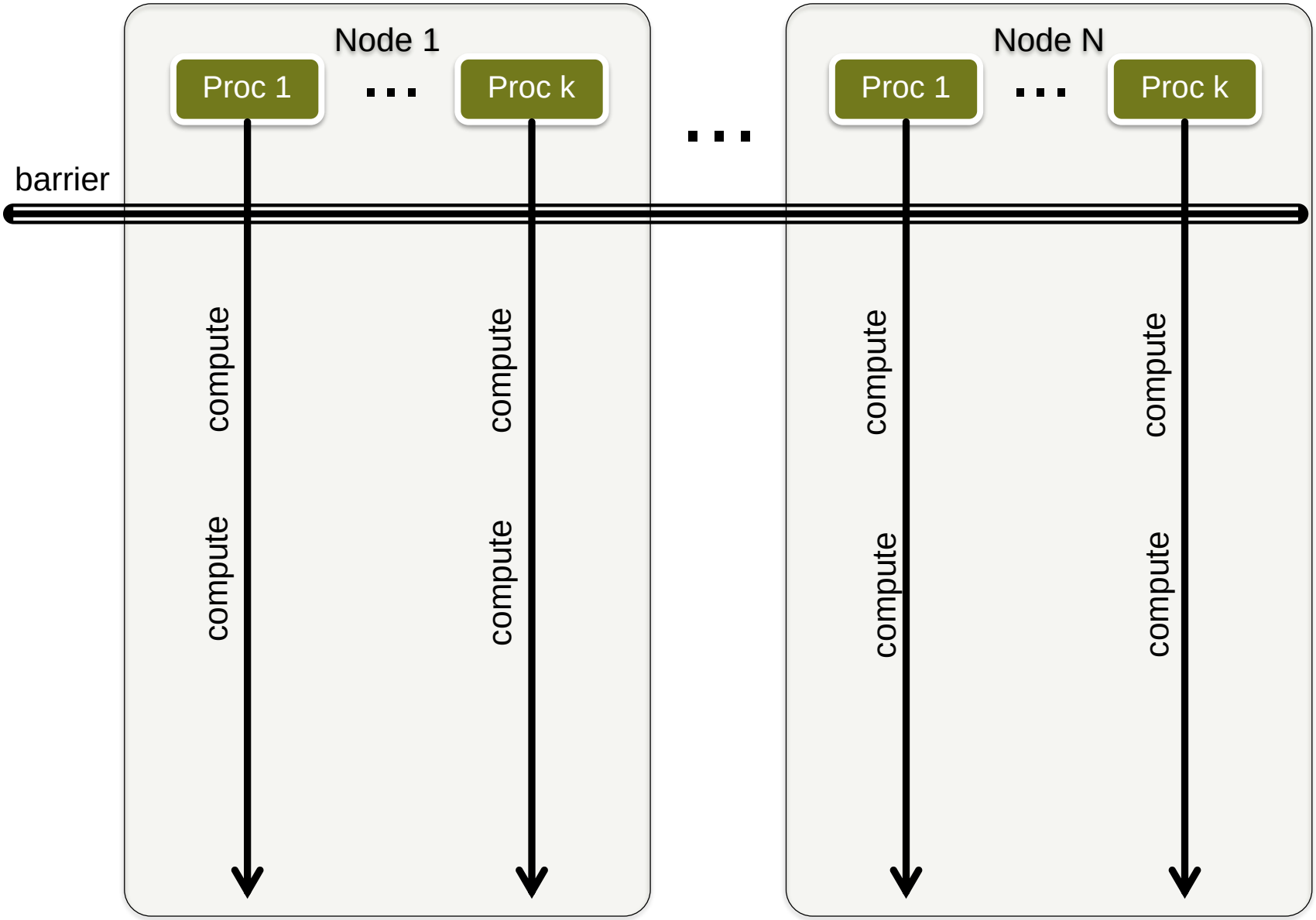

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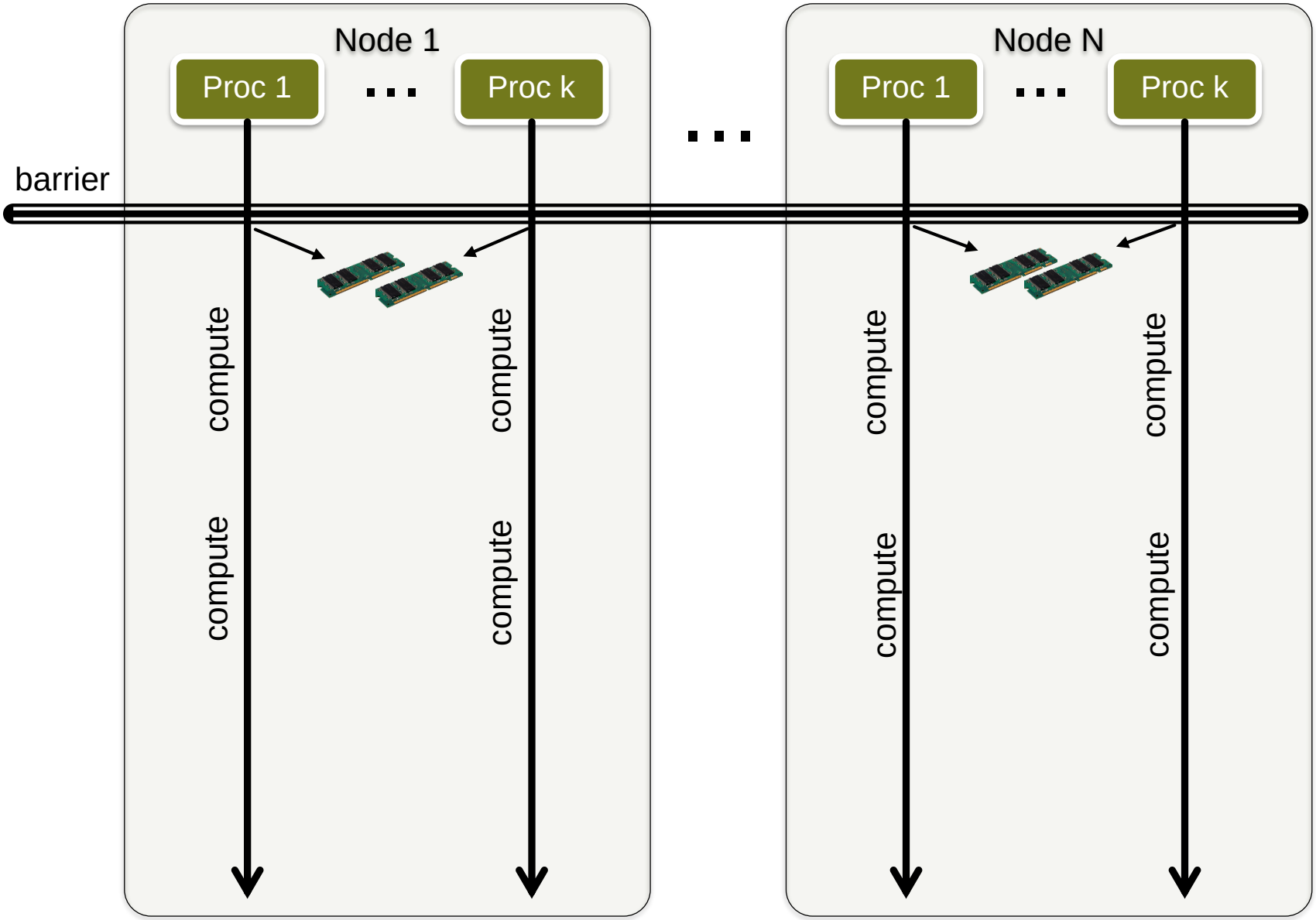

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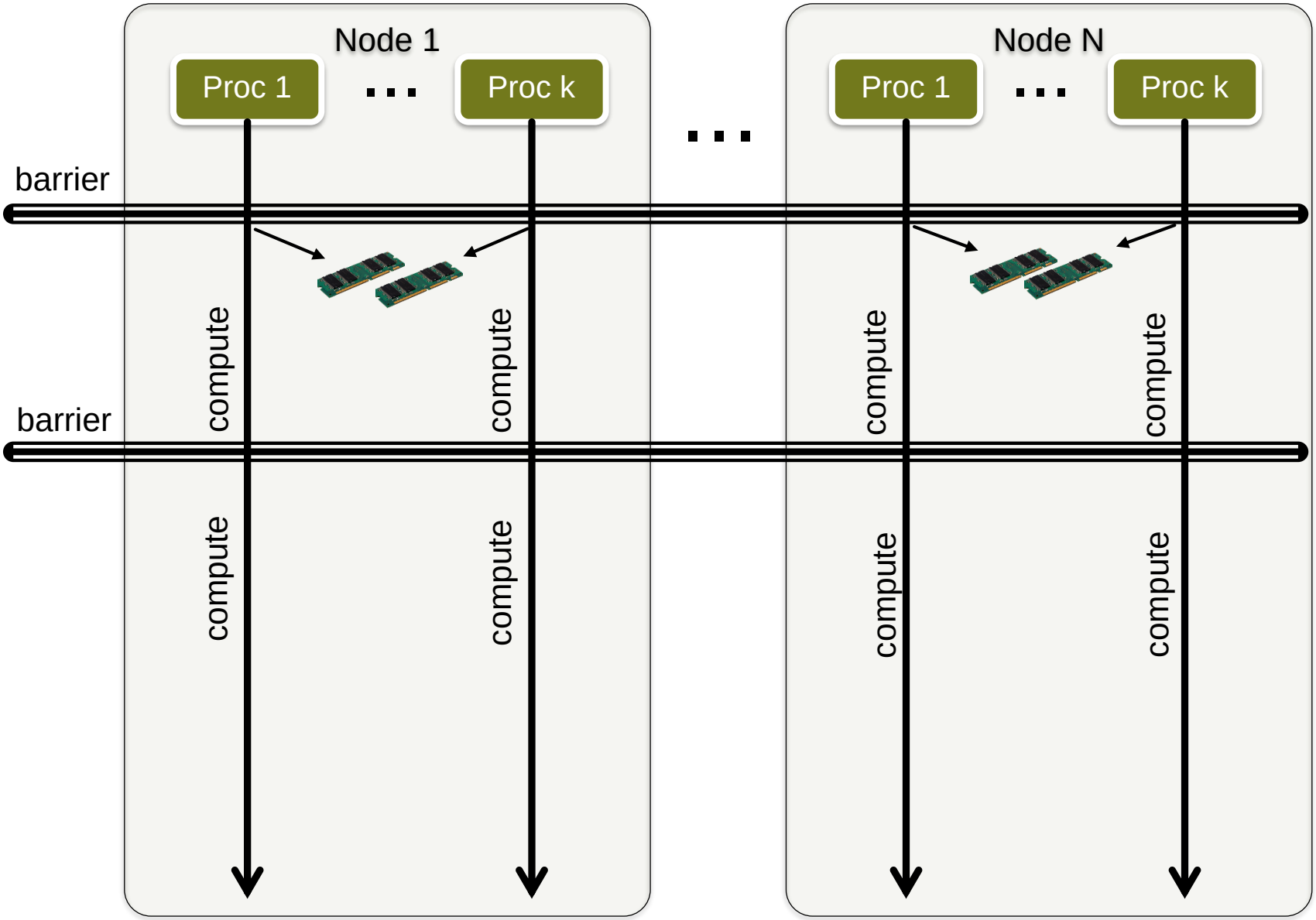

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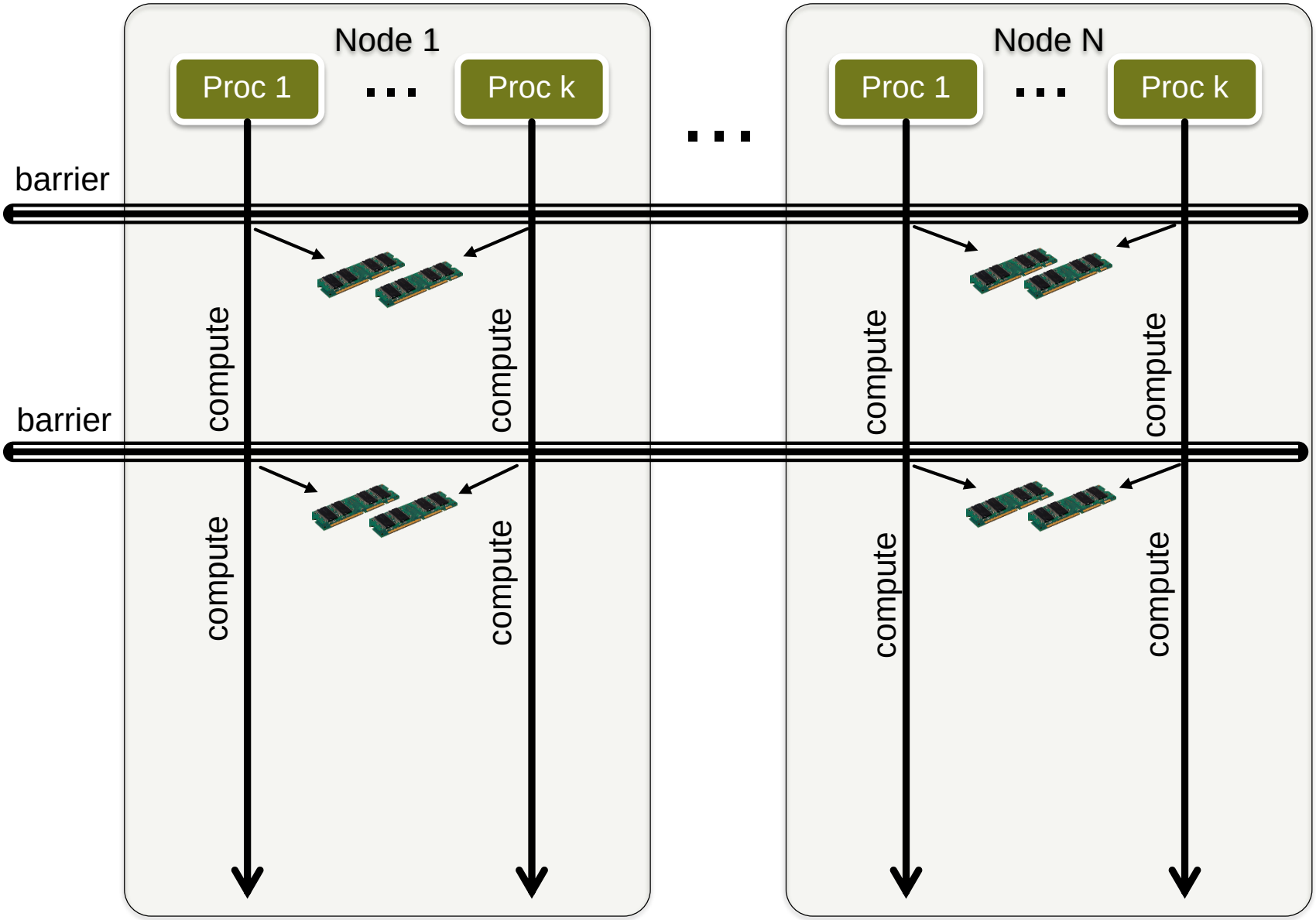

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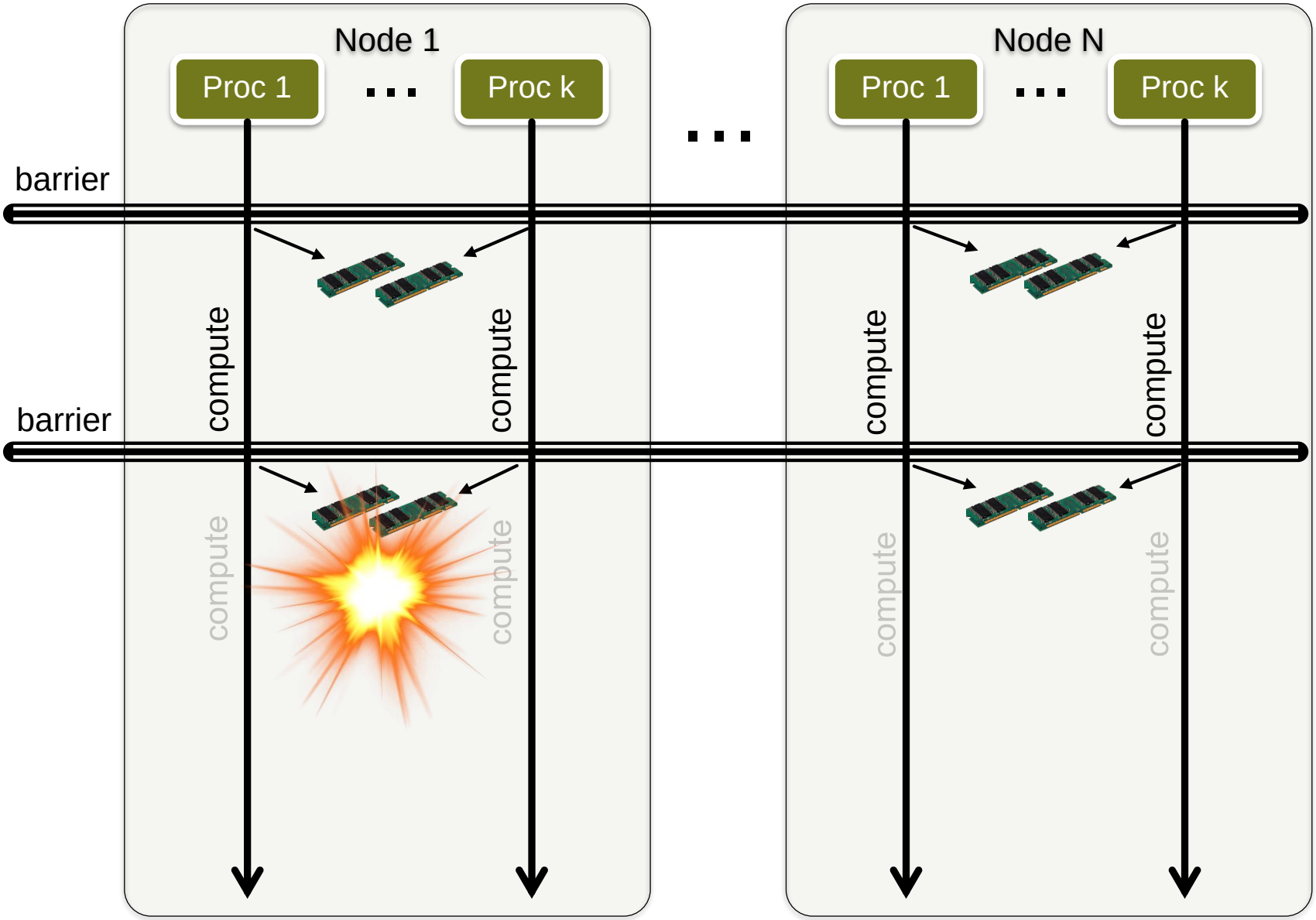

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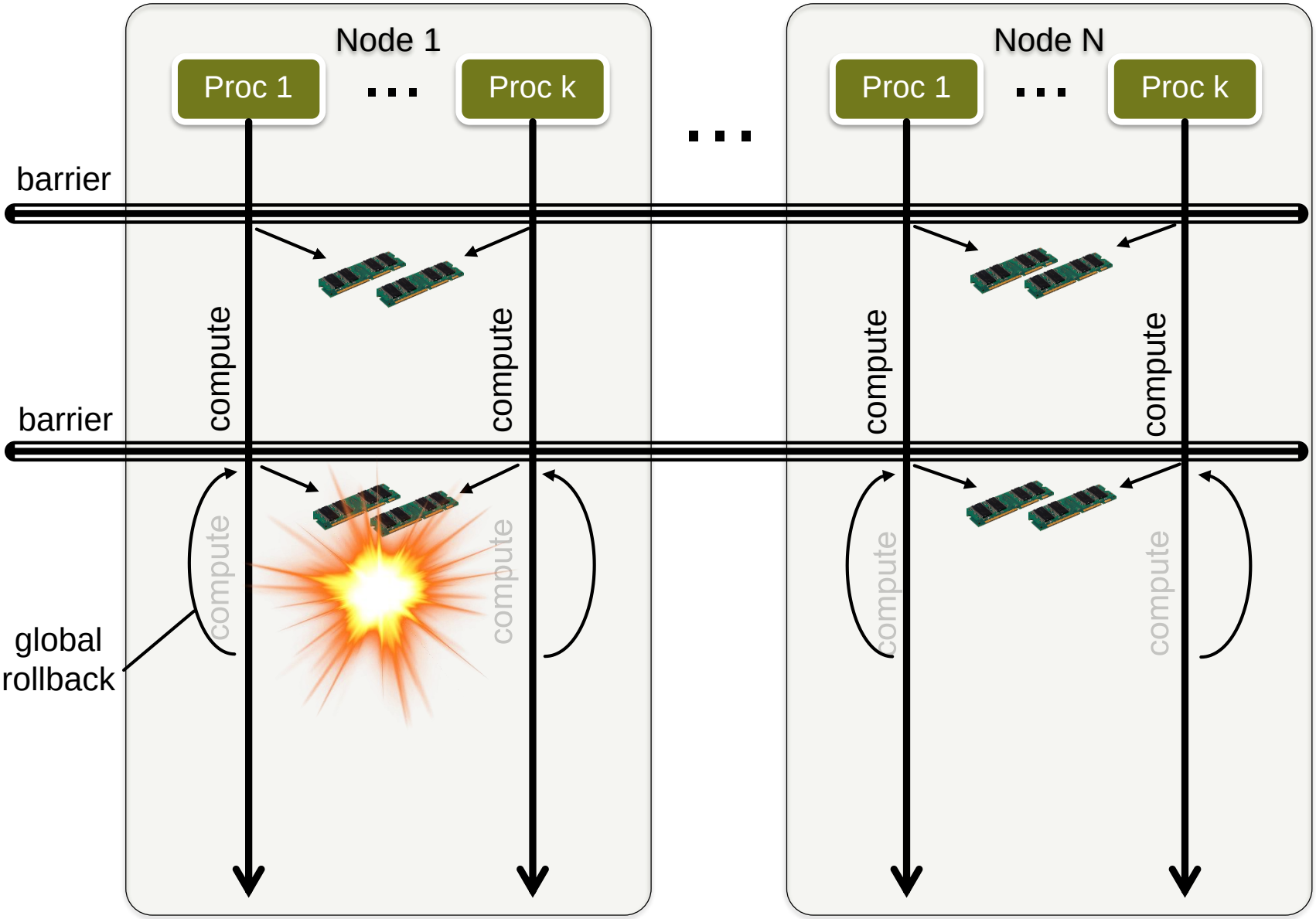

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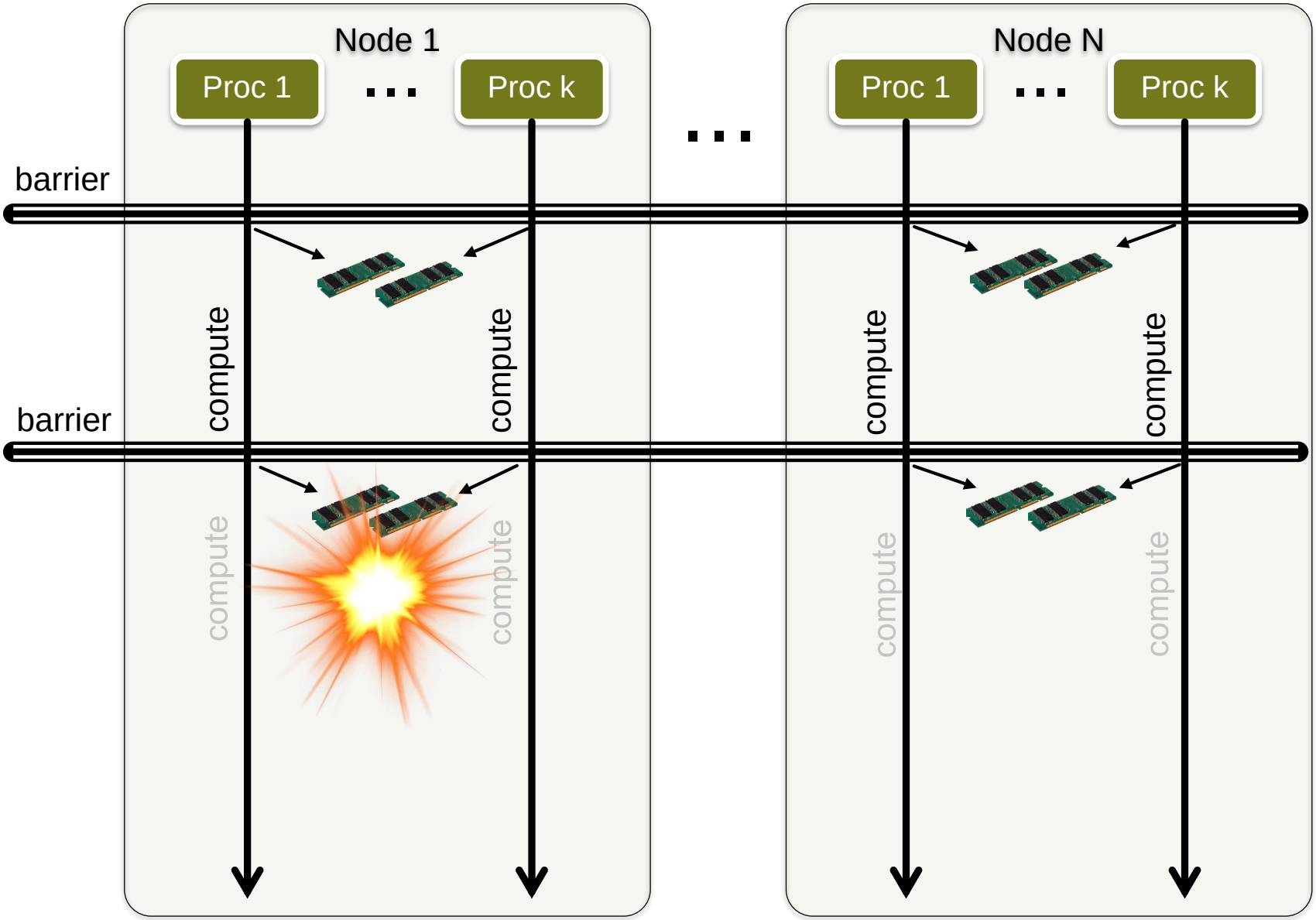

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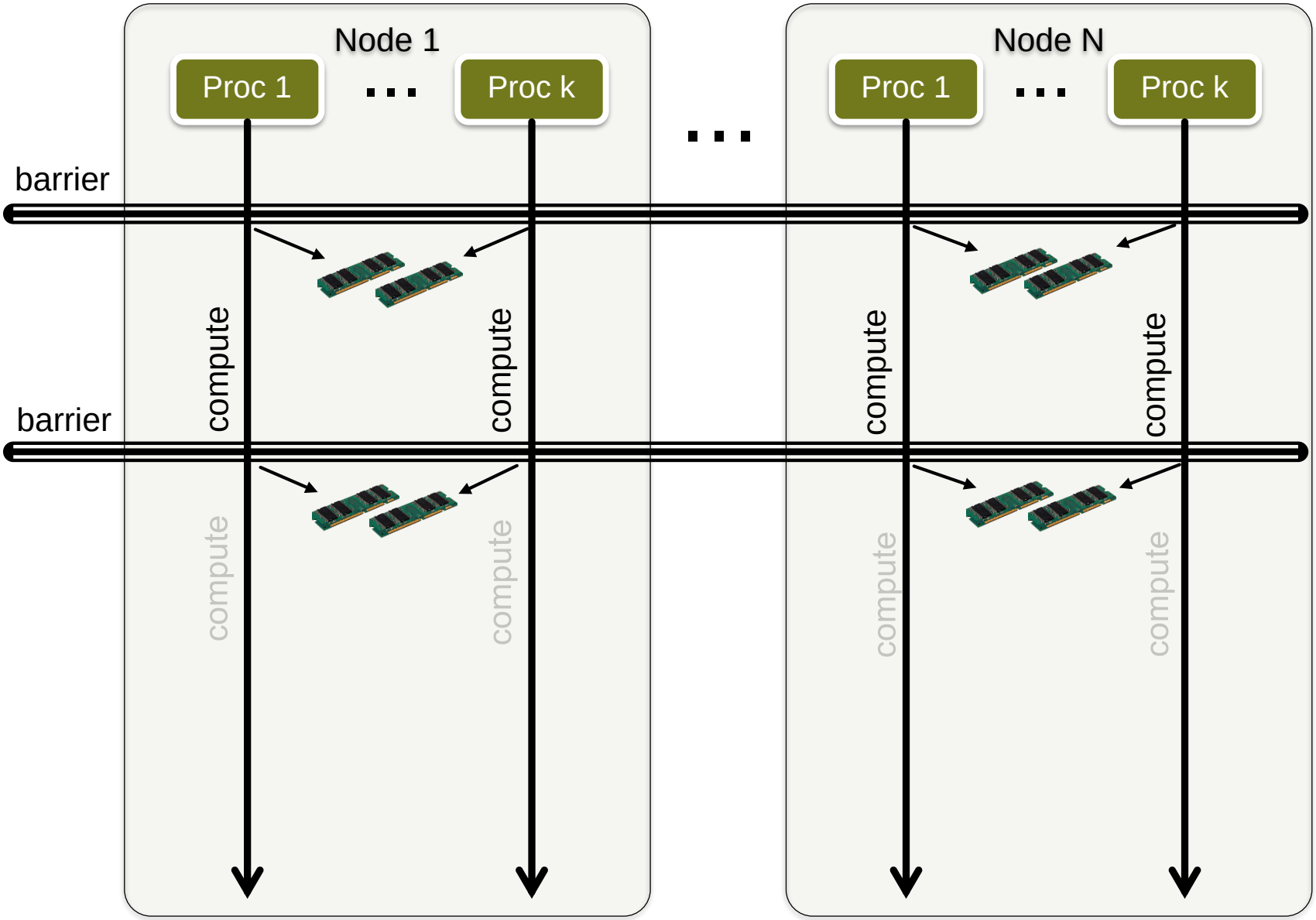

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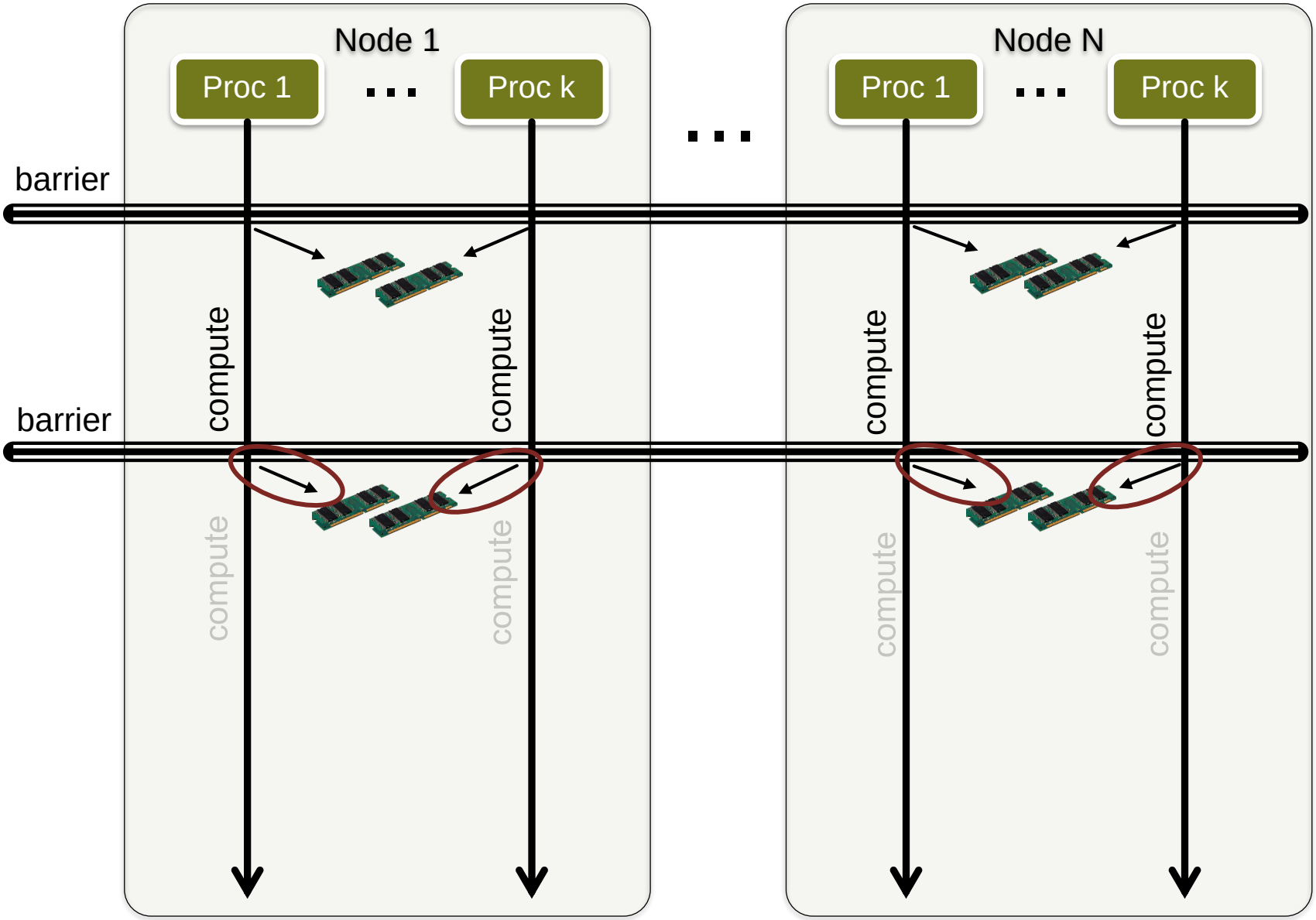

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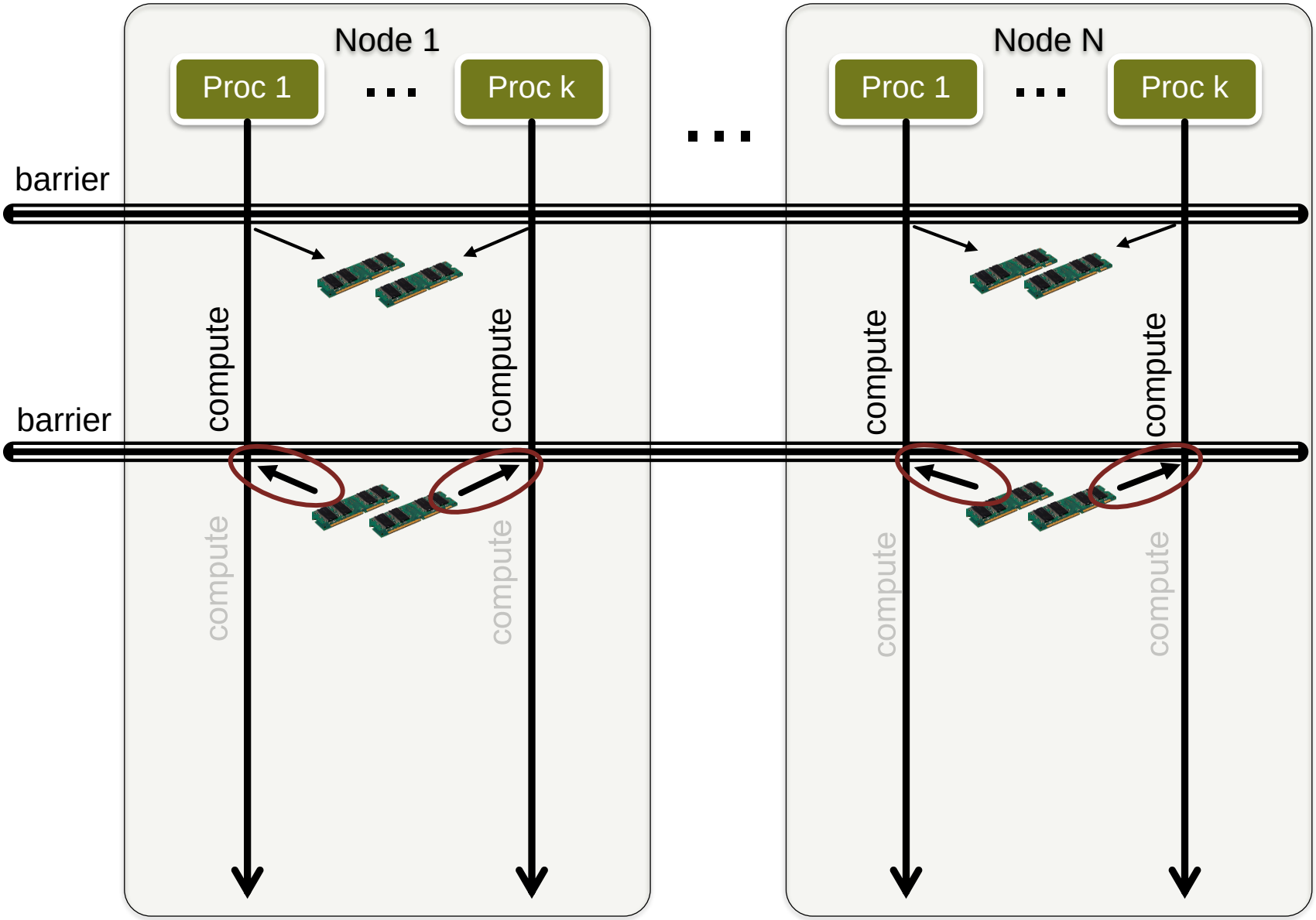

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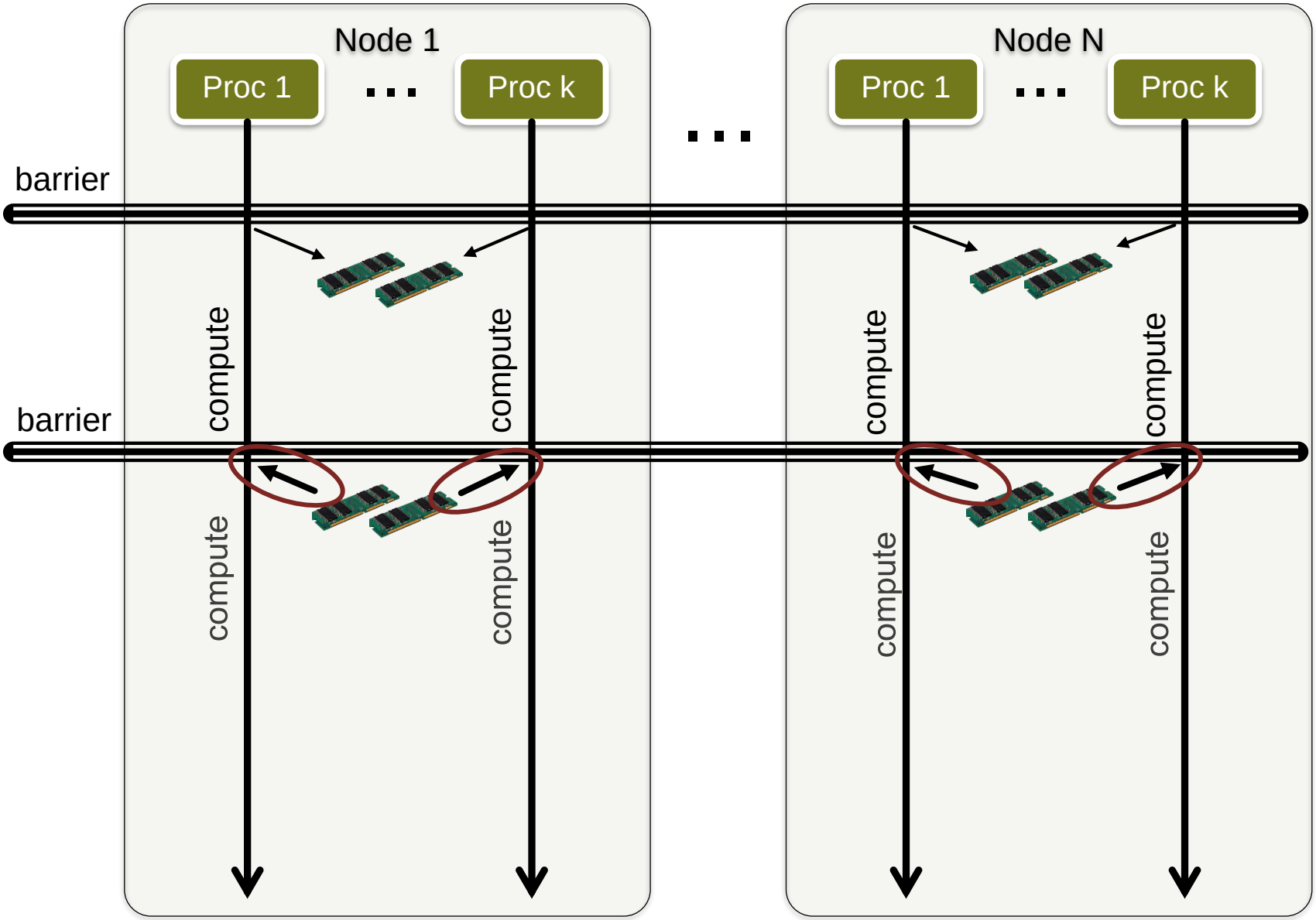

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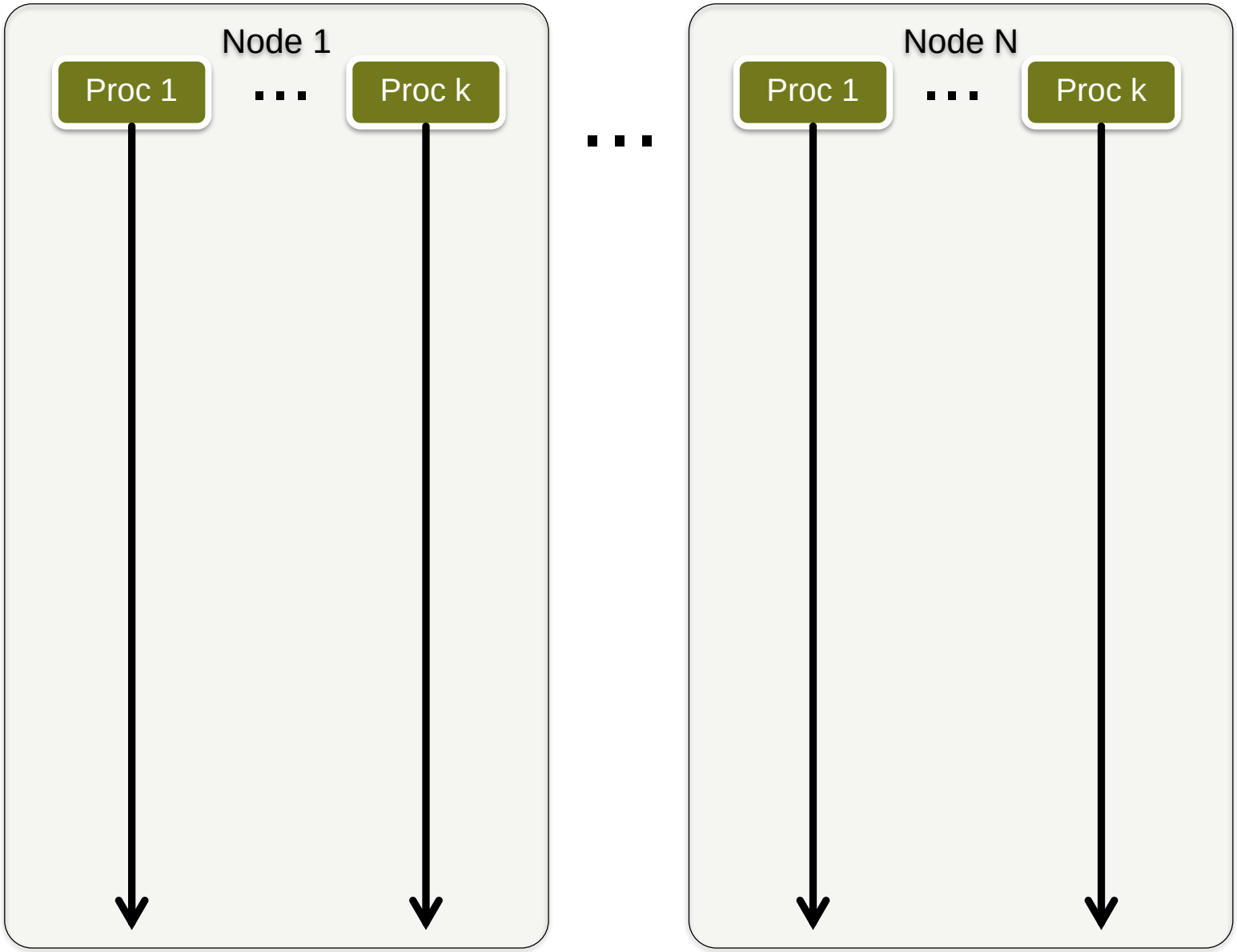

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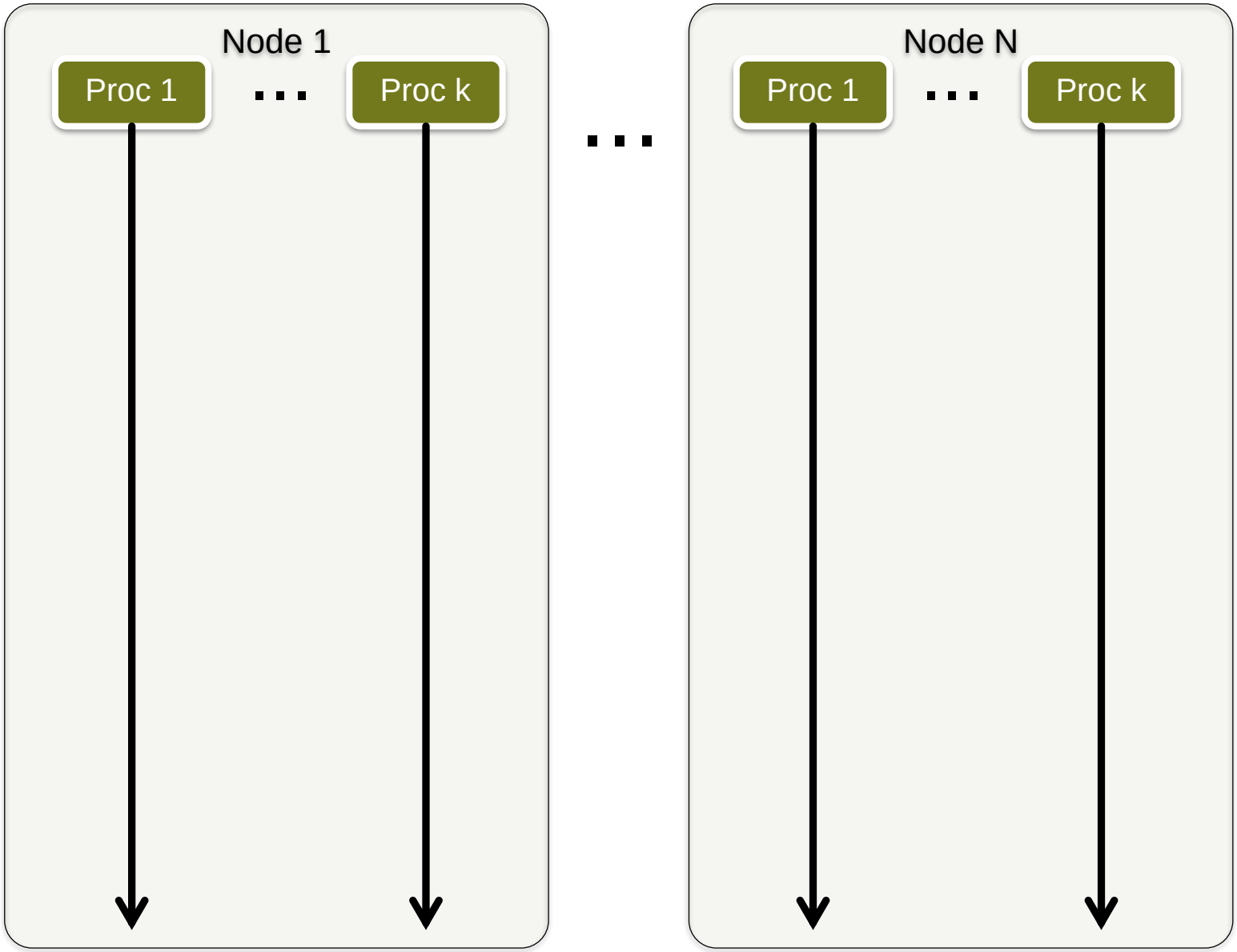

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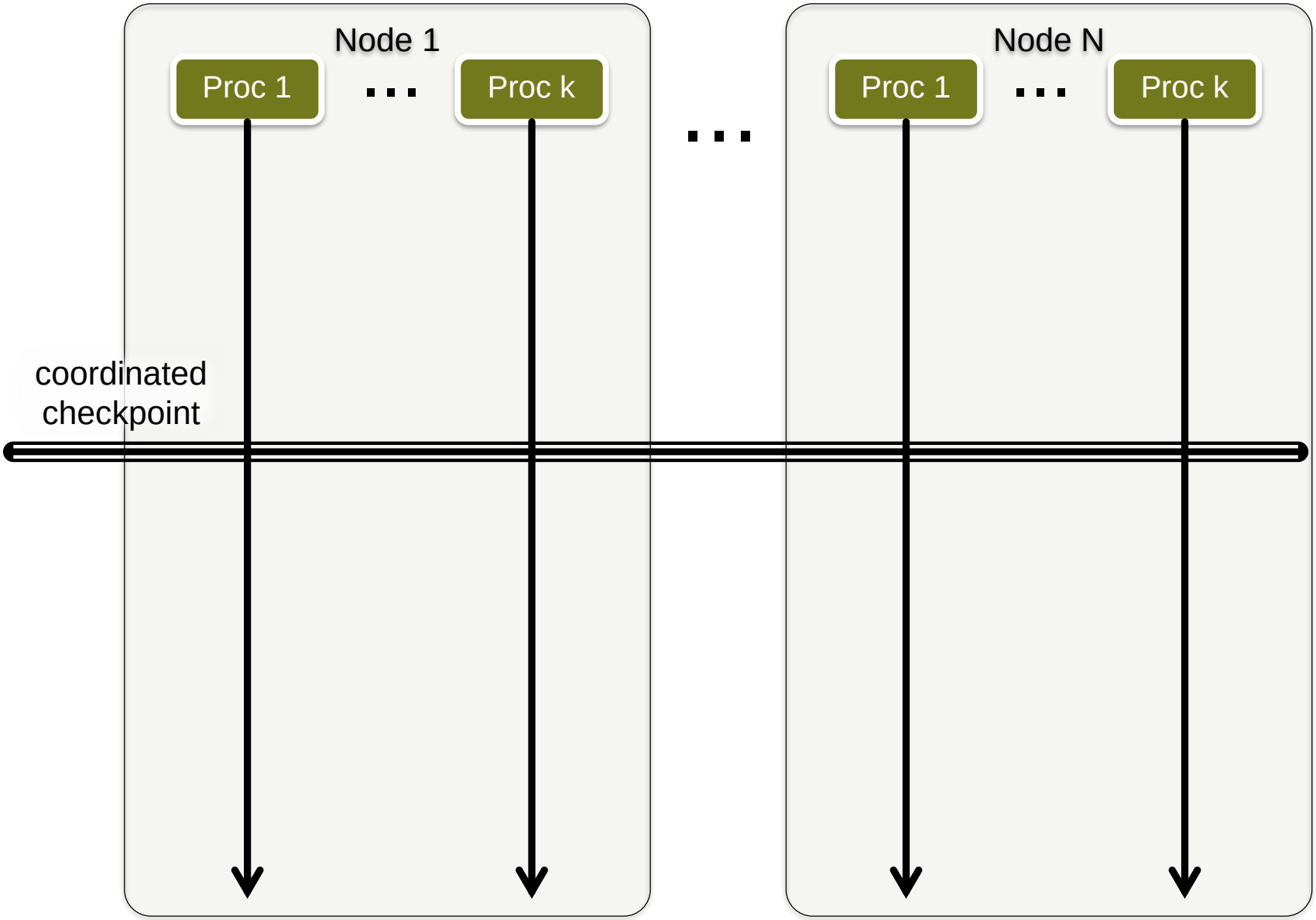

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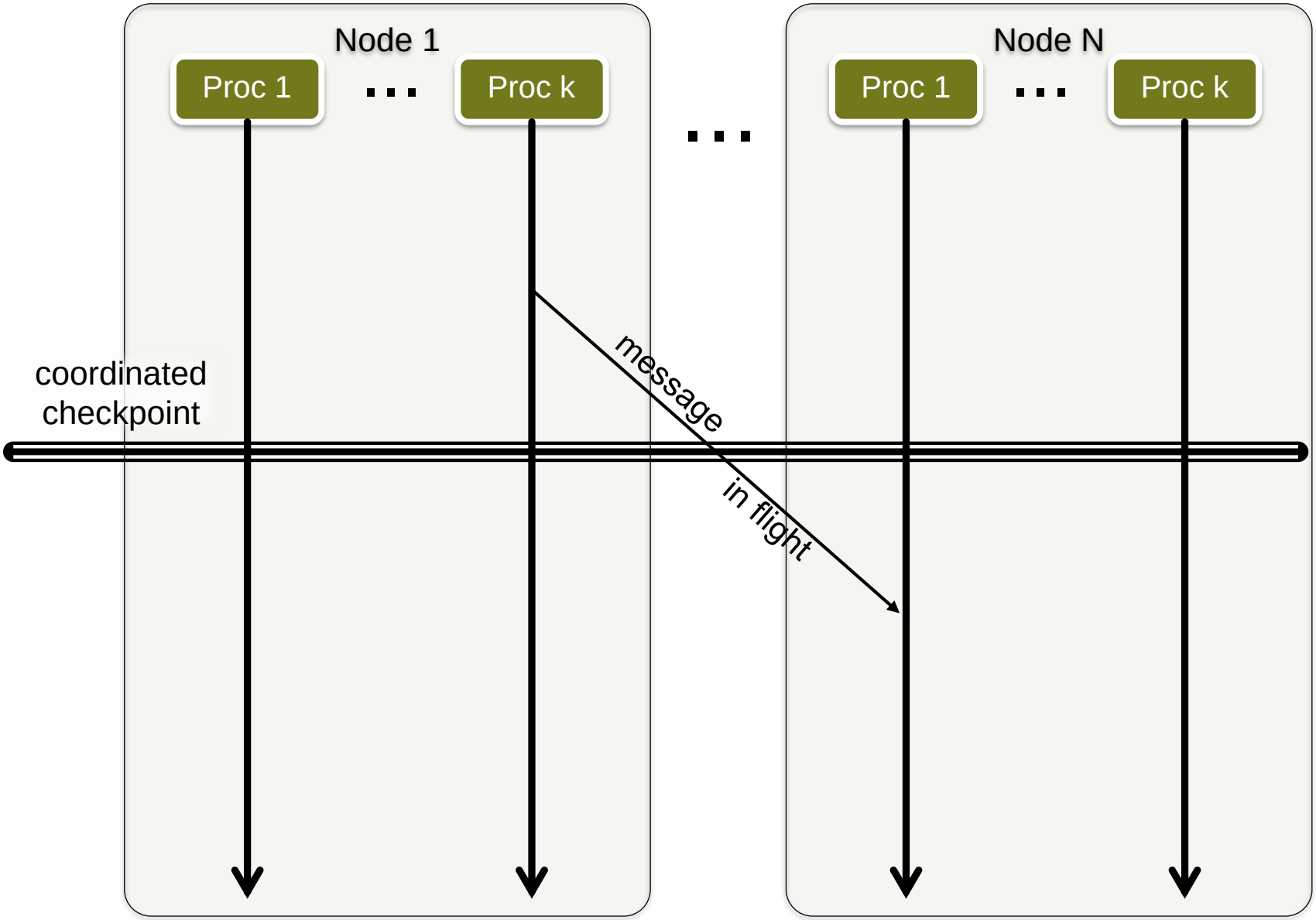

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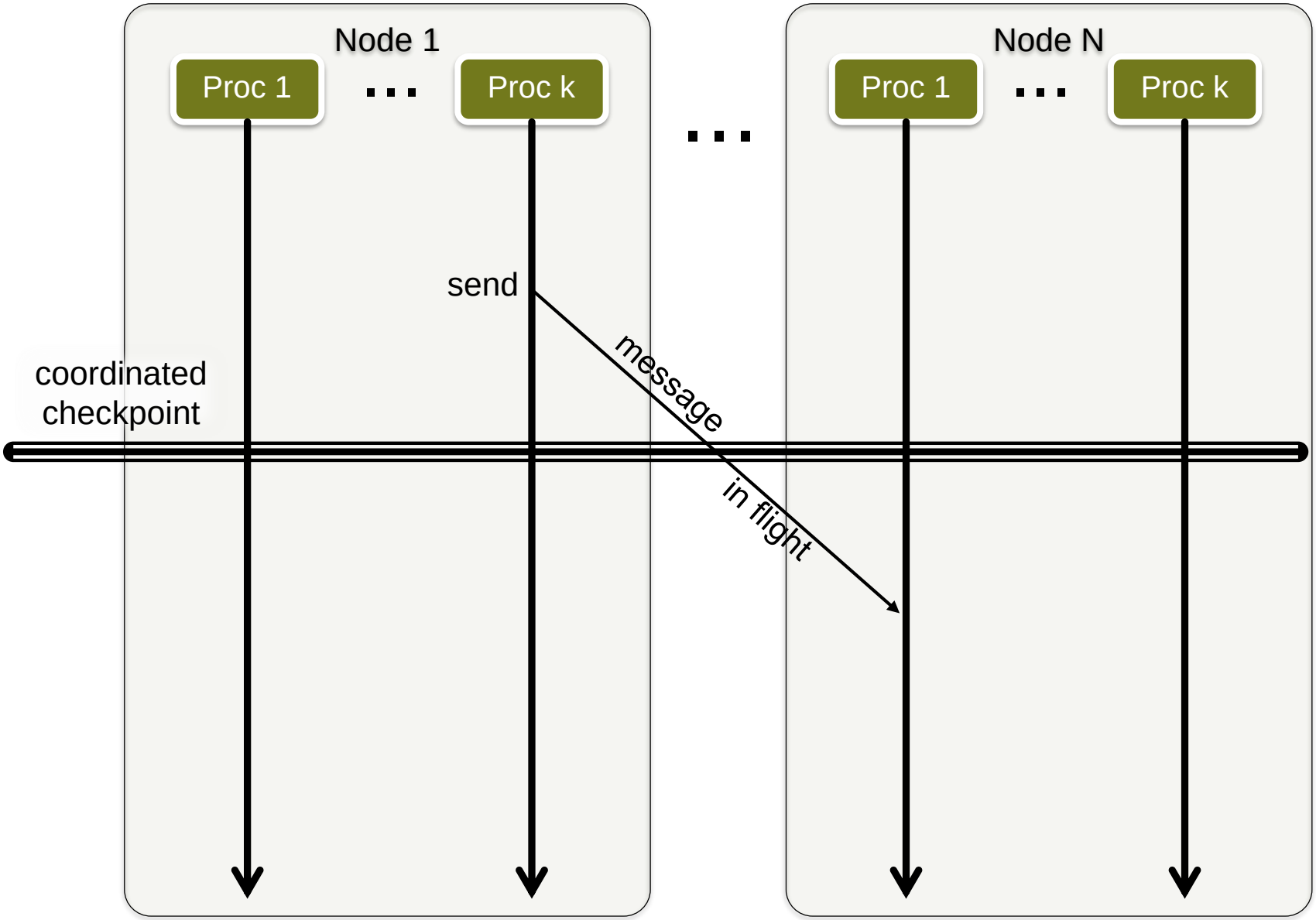

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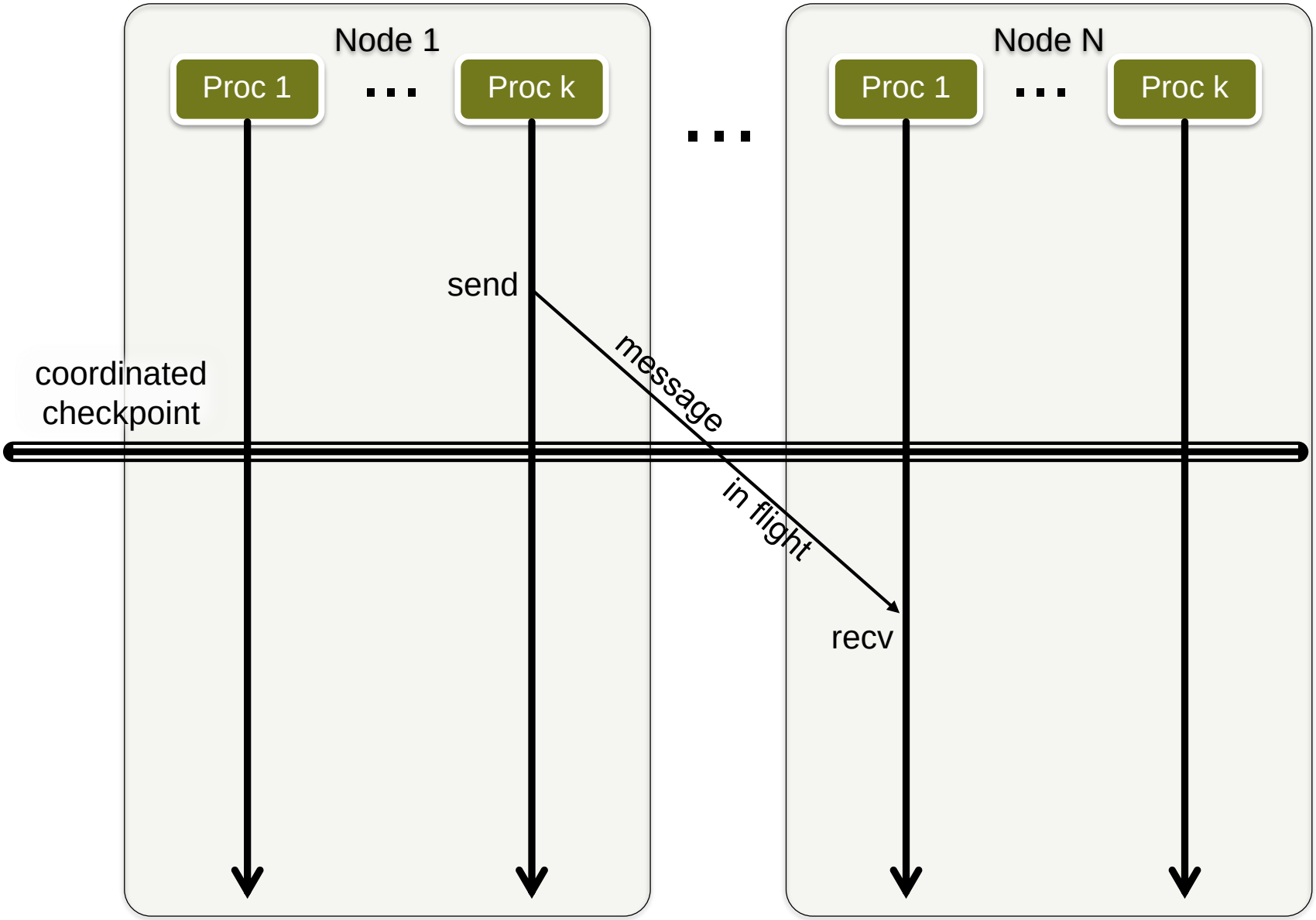

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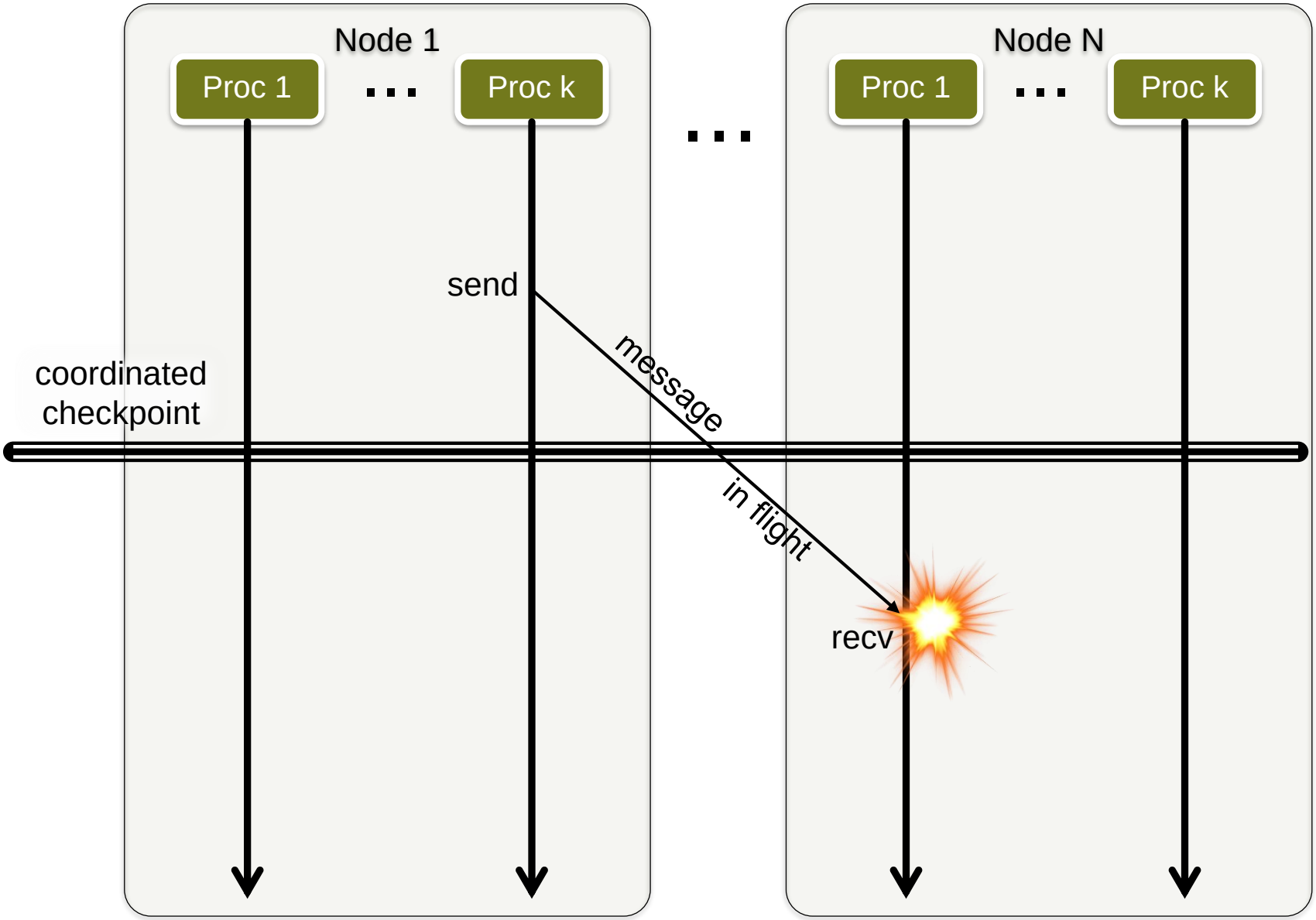

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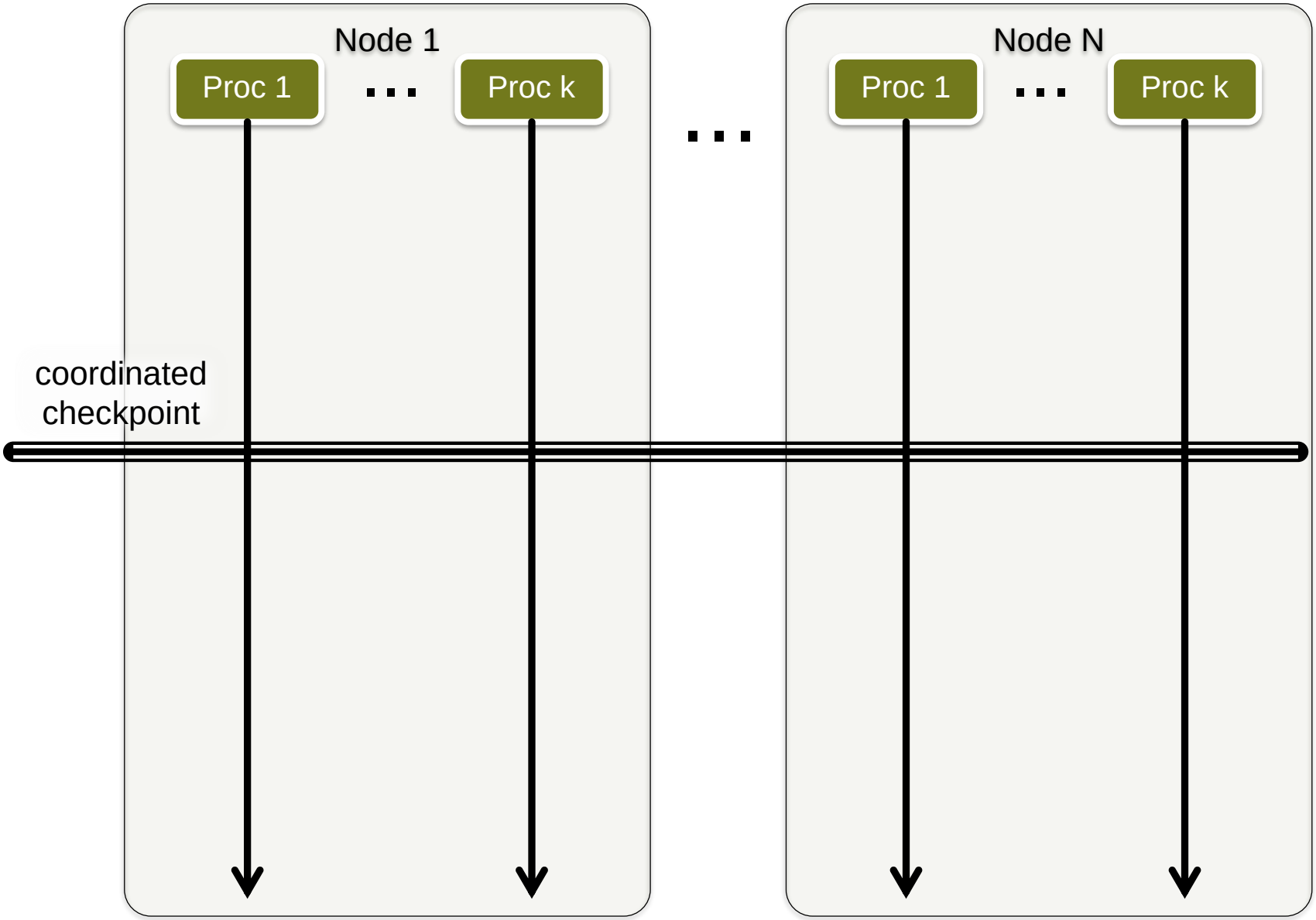

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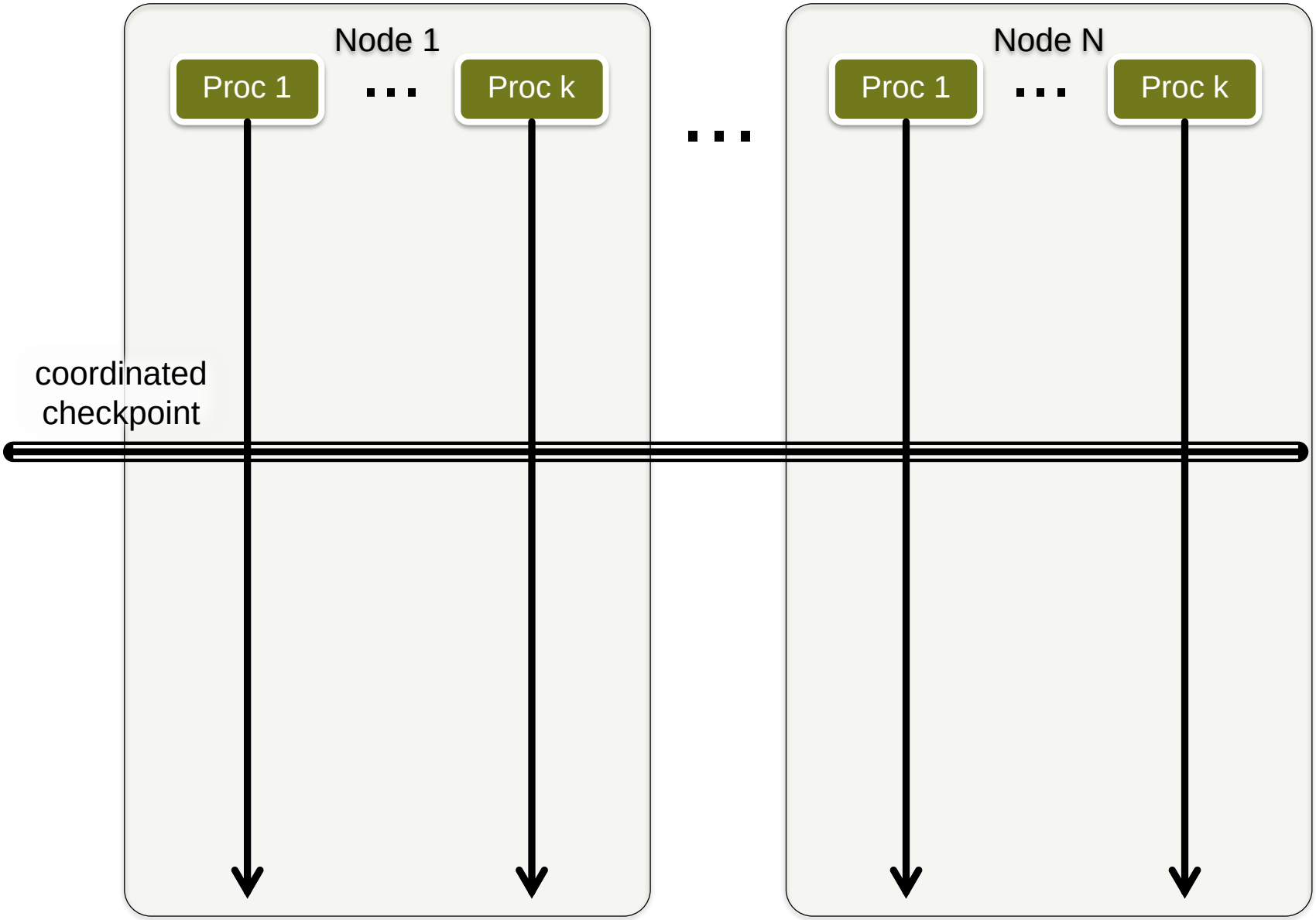

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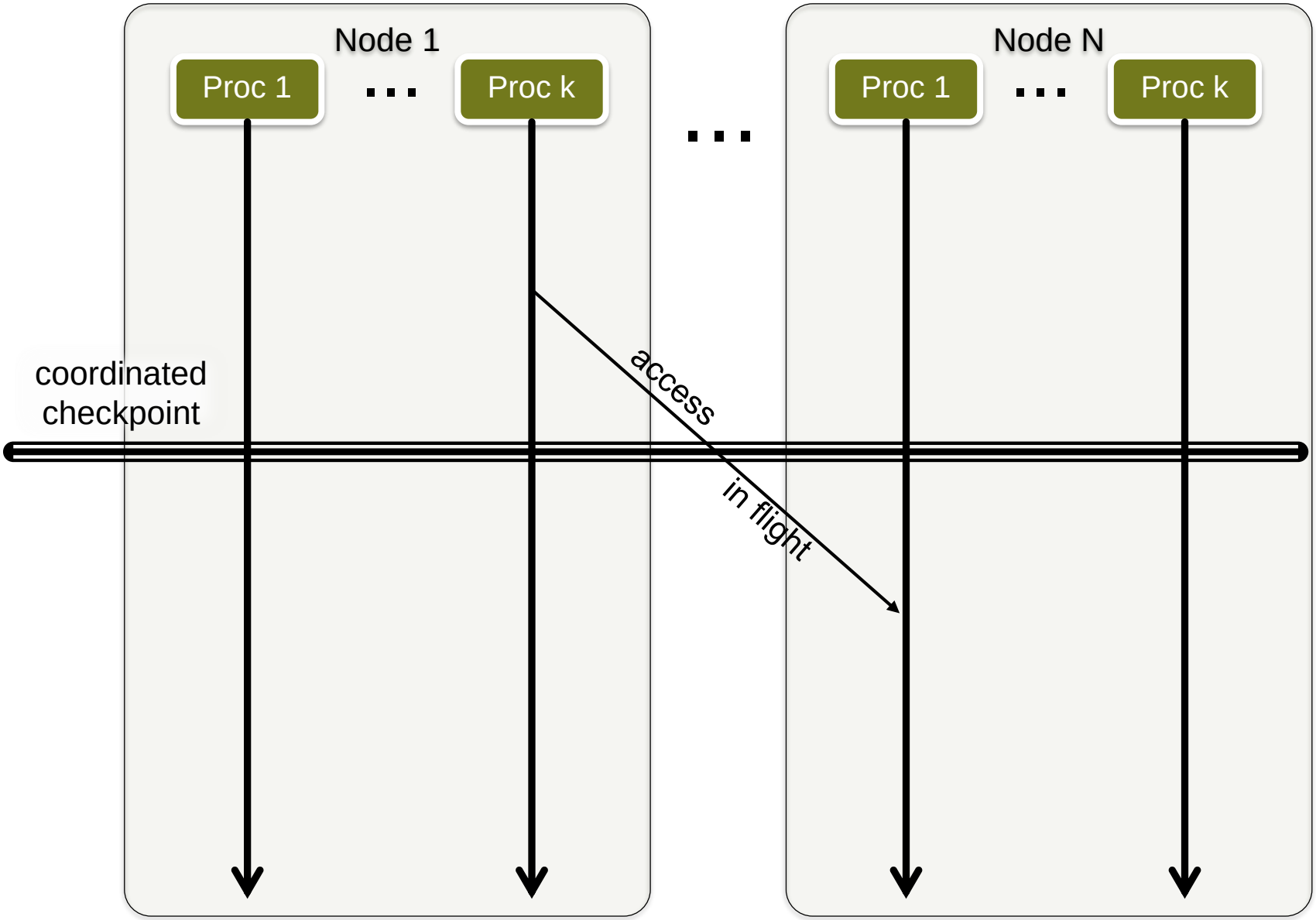
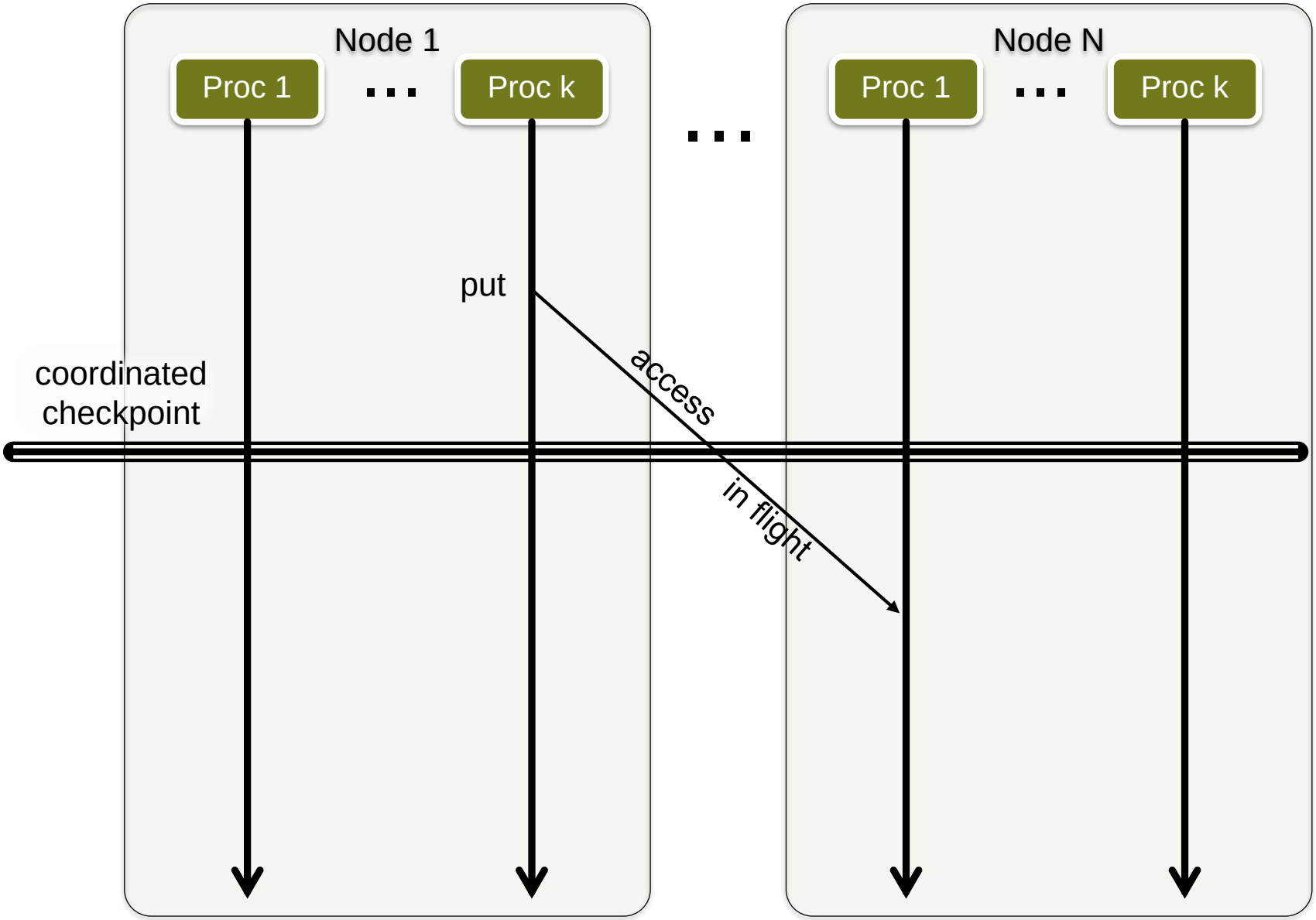


COORDINATED CHECKPOINTING (RMA)



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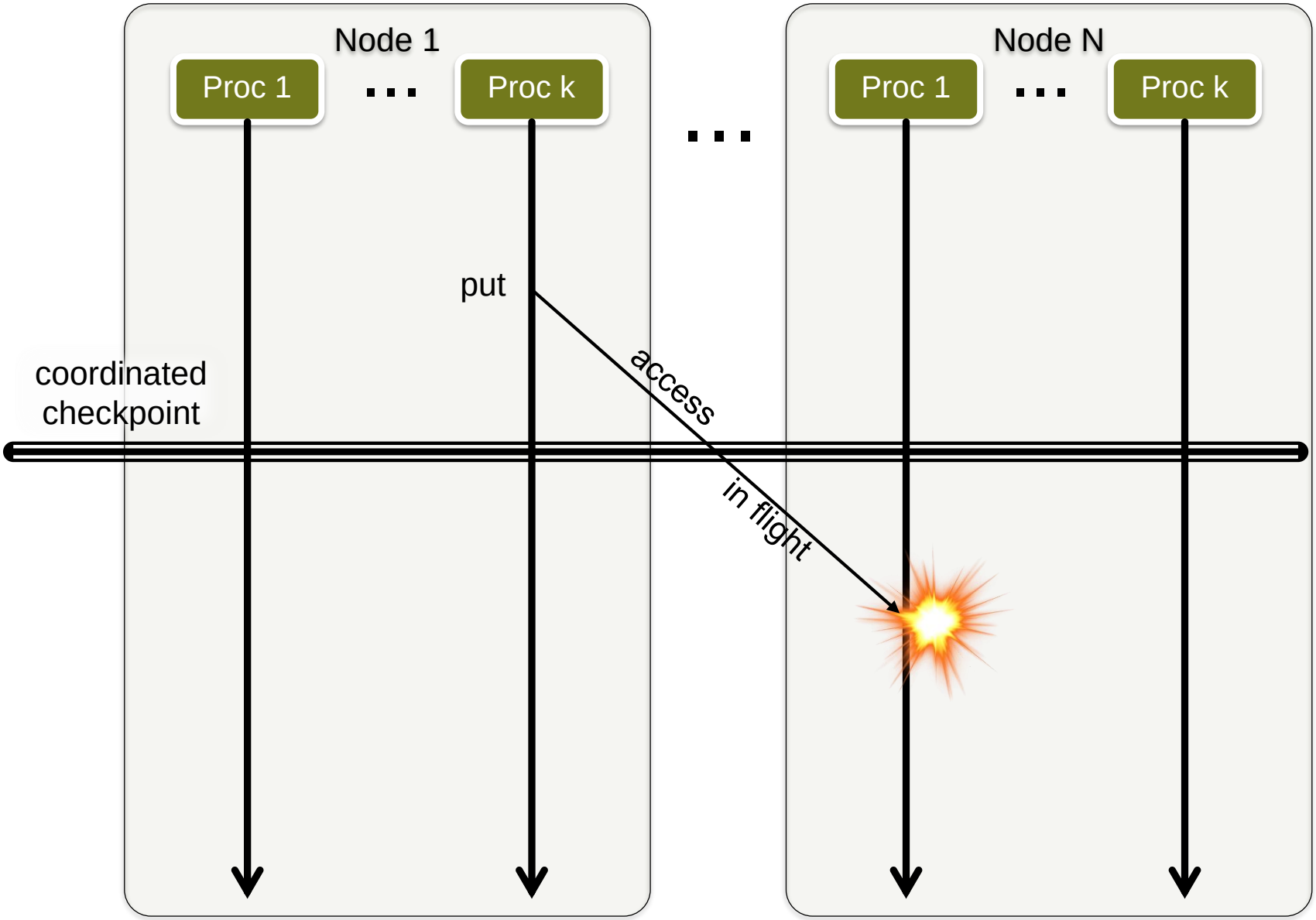

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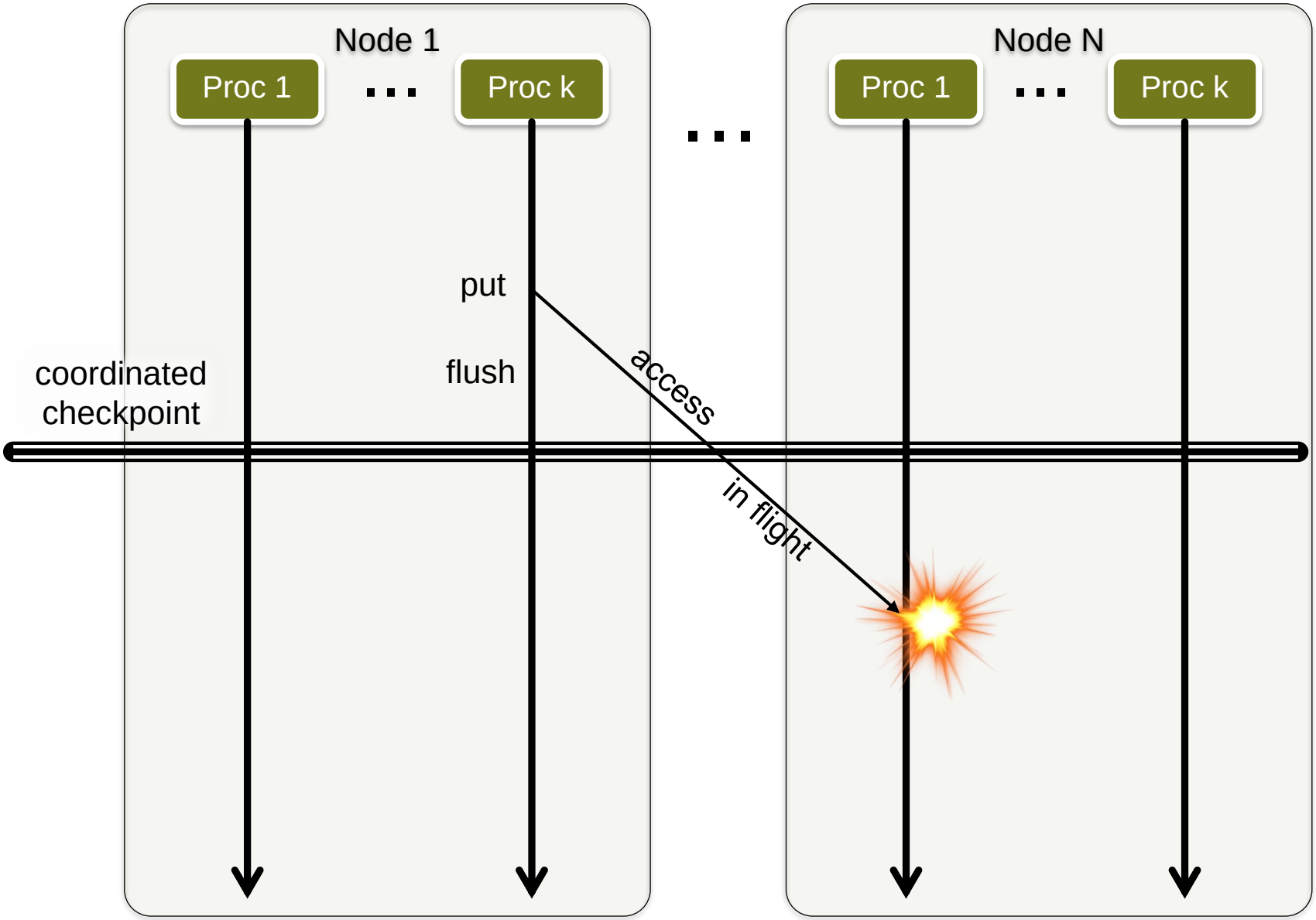

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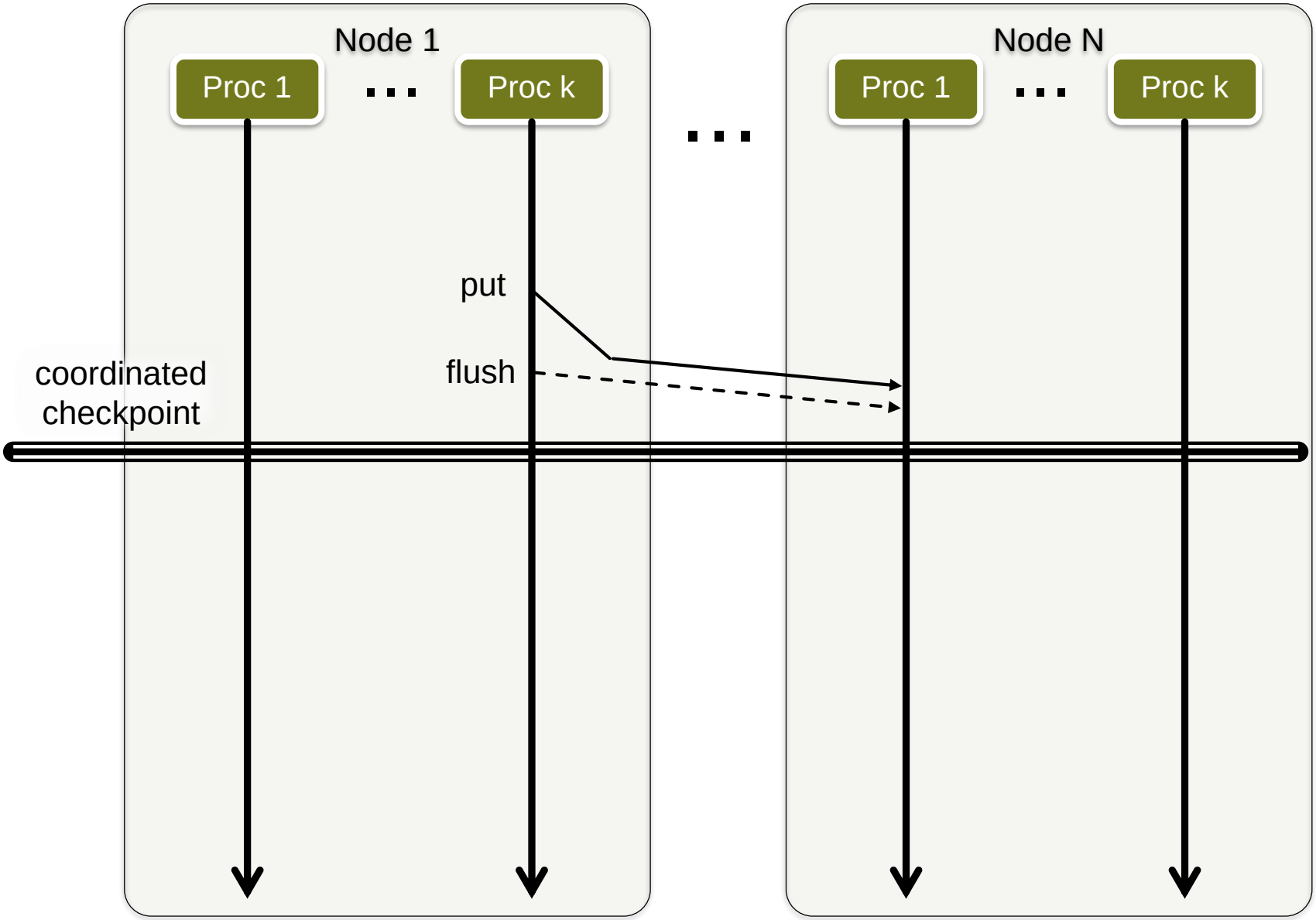


Overview of our Research

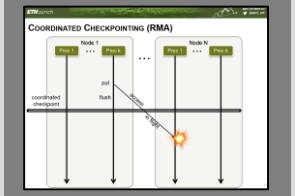
Generic model

$$\mathcal{D} = \langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co} \rangle,$$

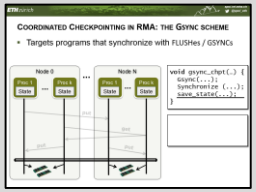
$$\text{PUT}(p \rightrightarrows q)$$
$$\text{GET}(p \leftrightarrows q)$$

MPI-2 PGAS

CC in RMA



MP vs. RMA



Schemes

UC in RMA

MP vs. RMA

Checkpointing schemes

Logging accesses

Recovery in RMA

Basic scheme

Extended RMA semantics

Proofs

Theorem 4.2. *The recove rithm 2 preserves the* $\xrightarrow{cohb}$ *or ferred to as the* gsync order*).*

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Correct recovery

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$$\langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \mathcal{H}, \mathcal{G}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co}, \mathcal{M} \rangle$$

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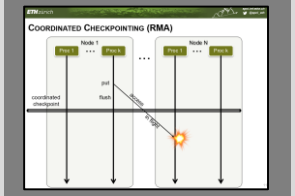

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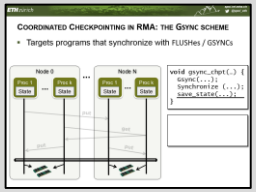

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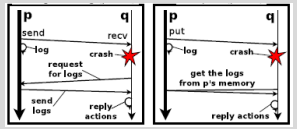

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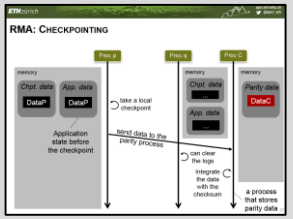
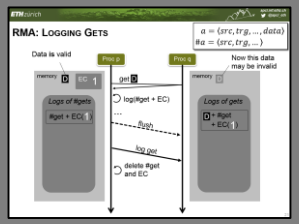
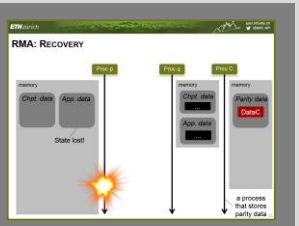


Checkpointing schemes



Logging accesses

Recovery in RMA



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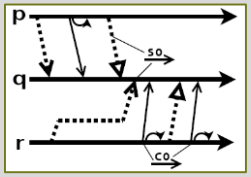

Proofs

THEOREM 4.2. *The recovery algorithm 2 preserves the* $\xrightarrow{cohb}$ *order (referred to as the* gsync order*).*

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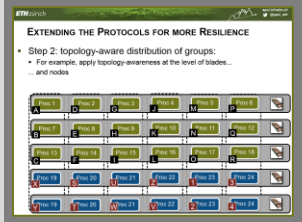

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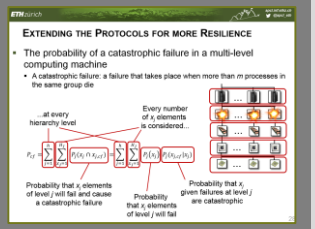
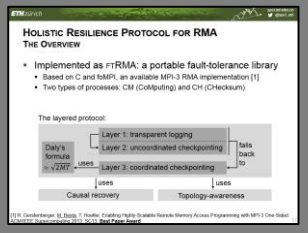


Decreasing failure prob.

Holistic fault-tolerance library



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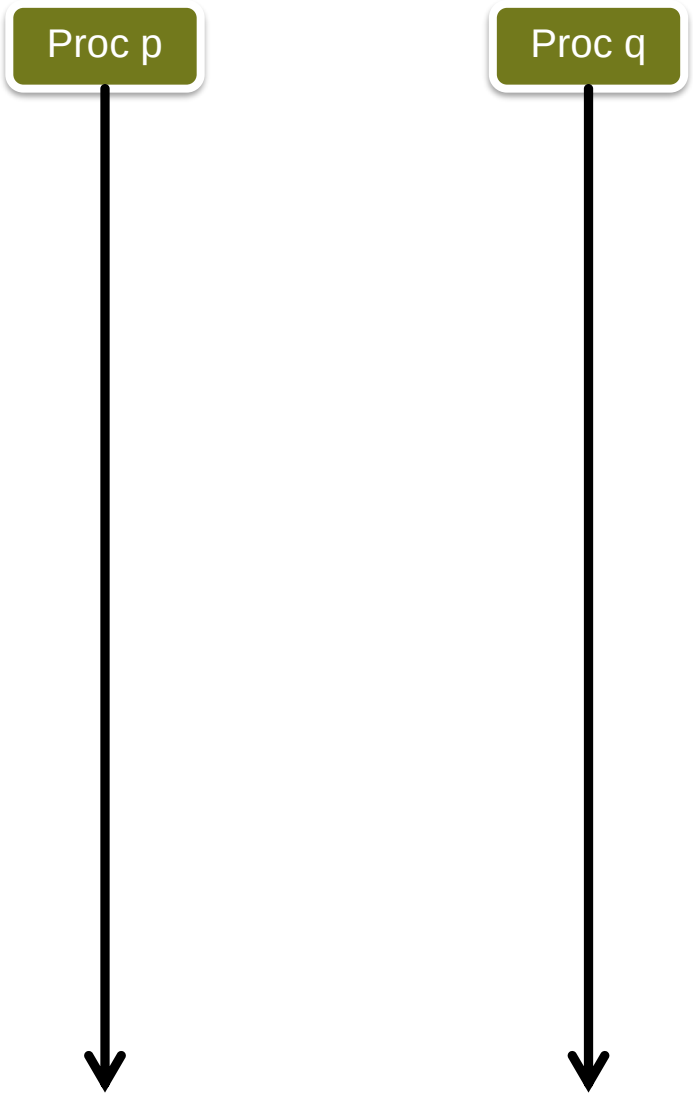

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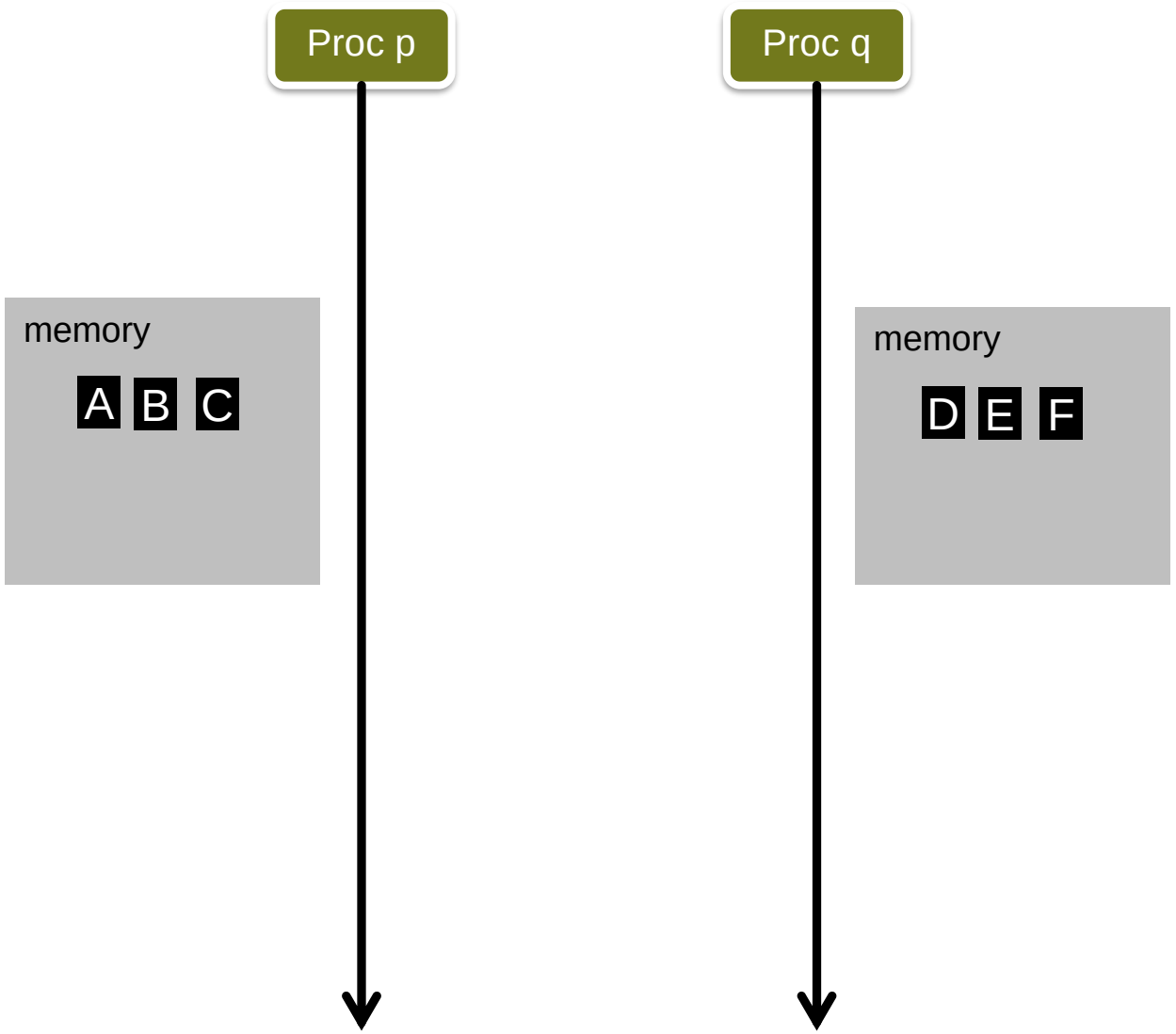

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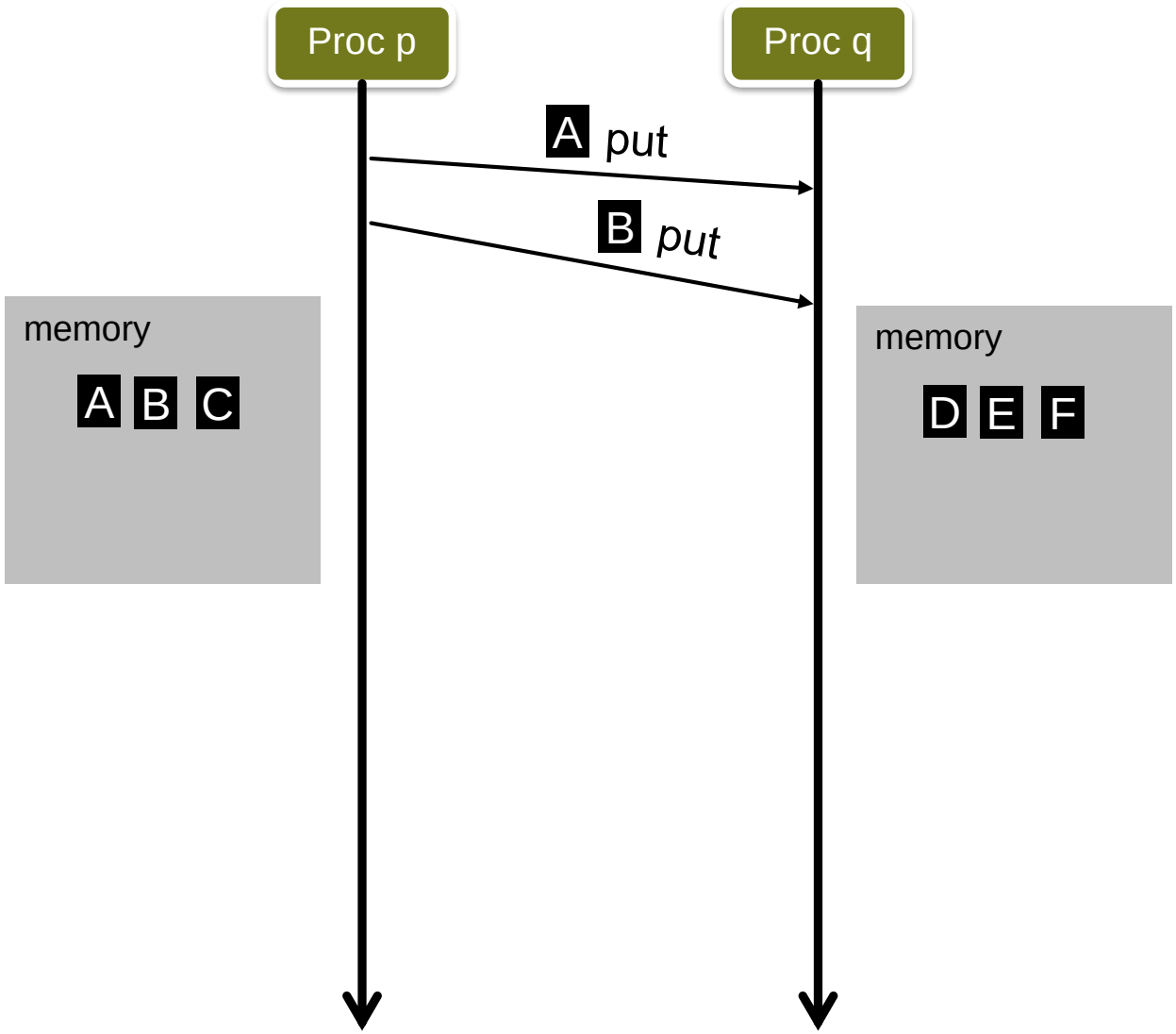

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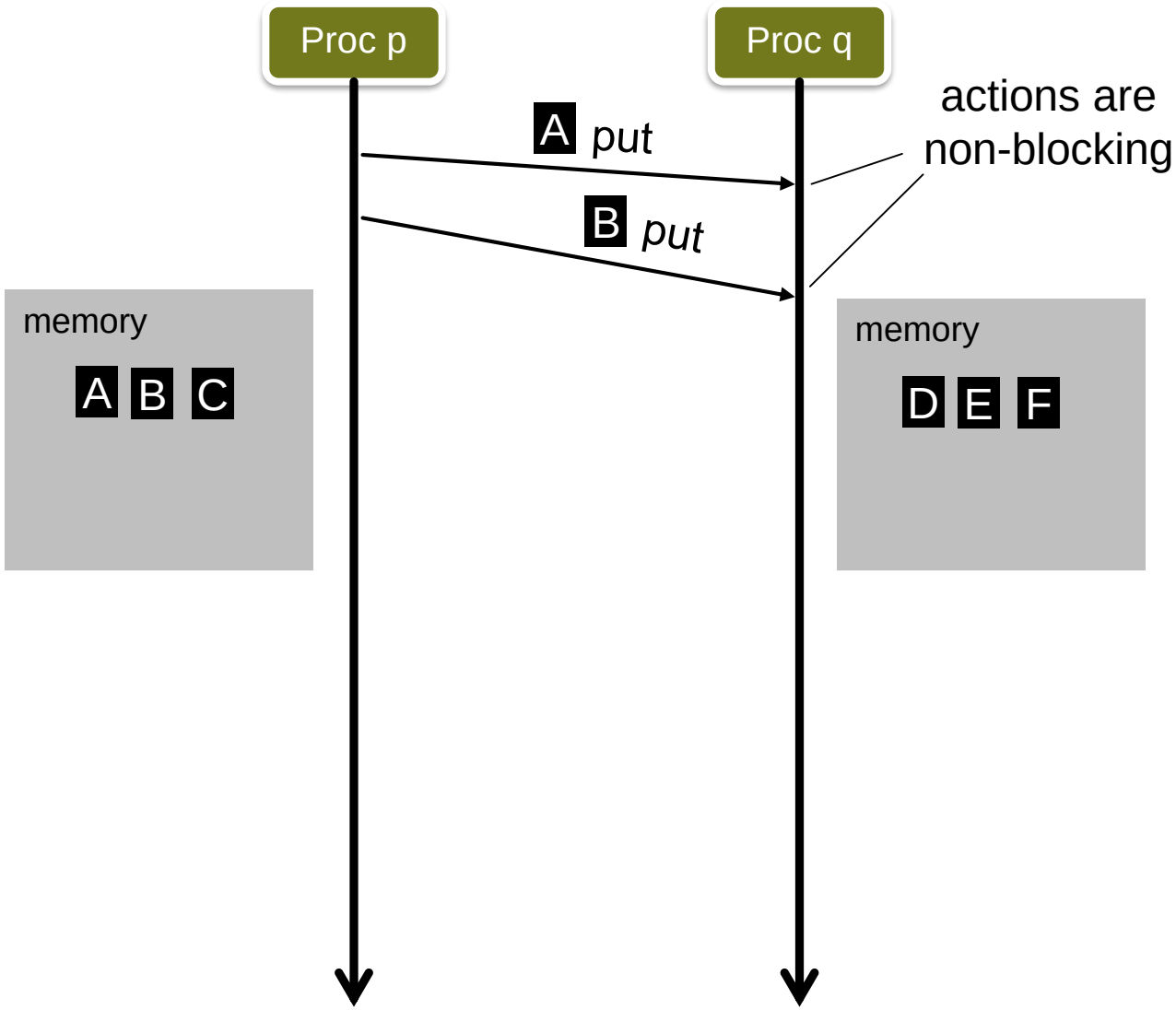
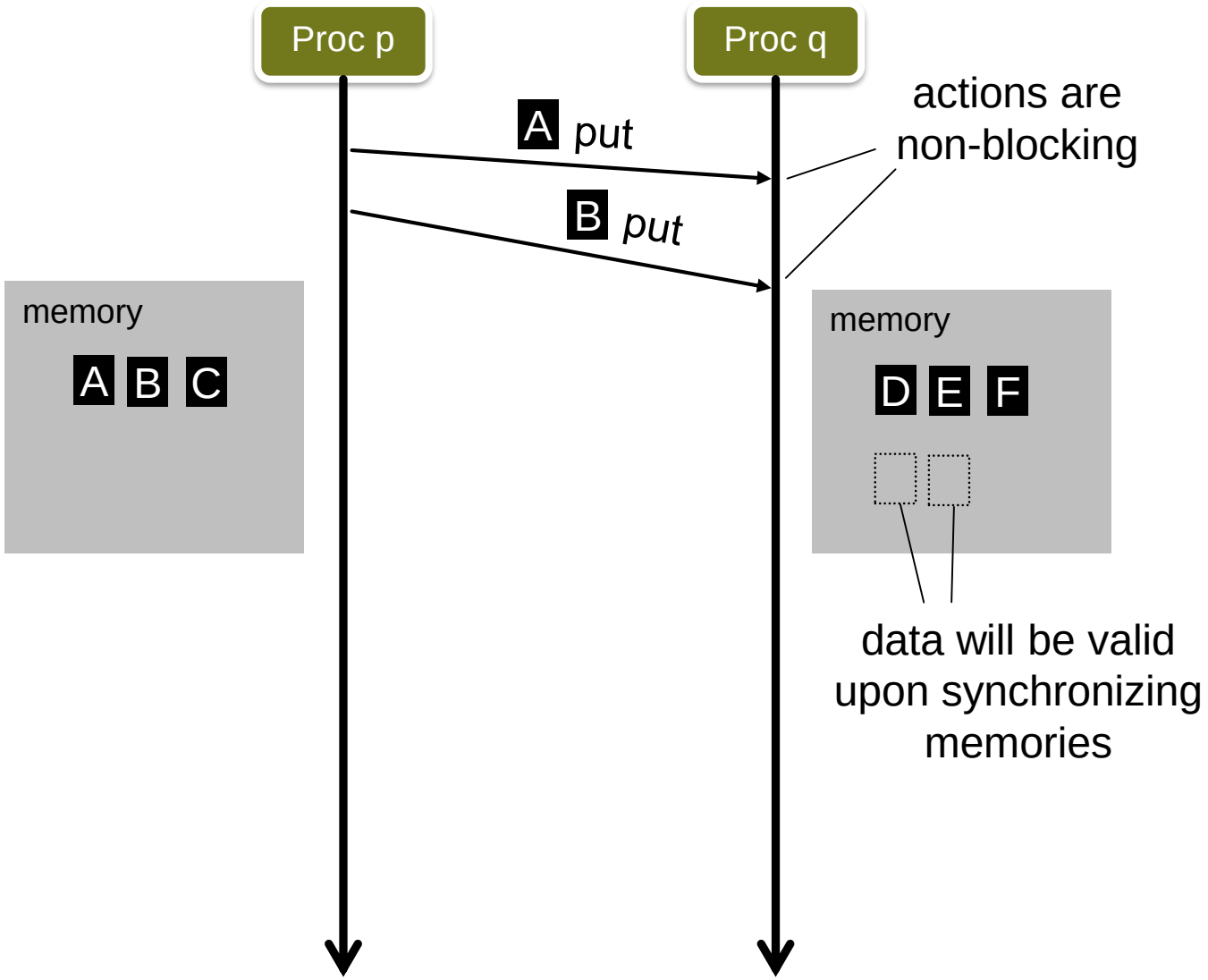
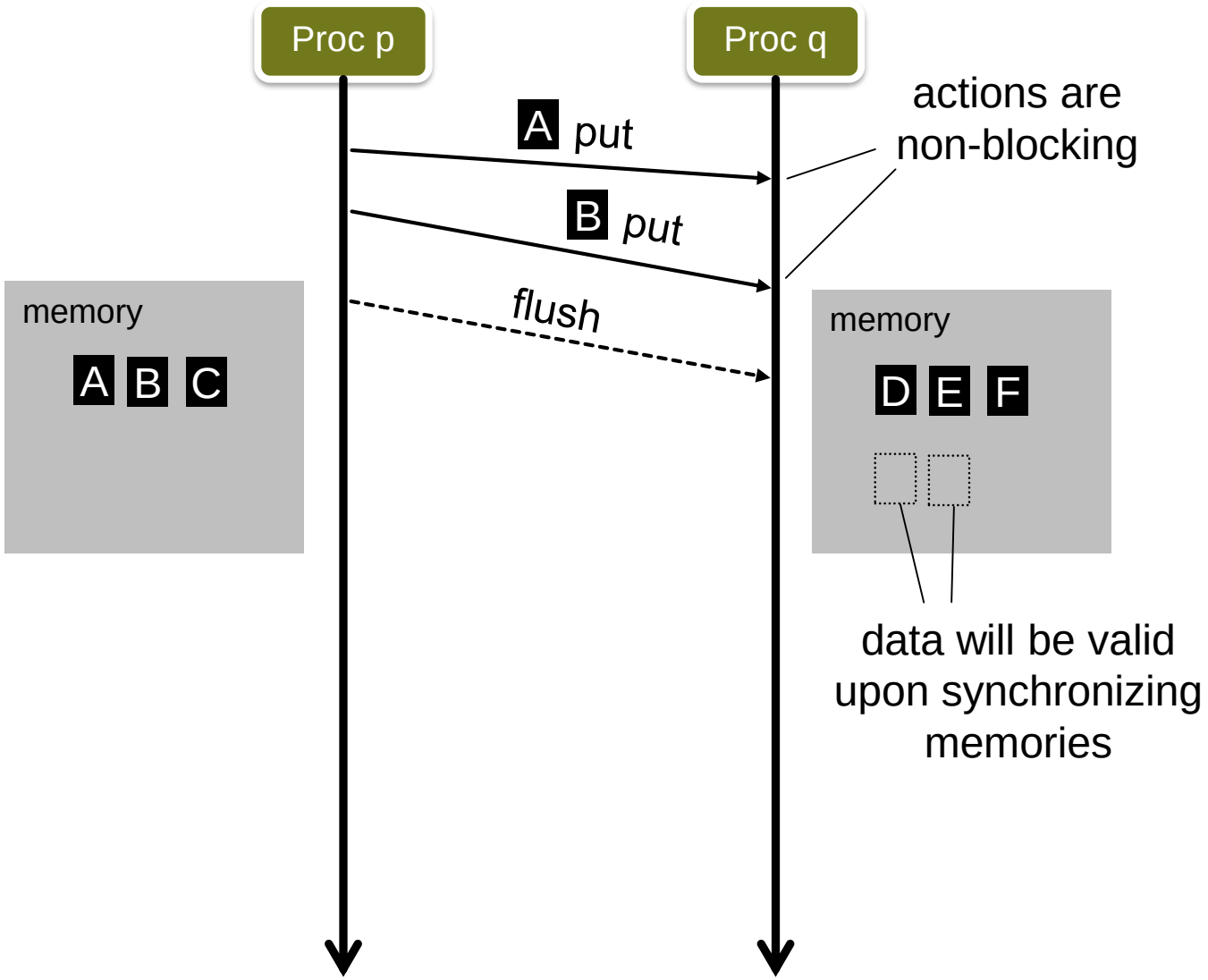

Proc p
Proc q
A put
B put
actions are non-blocking
memory
A B C
memory
D E F

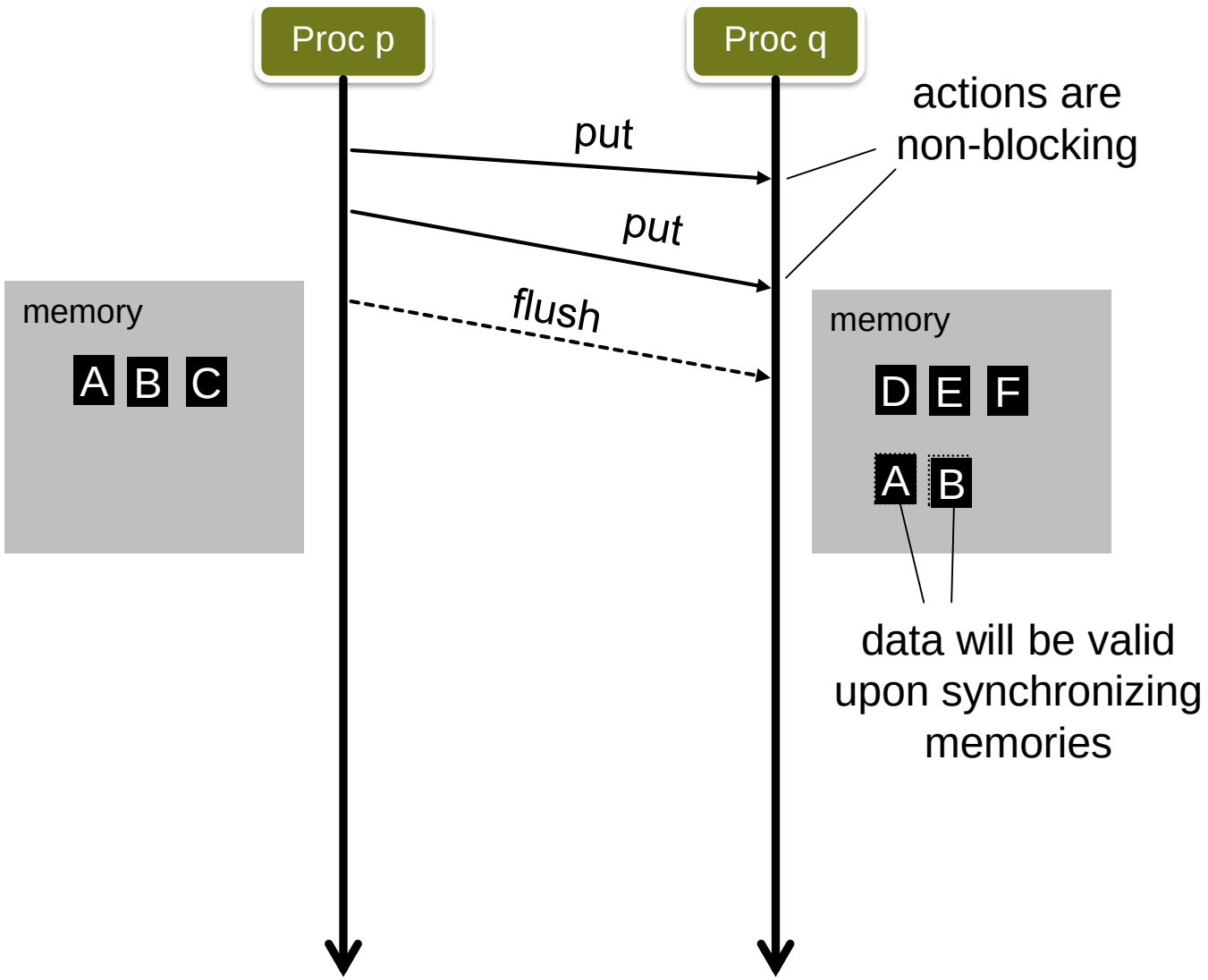
RMA: EPOCHS


Proc p
Proc q
A put
B put
actions are non-blocking
memory
A B C
memory
D E F
data will be valid upon synchronizing memories

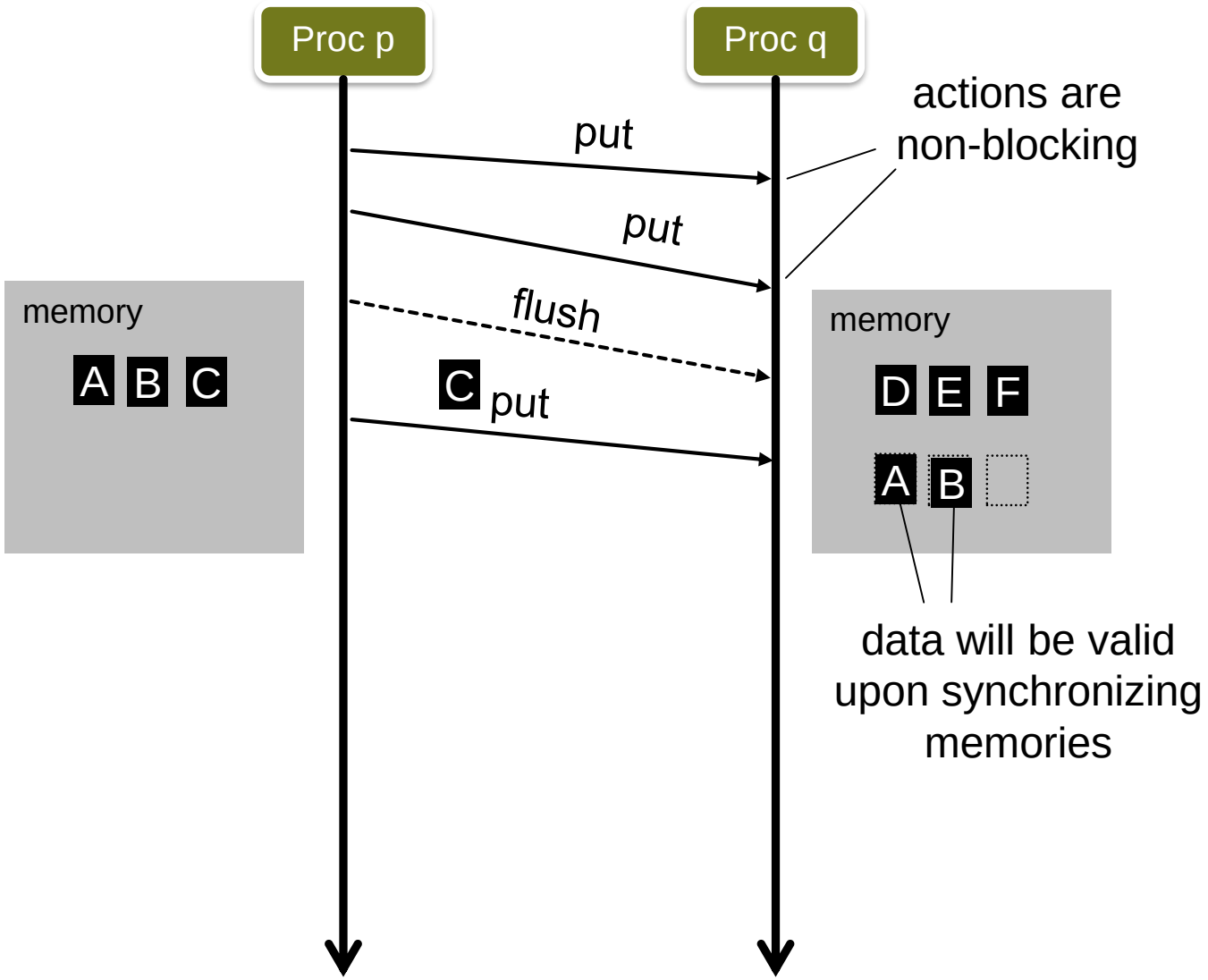
RMA: EPOCHS


Proc p
Proc q
A put
B put
flush
actions are non-blocking
memory
A B C
memory
D E F
data will be valid upon synchronizing memories

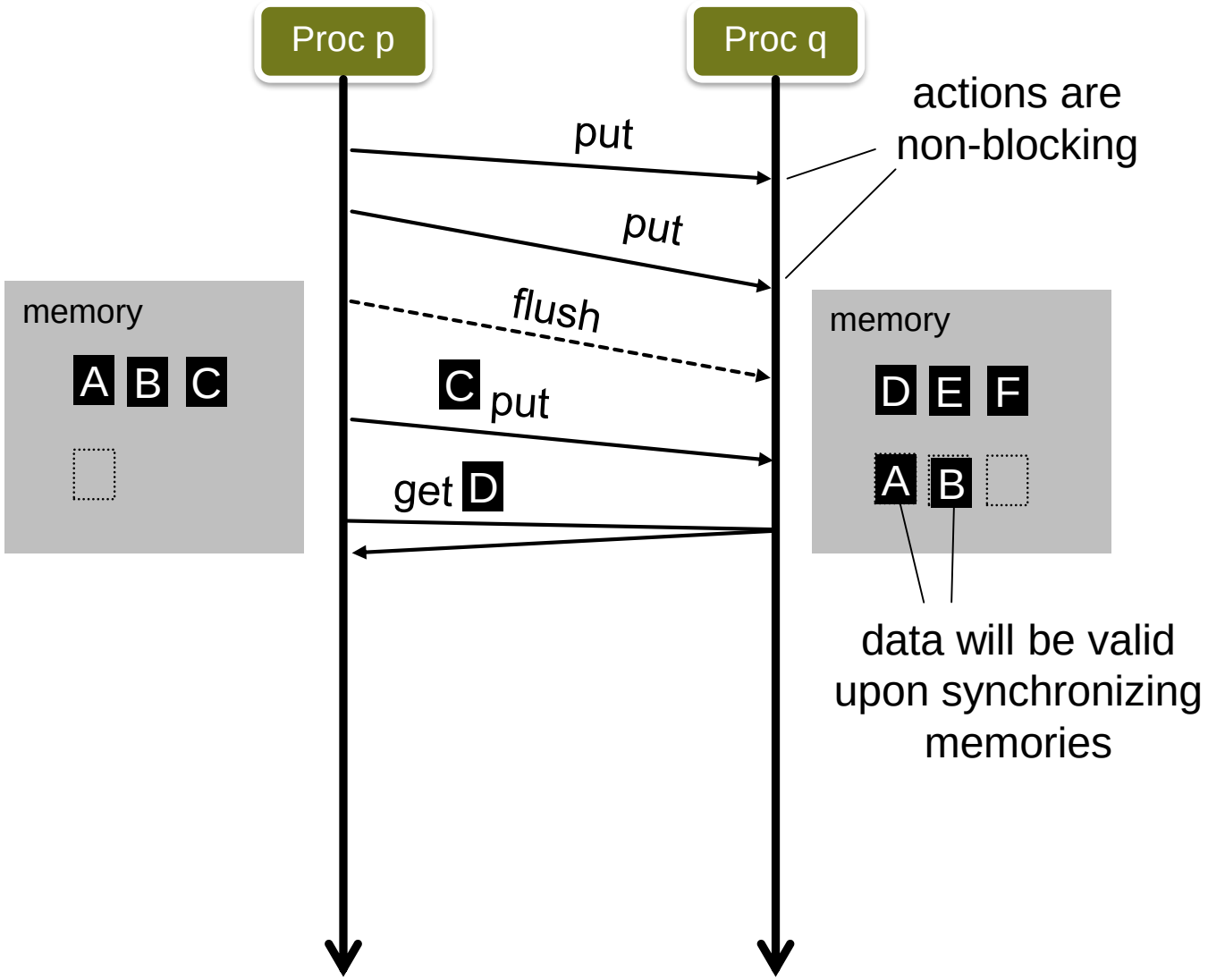
RMA: EPOCHS


Proc p
Proc q
put
put
flush
actions are non-blocking
memory
A B C
memory
D E F
A B
data will be valid upon synchronizing memories

RMA: EPOCHS


Proc p
Proc q
actions are non-blocking
put
put
flush
C put
memory
A B C
memory
D E F
A B
data will be valid upon synchronizing memories

RMA: EPOCHS


Proc p
Proc q
actions are non-blocking
put
put
flush
C put
get D
memory
A B C
memory
D E F
A B
data will be valid upon synchronizing memories

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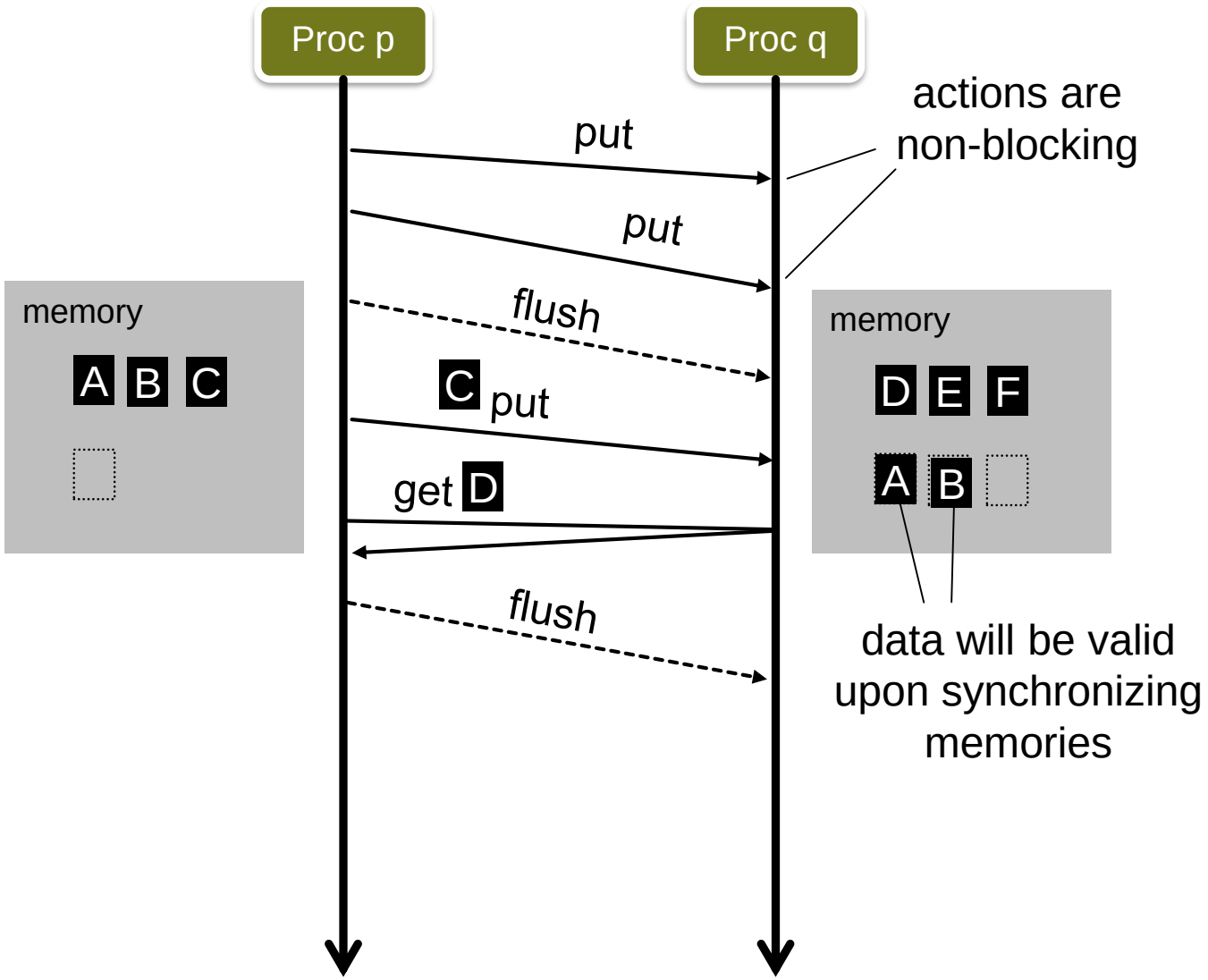
Proc p
Proc q
actions are non-blocking
put
put
flush
C put
get D
flush
memory
A B C
memory
D E F
A B
data will be valid upon synchronizing memories

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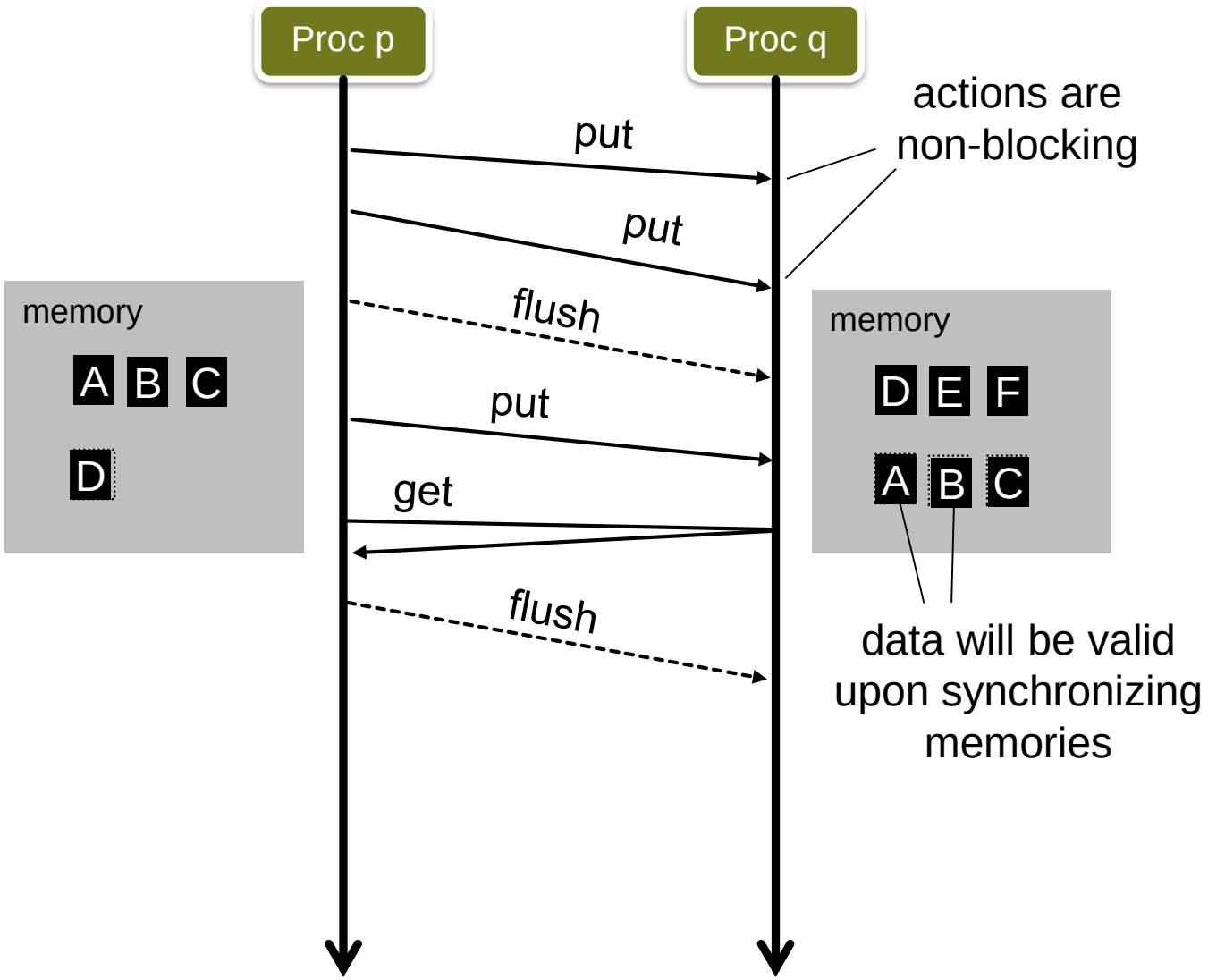
Proc p
Proc q
actions are non-blocking
put
put
flush
put
get
flush
memory
A B C
D
memory
D E F
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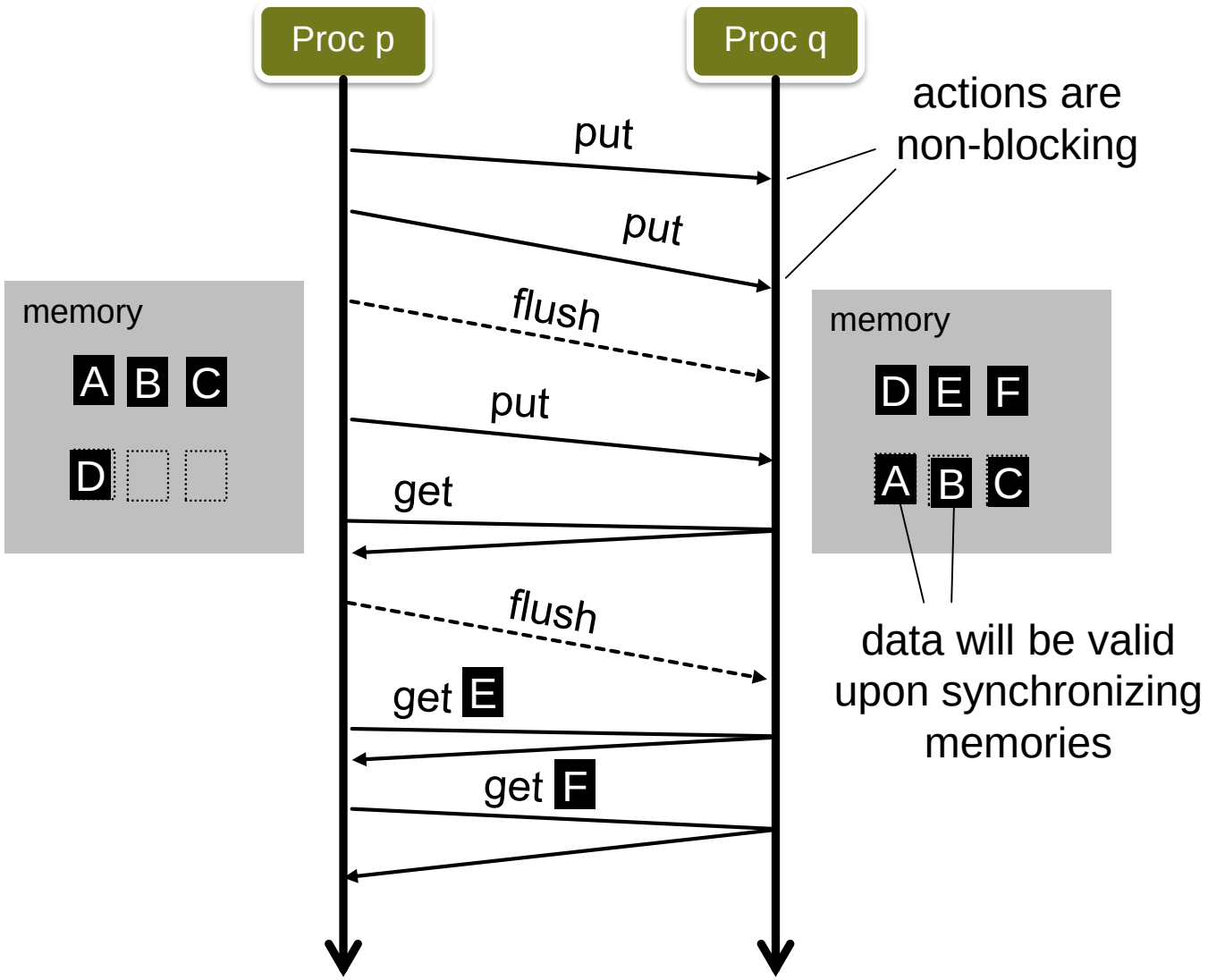
Proc p
Proc q
actions are non-blocking
put
put
flush
put
get
flush
get E
get F
memory
A B C
D
memory
D E F
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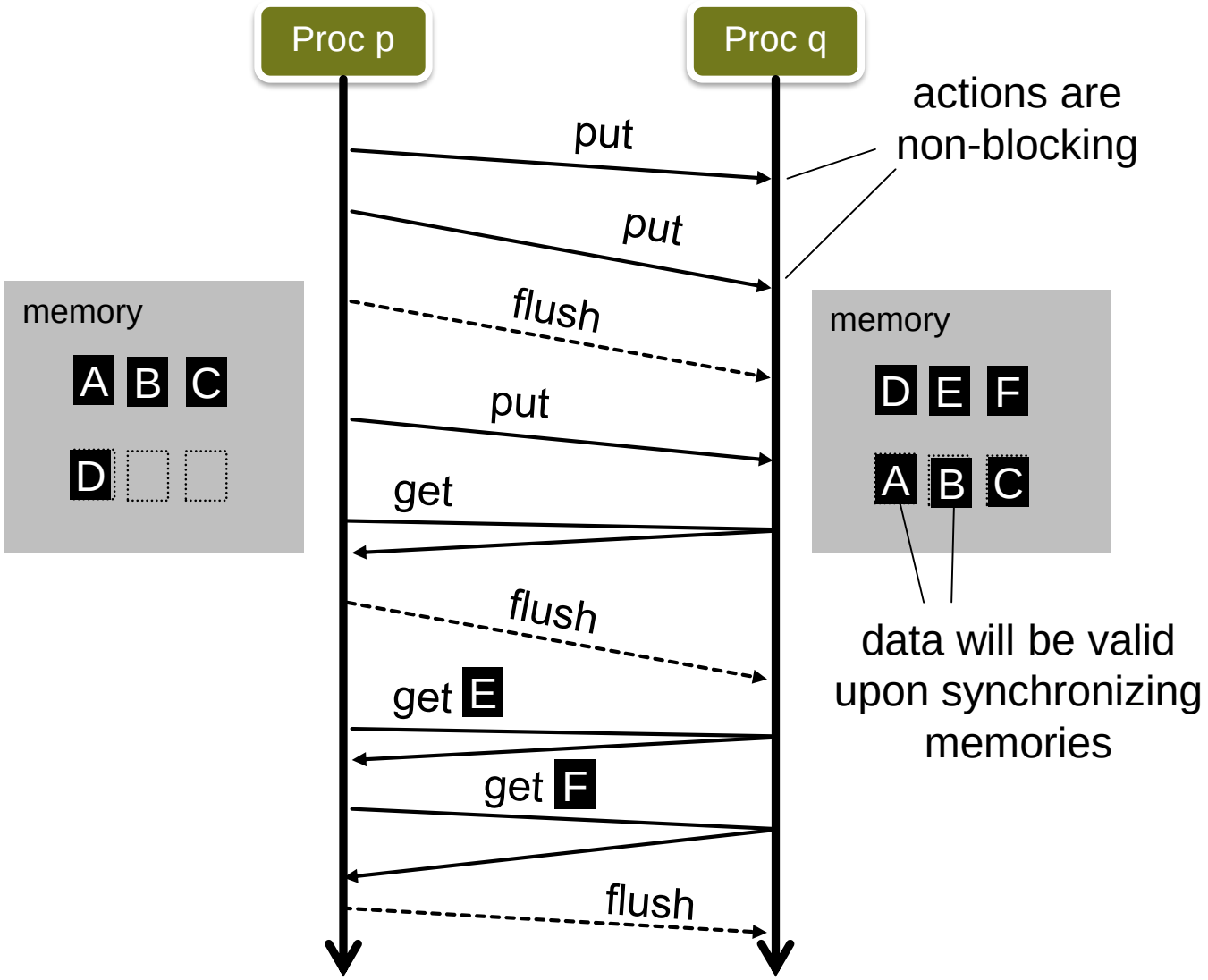
Proc p
Proc q
actions are non-blocking
put
put
flush
put
get
flush
get E
get F
flush
memory
A B C
D
memory
D E F
A B C
data will be valid upon synchronizing memories

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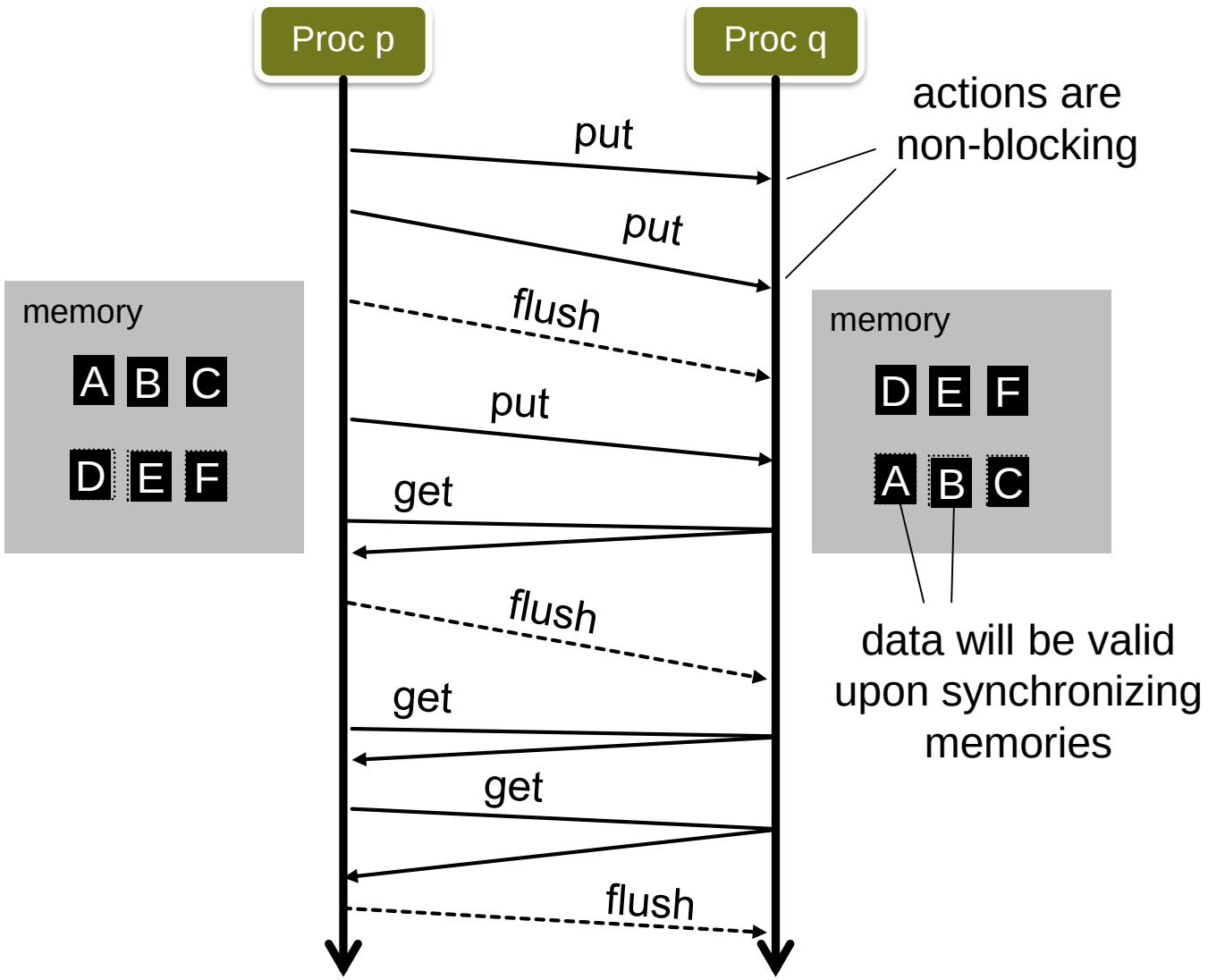
Proc p
Proc q
actions are non-blocking
put
put
flush
put
get
flush
get
get
flush
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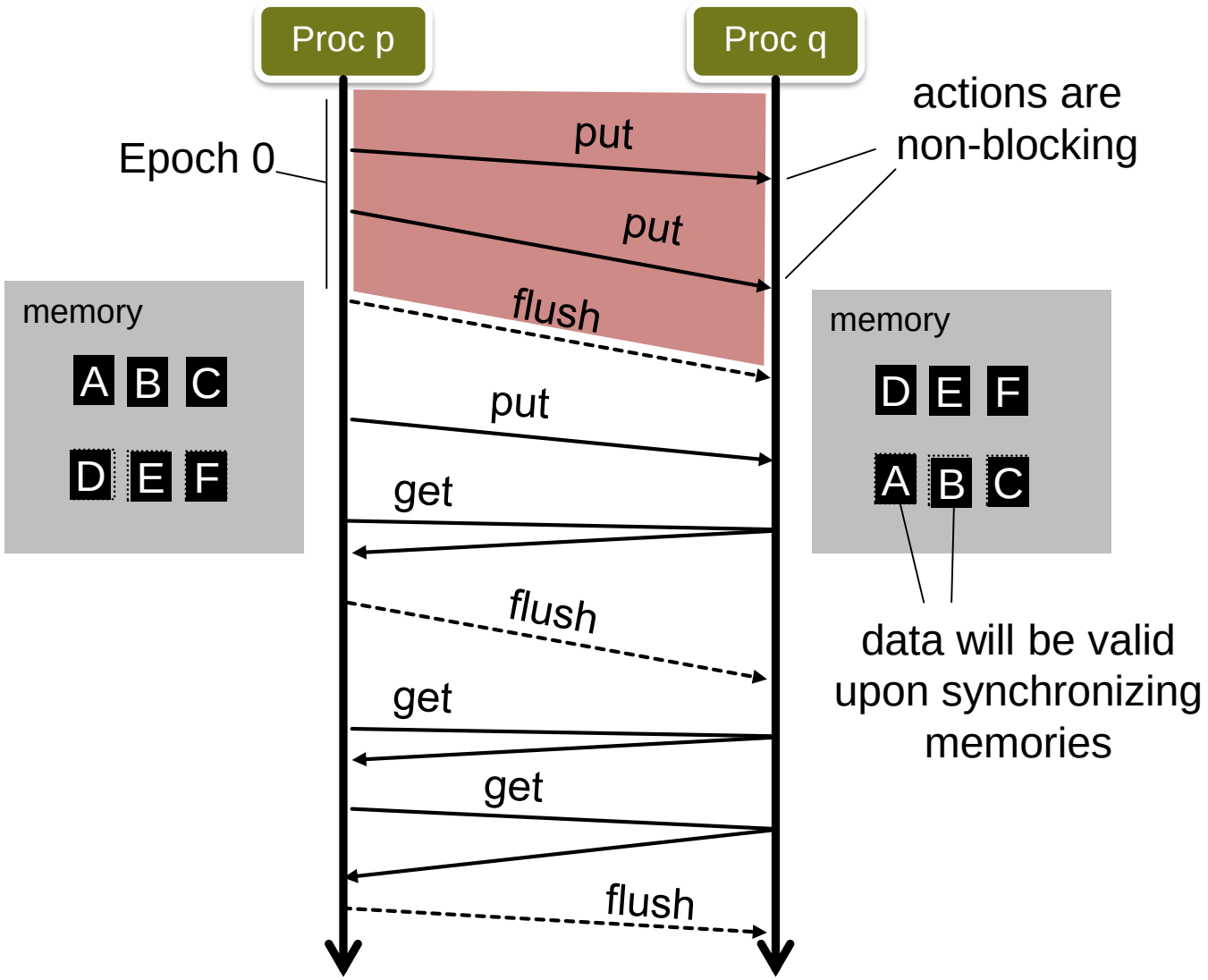
Proc p
Proc q
Epoch 0
put
put
flush
actions are non-blocking
memory
A B C
D E F
memory
D E F
A B C
put
get
flush
get
get
flush
data will be valid upon synchronizing memories

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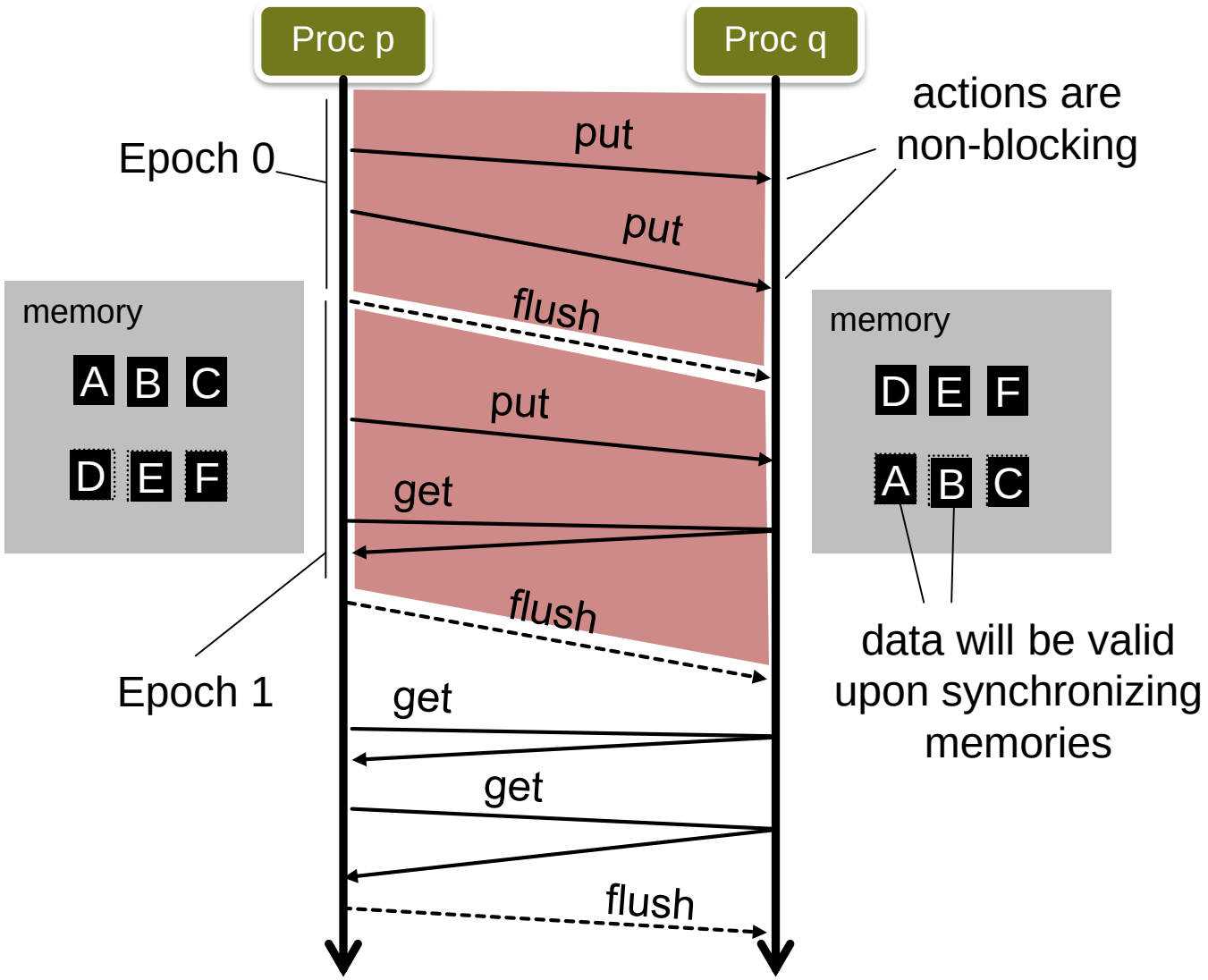
Proc p
Proc q
actions are non-blocking
Epoch 0
put
put
flush
memory
A B C
D E F
put
get
flush
Epoch 1
get
get
flush
memory
D E F
A B C
data will be valid upon synchronizing memories

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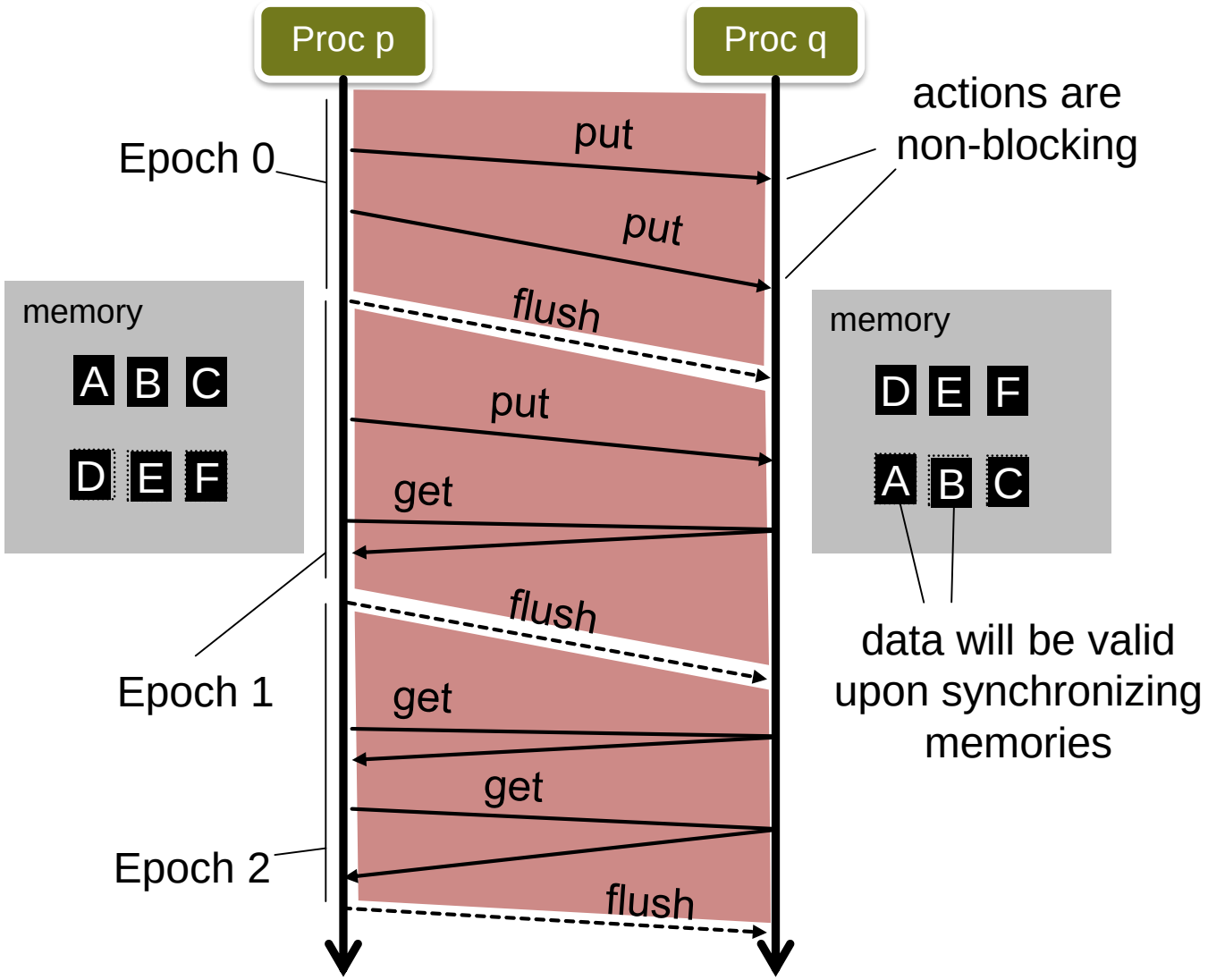
Proc p
Proc q
actions are non-blocking
Epoch 0
put
put
flush
memory
A B C
D E F
put
get
memory
D E F
A B C
flush
Epoch 1
get
get
Epoch 2
flush
data will be valid upon synchronizing memories

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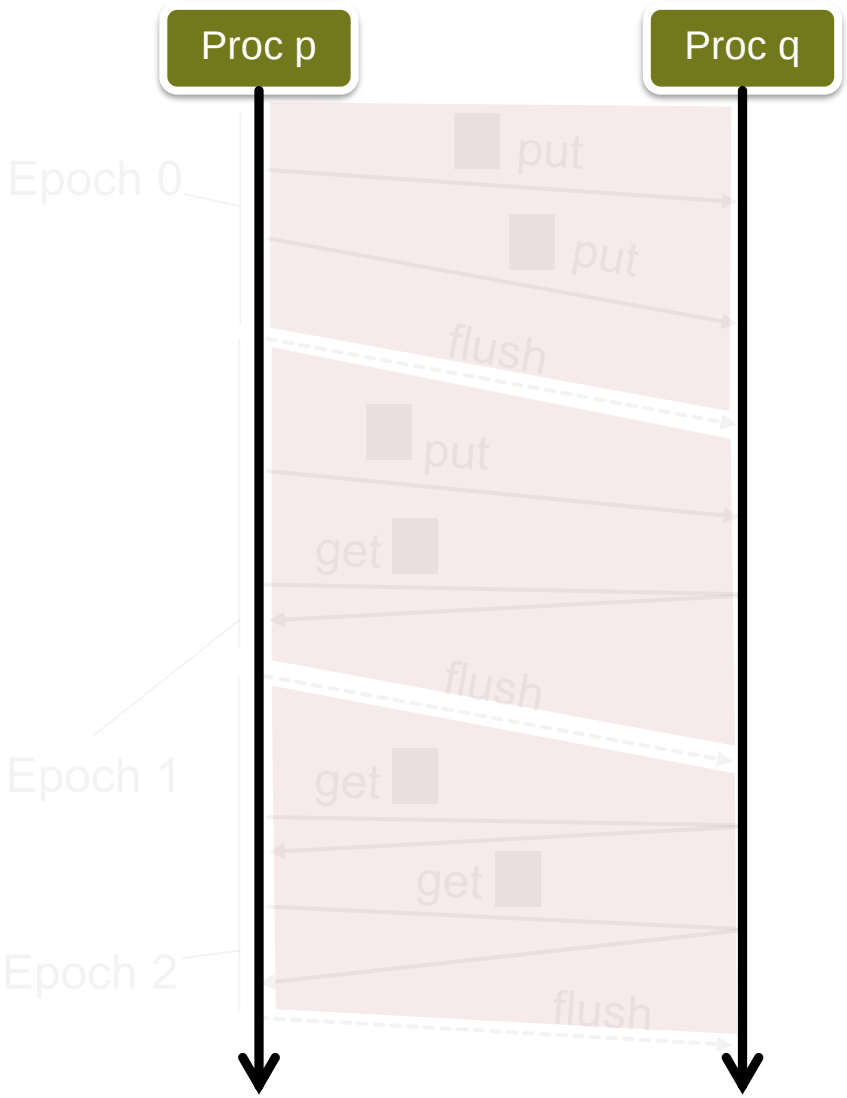
Proc p
Proc q
Epoch 0
put
put
flush
put
get
Epoch 1
flush
get
get
Epoch 2
flush

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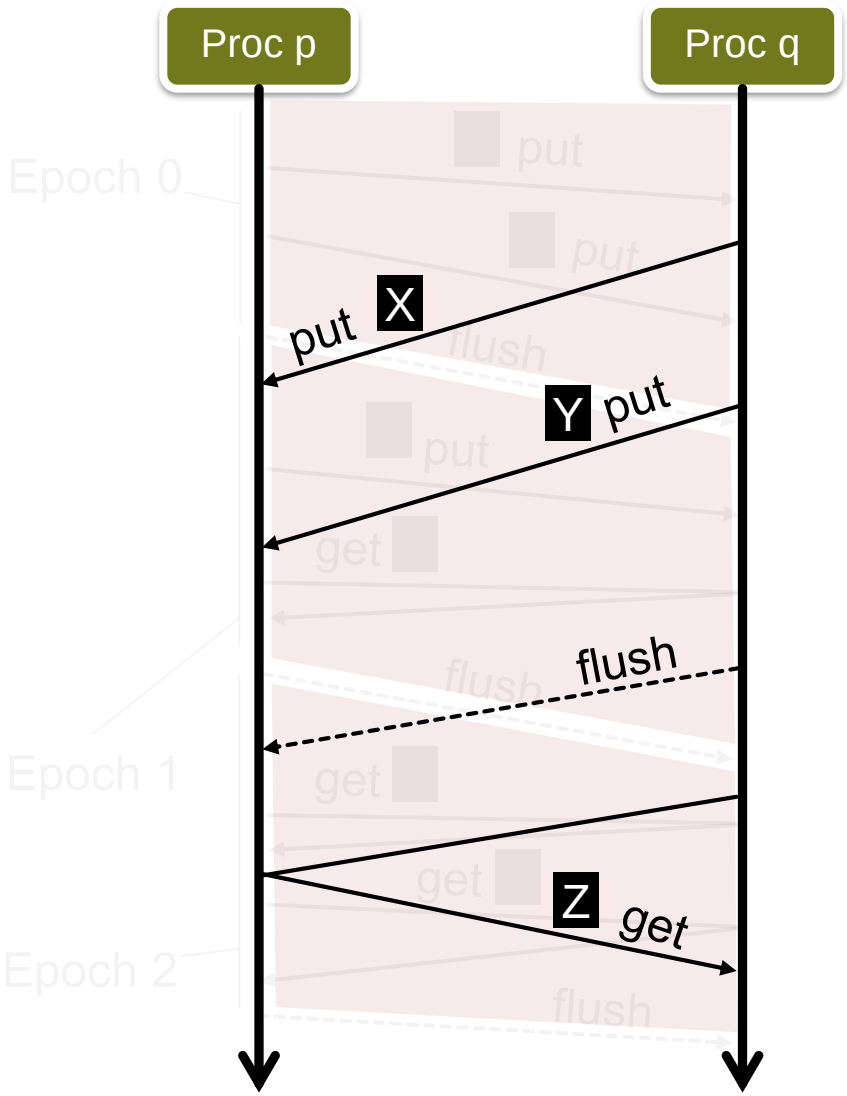
Proc p
Proc q
Epoch 0
Epoch 1
Epoch 2
put
X
Y
put
flush
get
Z
get
flush

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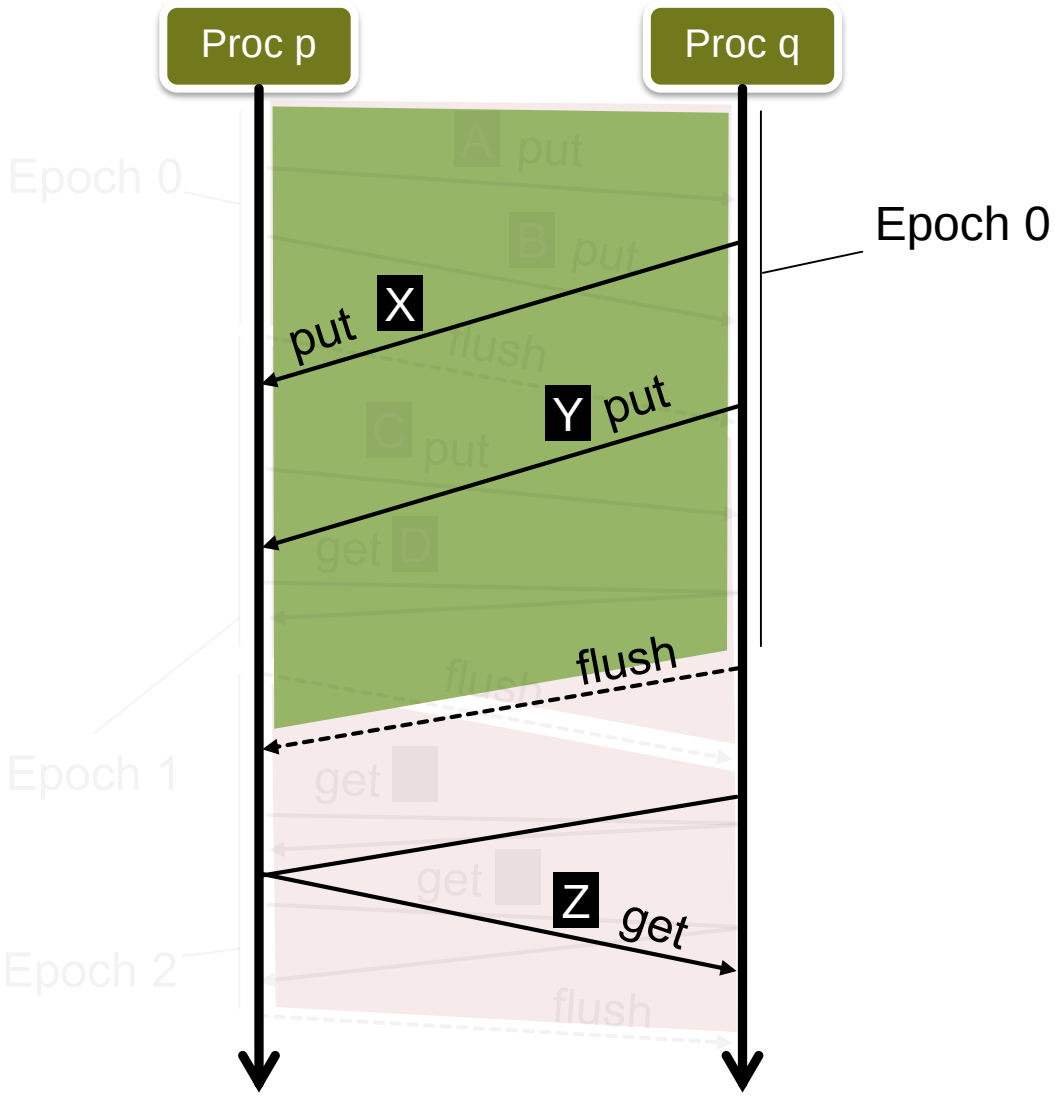
Proc p
Proc q
Epoch 0
put X
Y put
flush
Epoch 1
get
Z get
Epoch 2
flush

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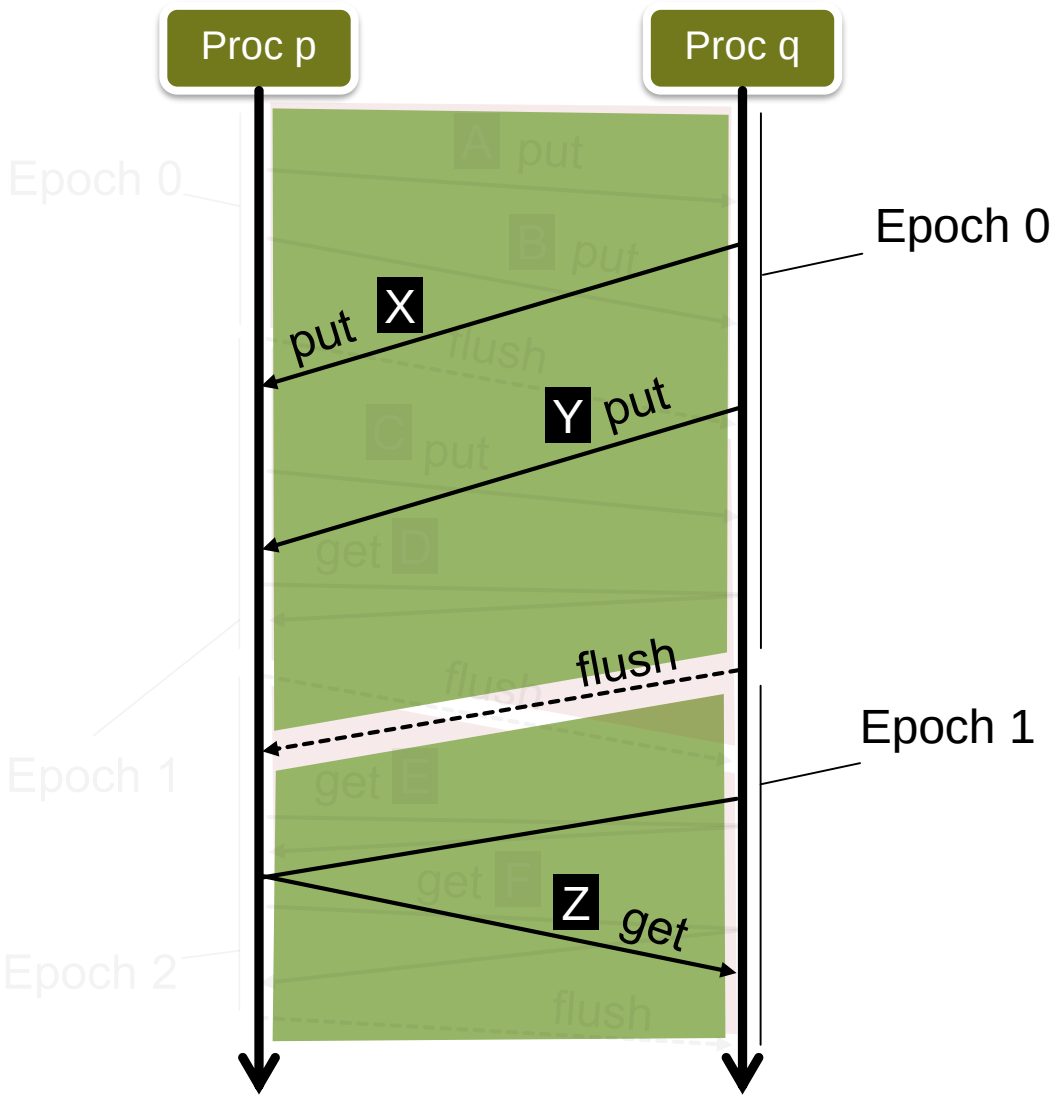

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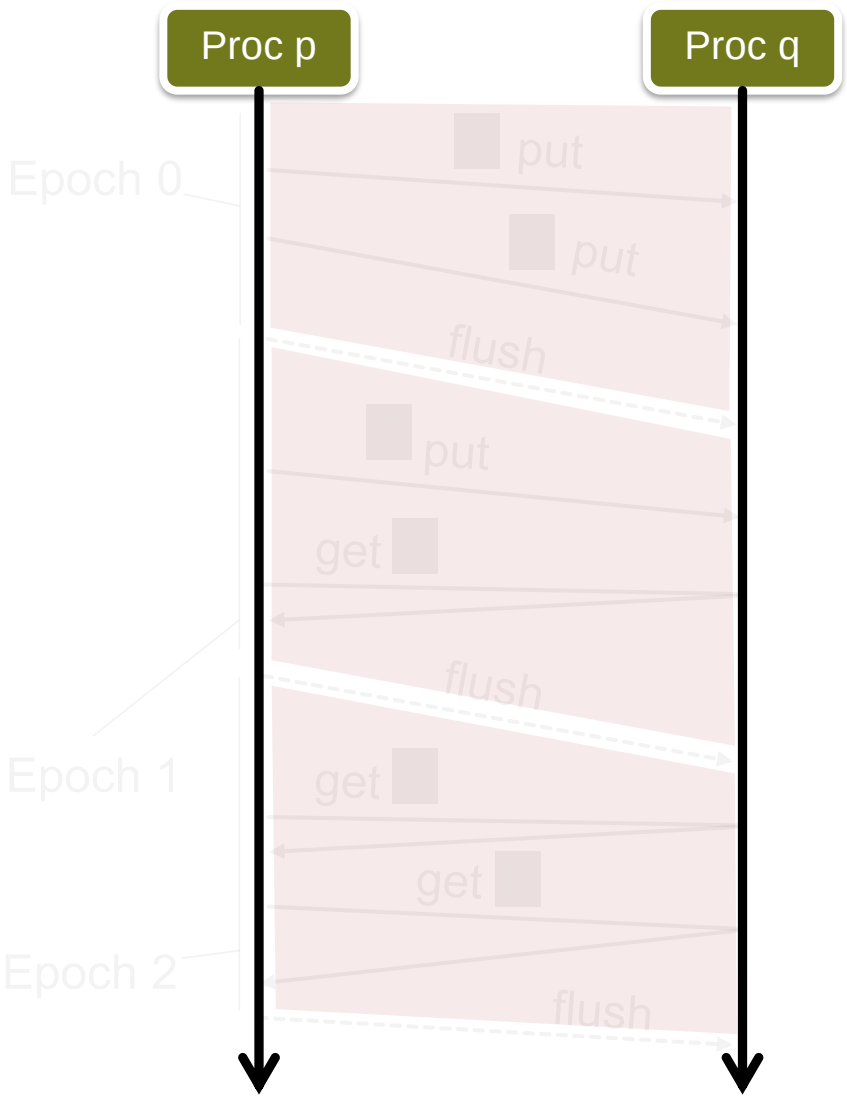
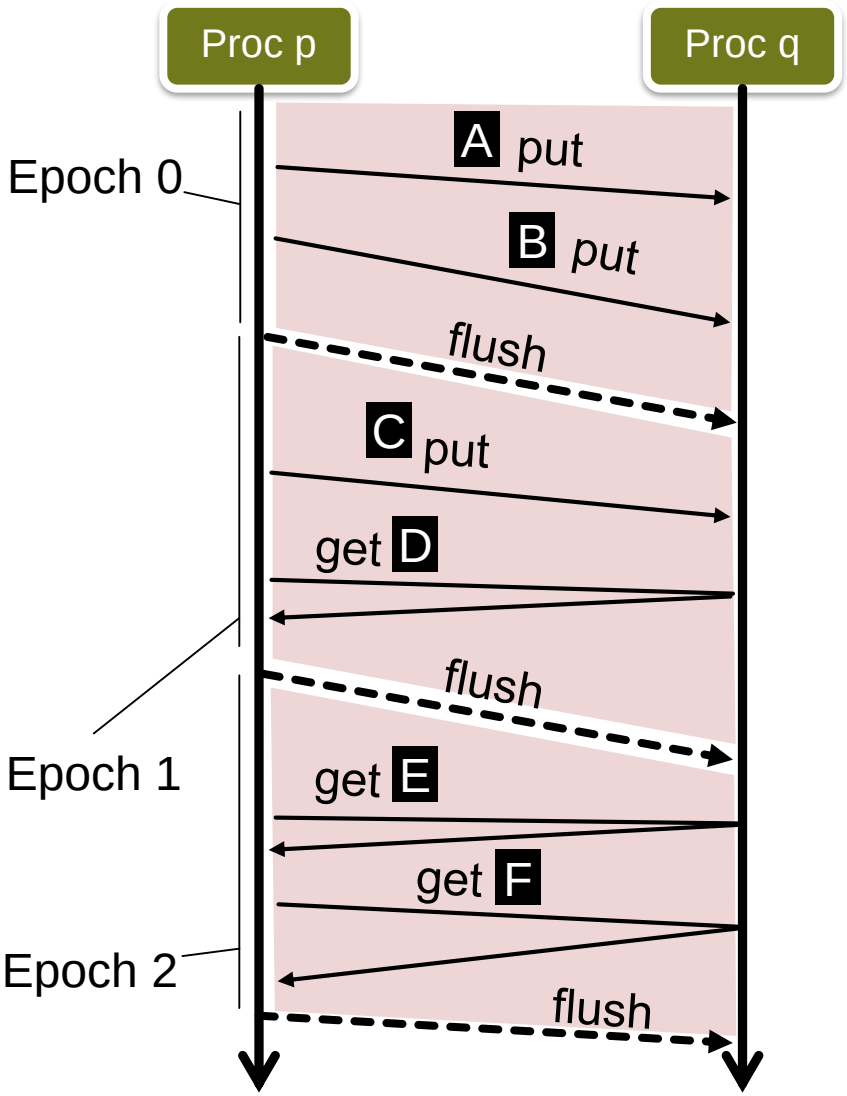

Proc p
Proc q
Epoch 0
put
put
flush
put
get
Epoch 1
flush
get
get
Epoch 2
flush

RMA: The Consistency Order $\xrightarrow{co}$



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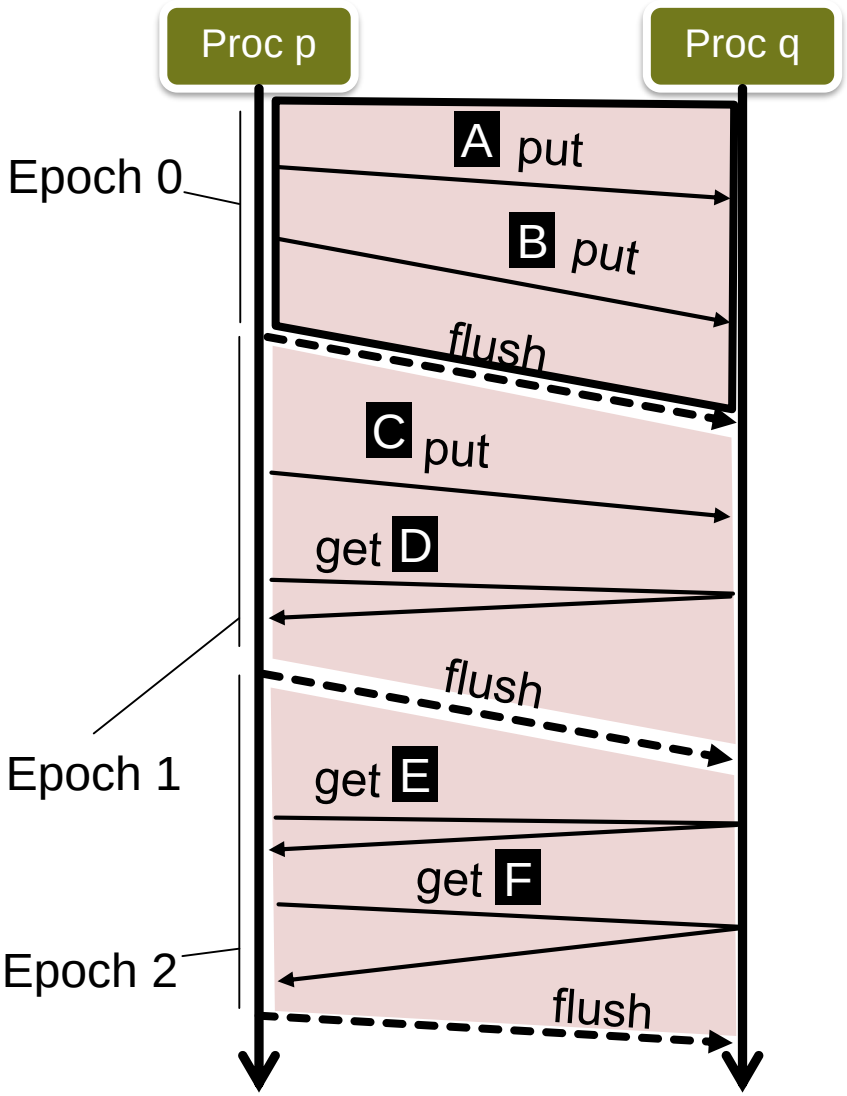

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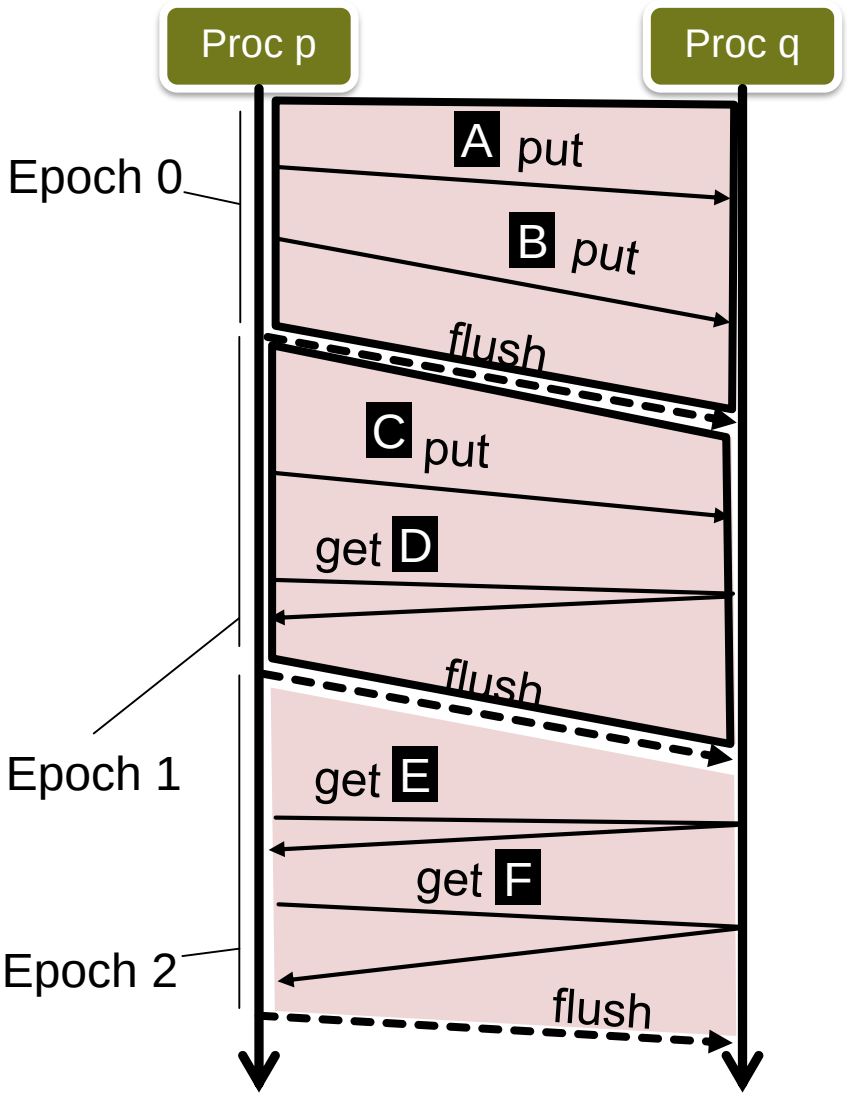

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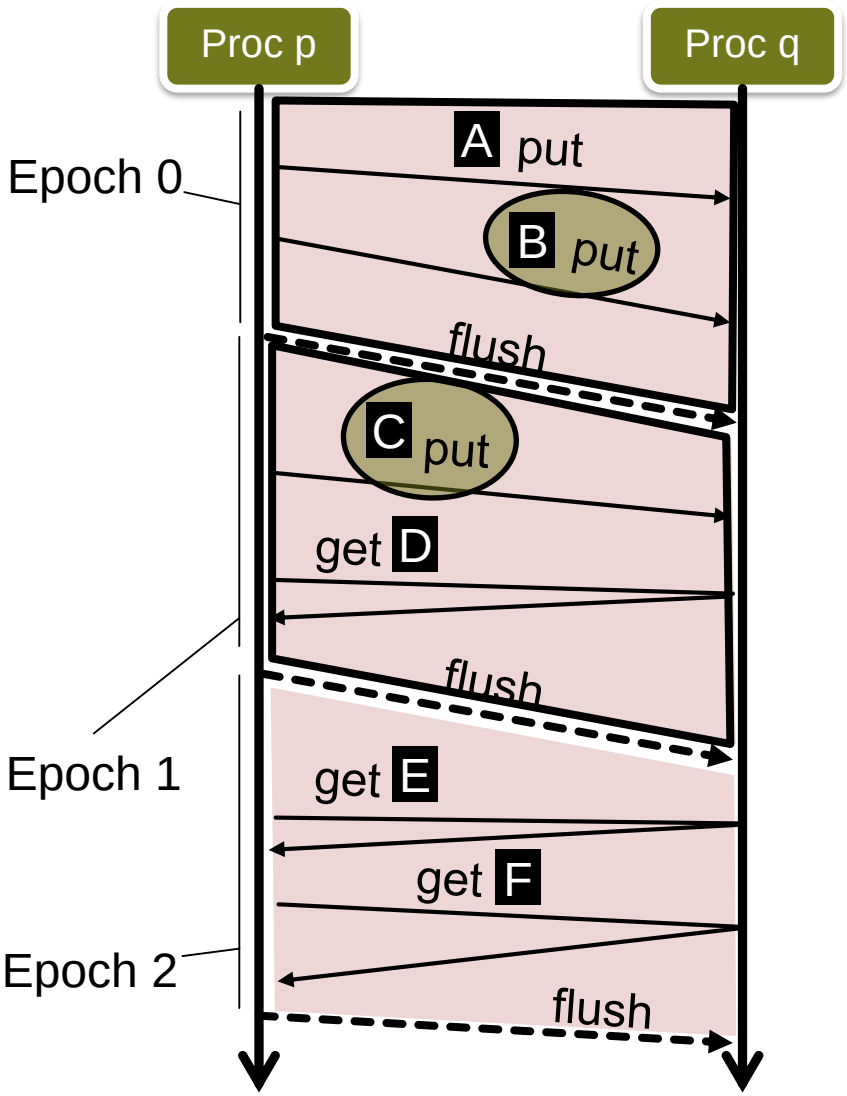

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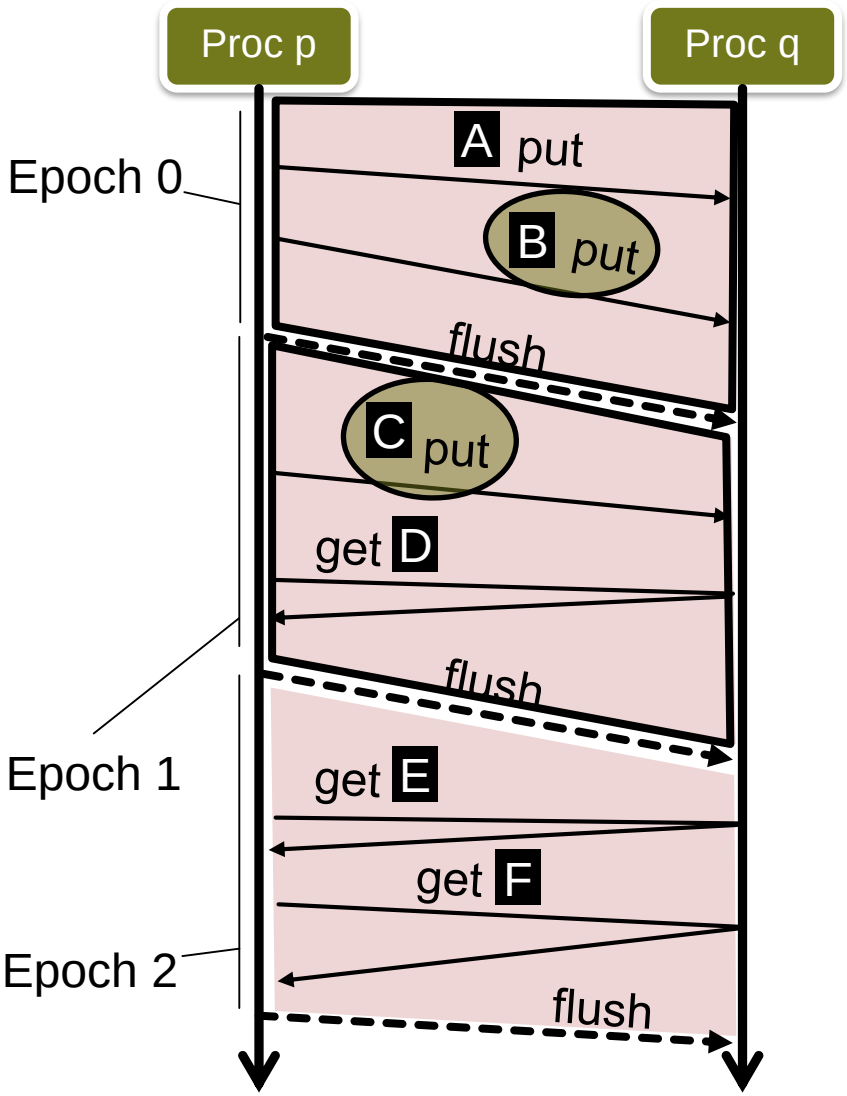

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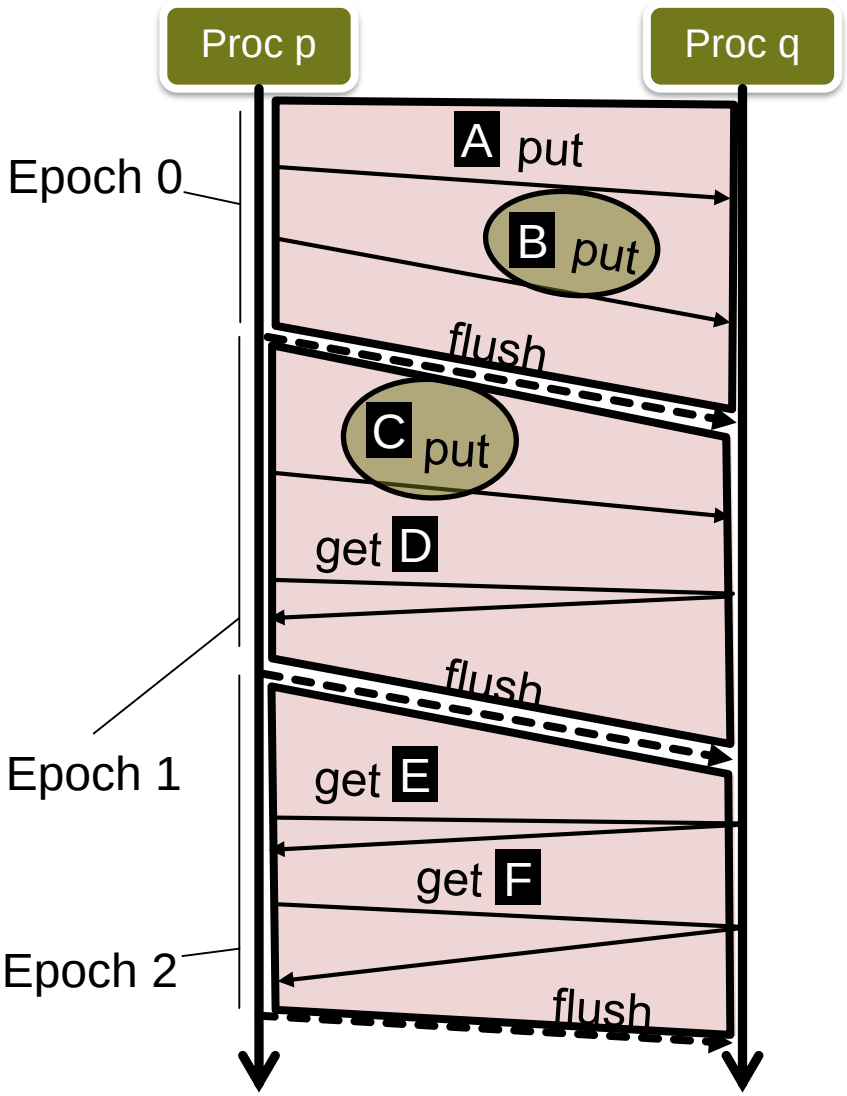

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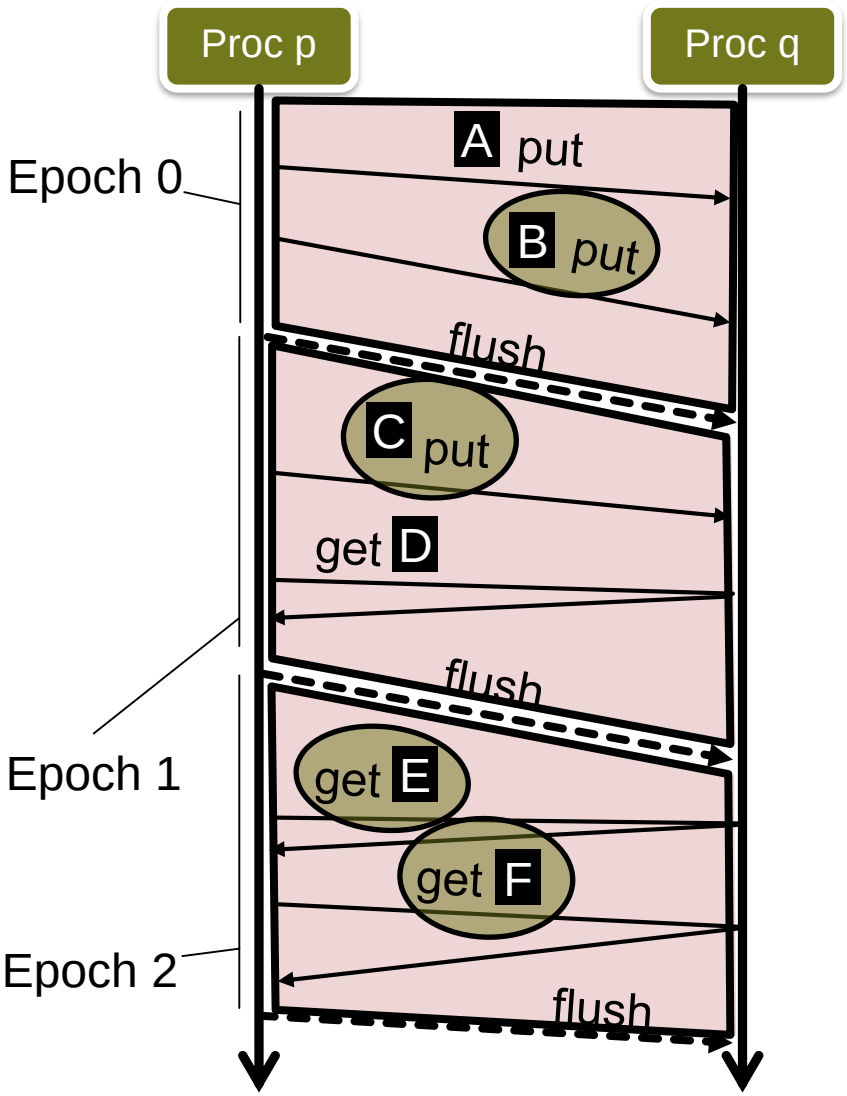

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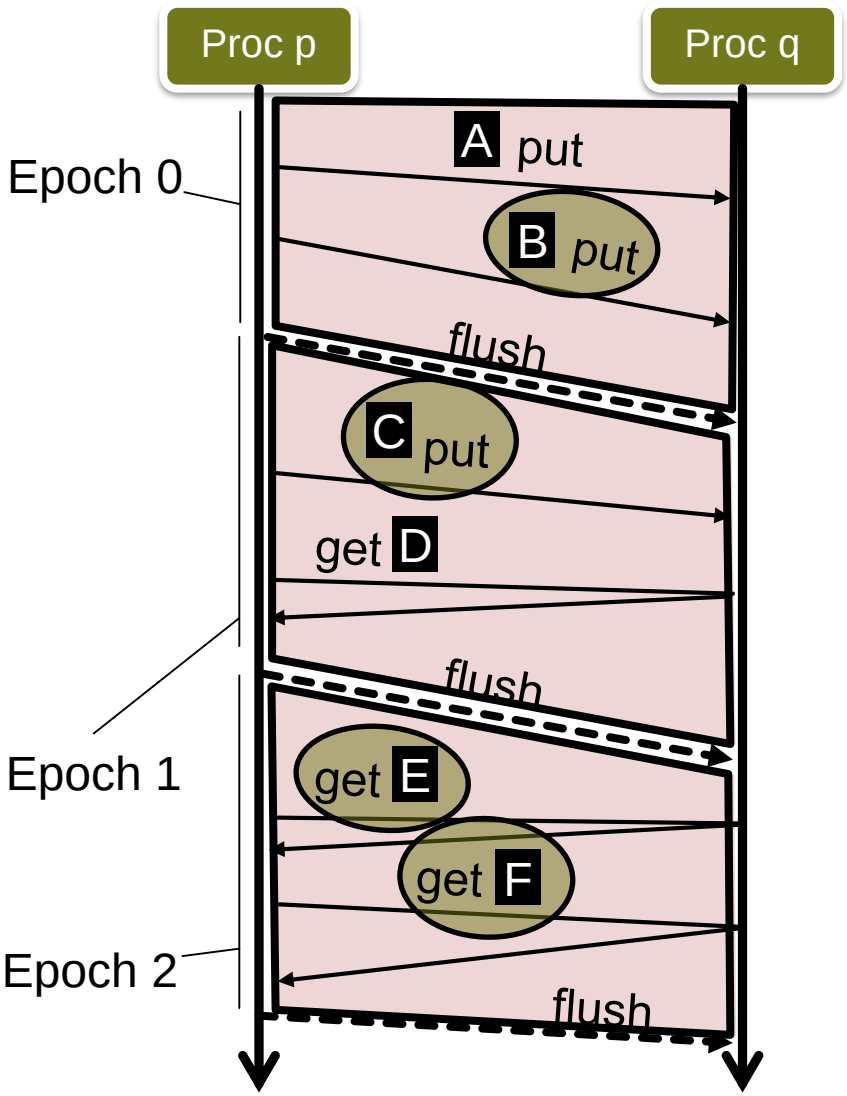

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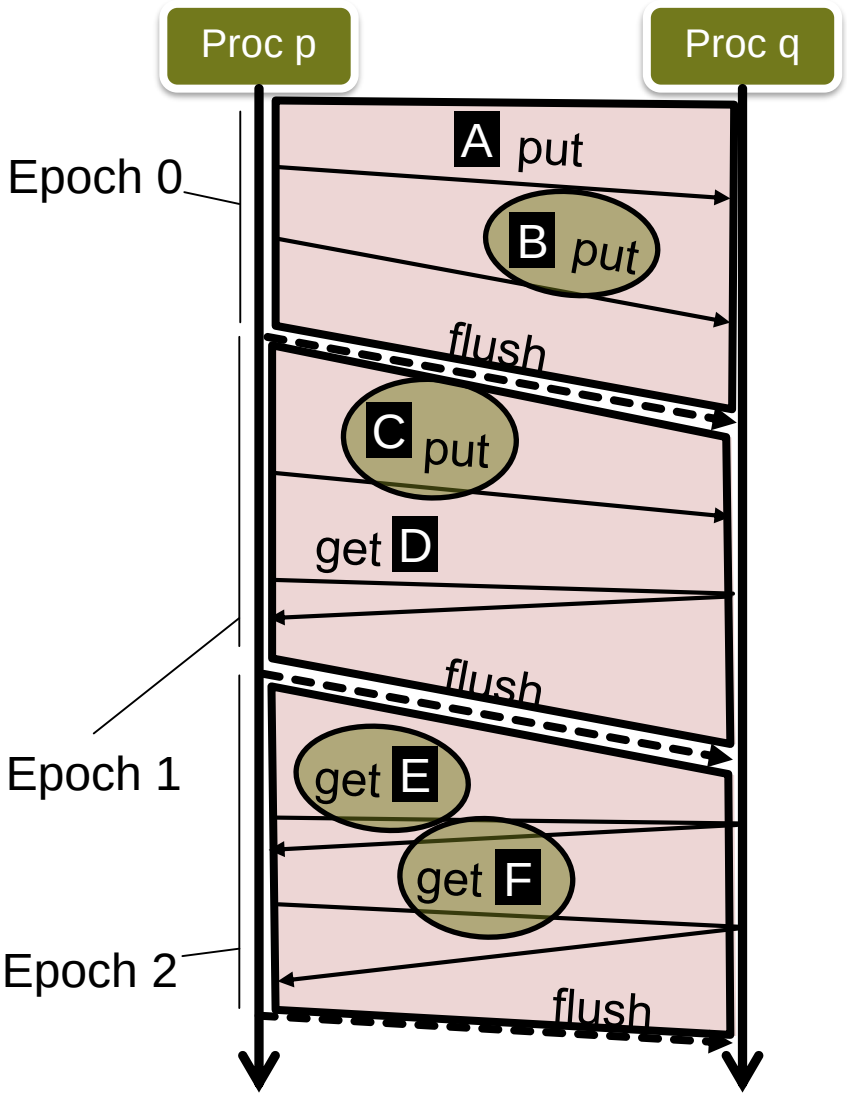

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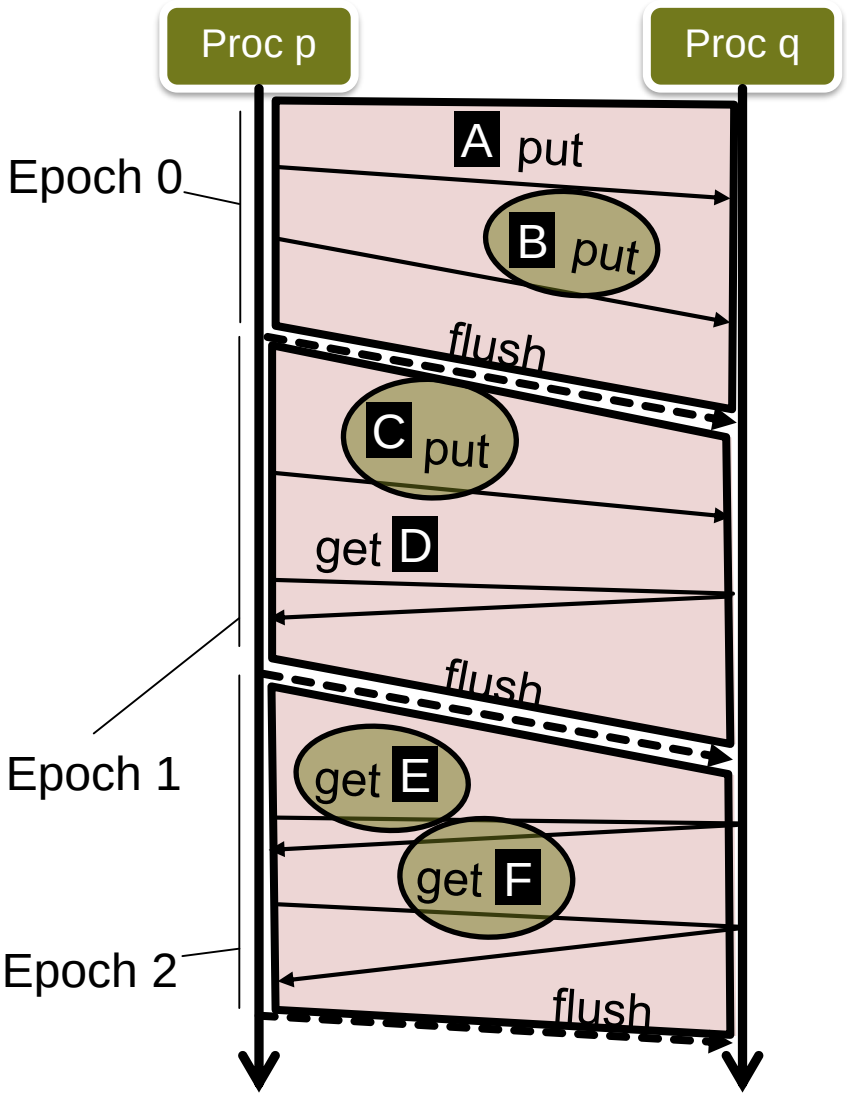

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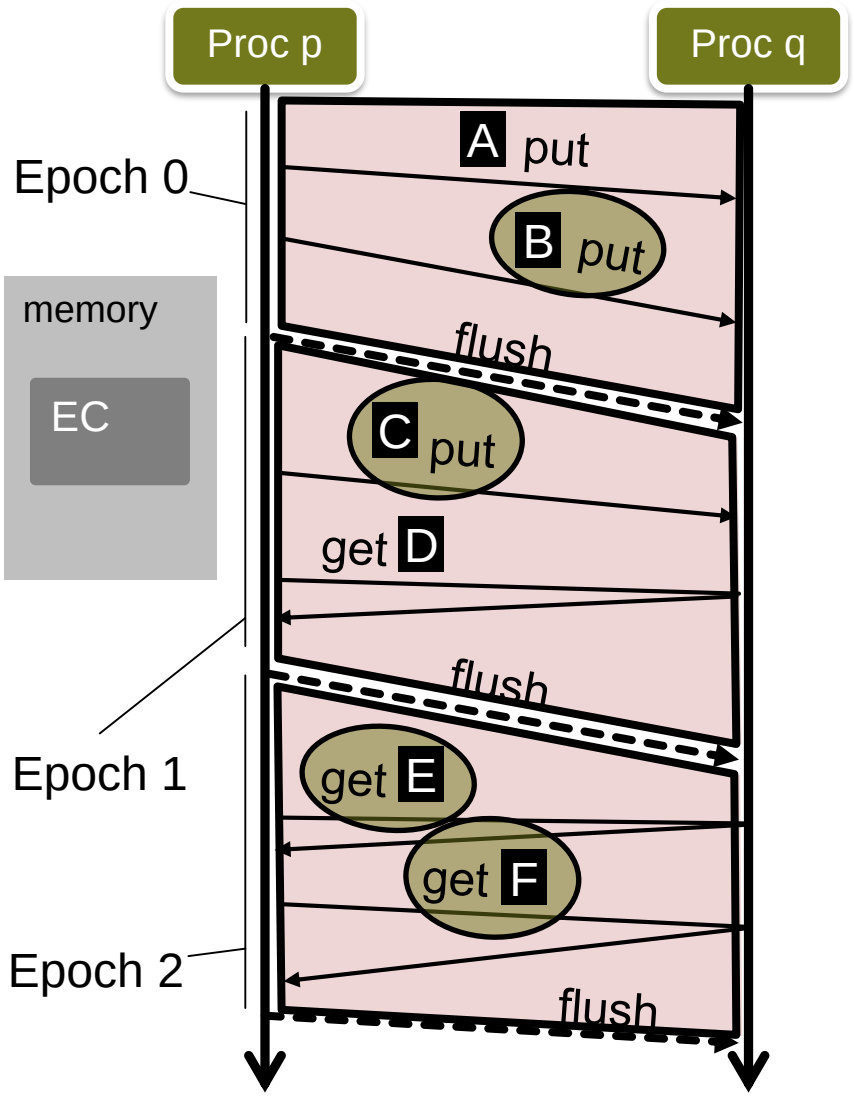

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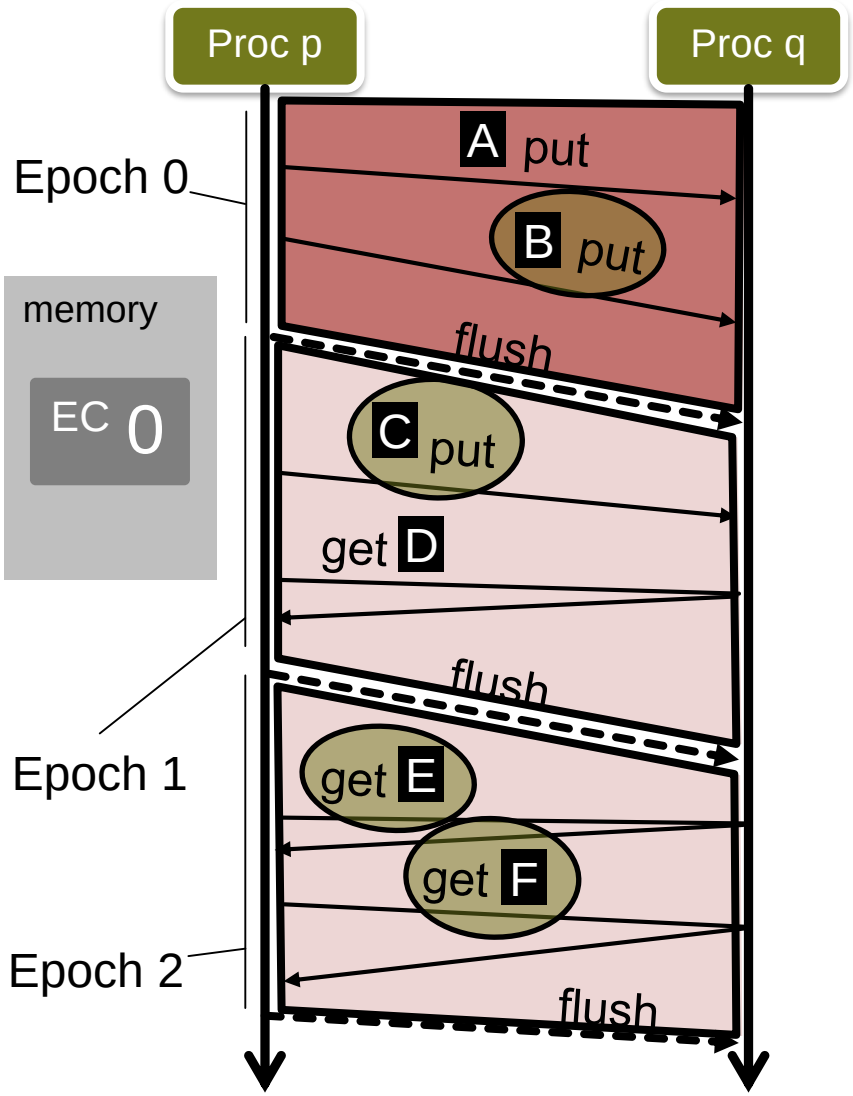

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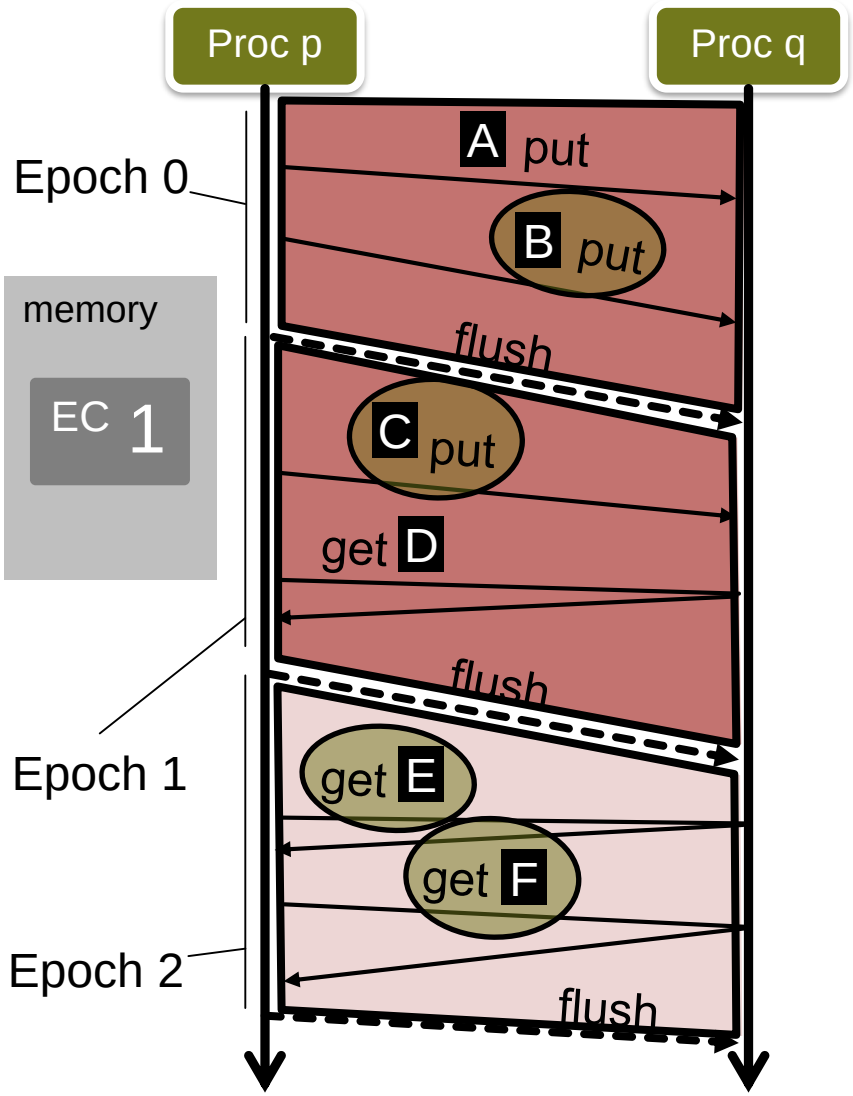

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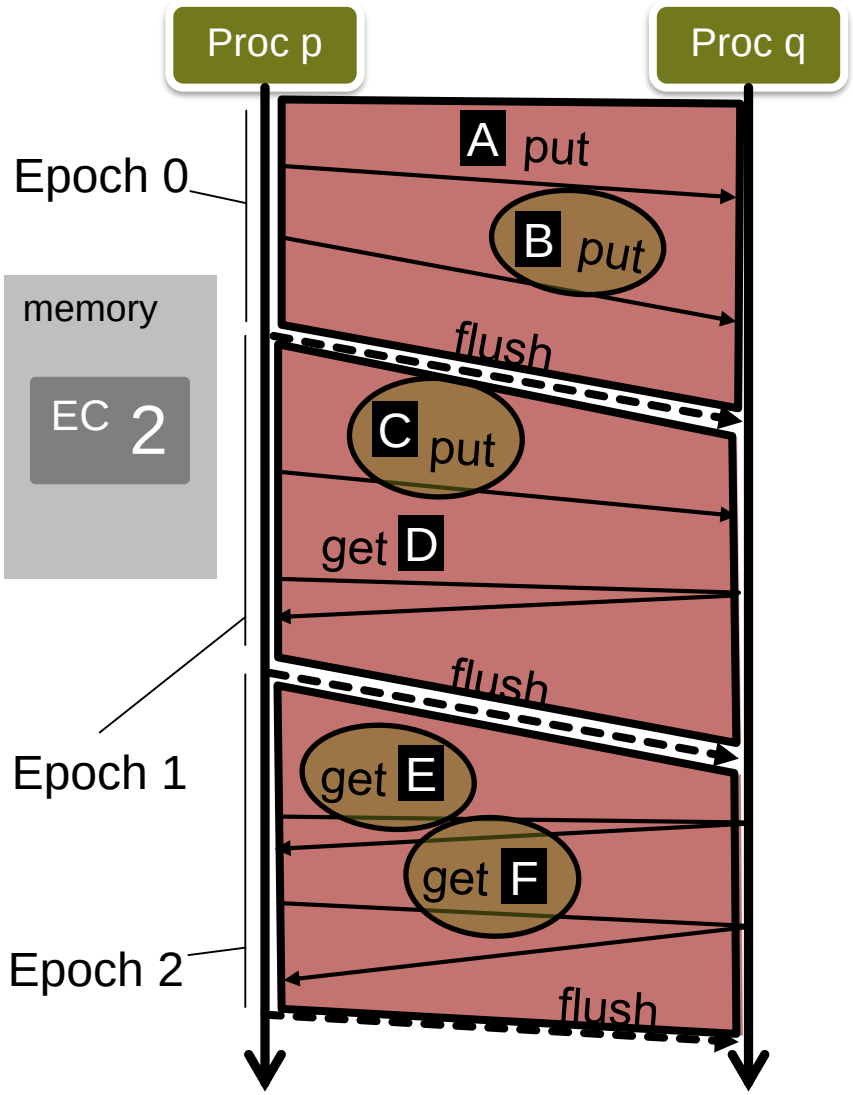

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Overview of our Research

Generic model

$\mathcal{D} = \langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co} \rangle,$

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$\text{GET}(p \leftrightarrows q)$

MPI-2 PGAS

CC in RMA

MP vs. RMA

Schemes

UC in RMA

MP vs. RMA

Checkpointing schemes

Logging accesses

Recovery in RMA

Basic scheme

Extended RMA semantics

Proofs

Theorem 4.2. *The recove rithm 2 preserves the* $\xrightarrow{cohb}$ *or ferred to as the* gsync order*).*

Deadlock freedom
Correct recovery

Topology-awareness

$\langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \mathcal{H}, \mathcal{G}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co}, \mathcal{M} \rangle$

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Decreasing failure prob.

Holistic fault-tolerance library

Design

Checkpoints on demand

Optimizations

Performance

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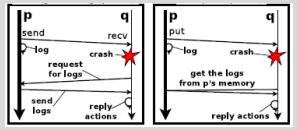

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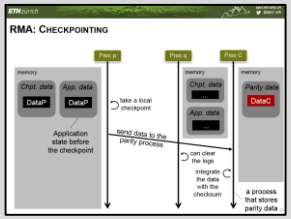

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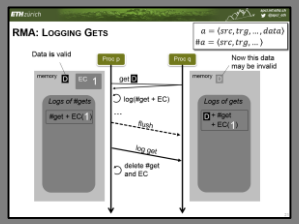

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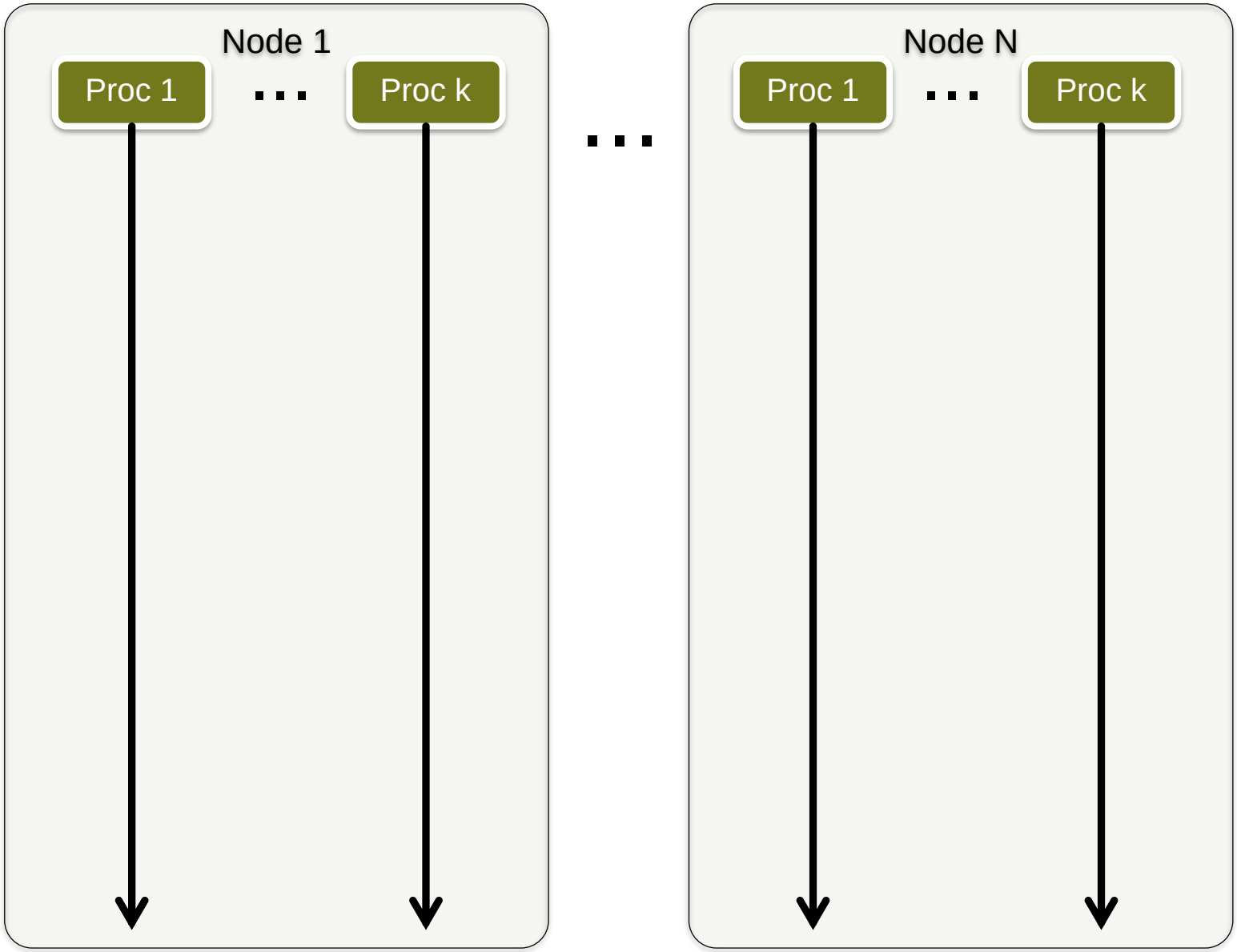

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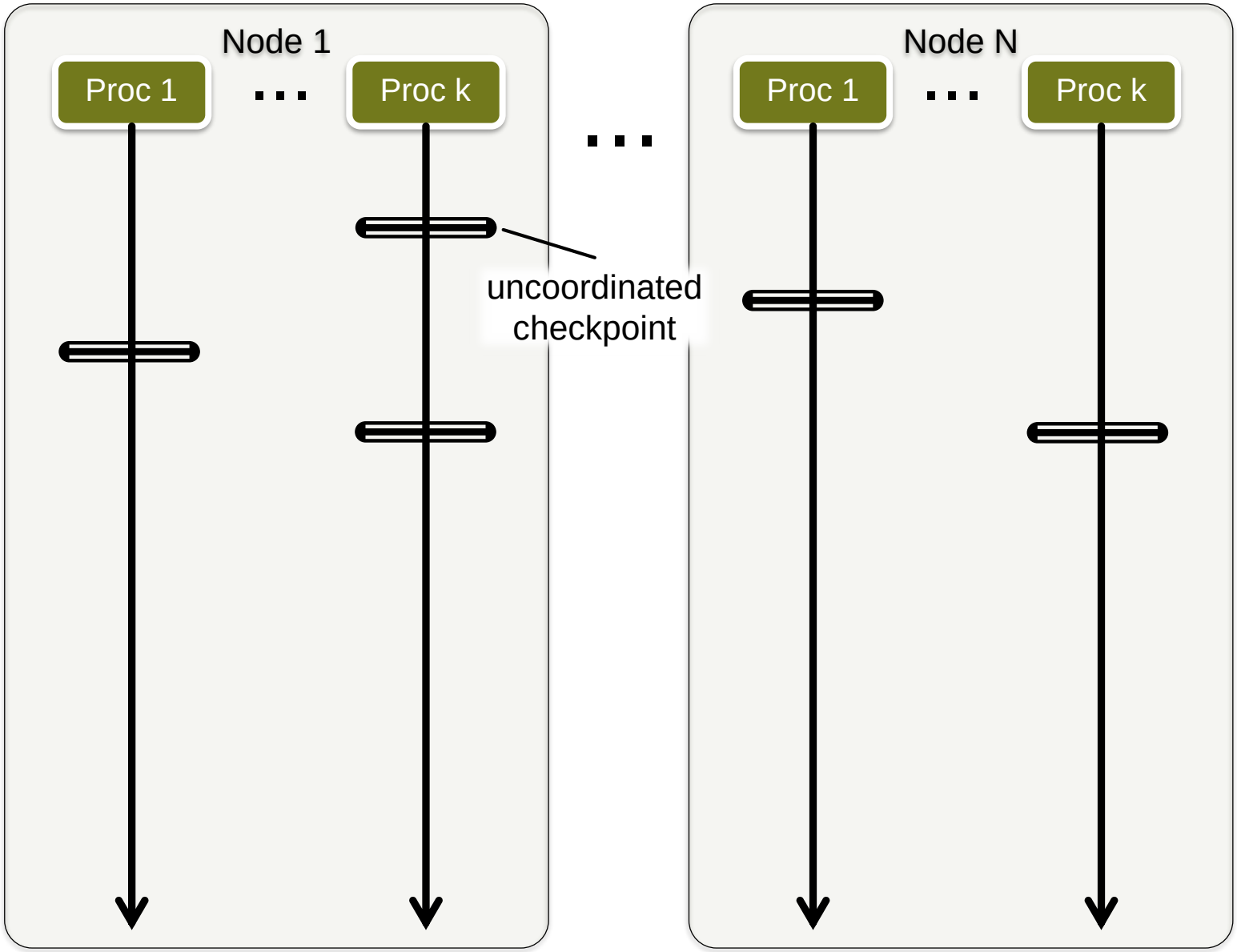

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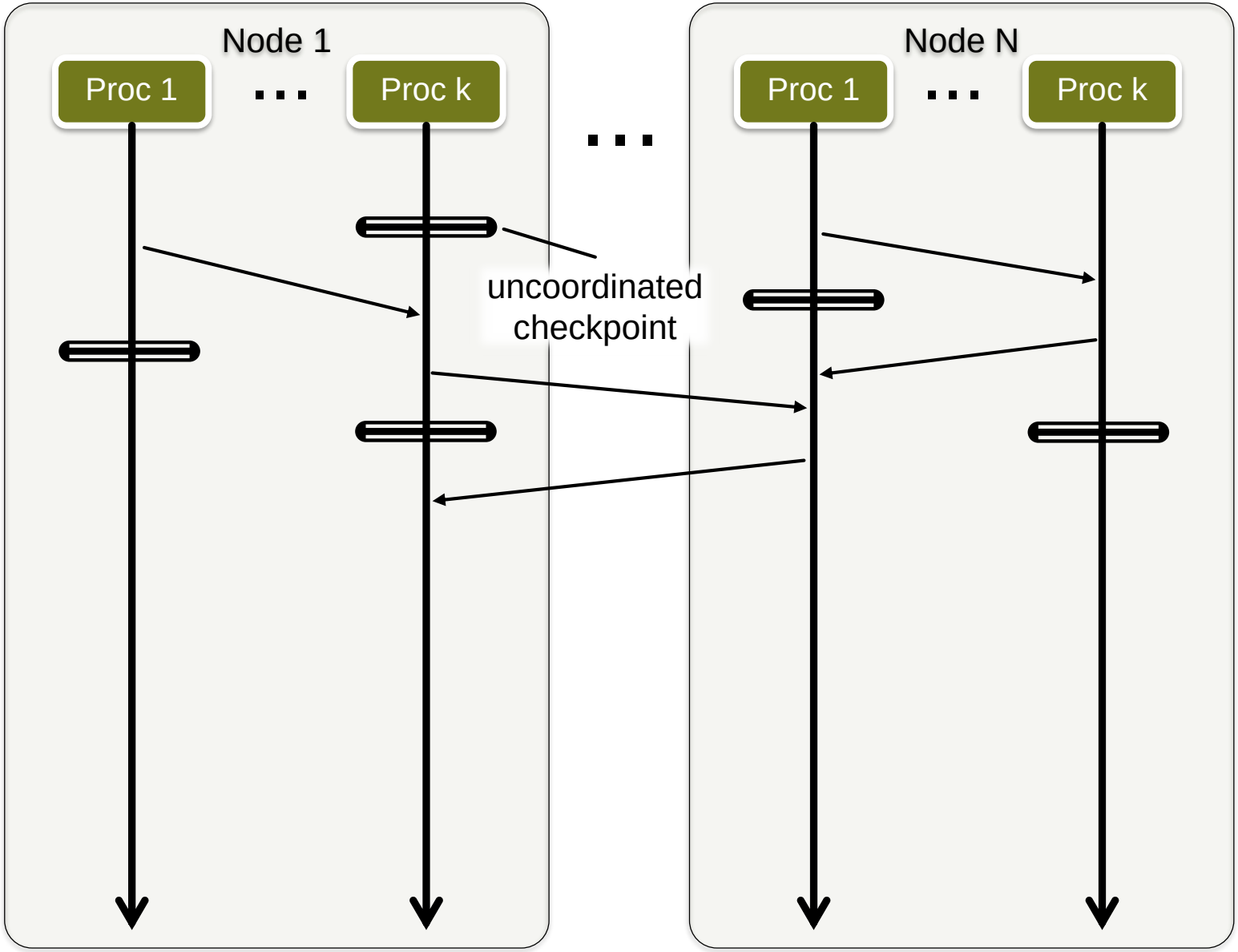

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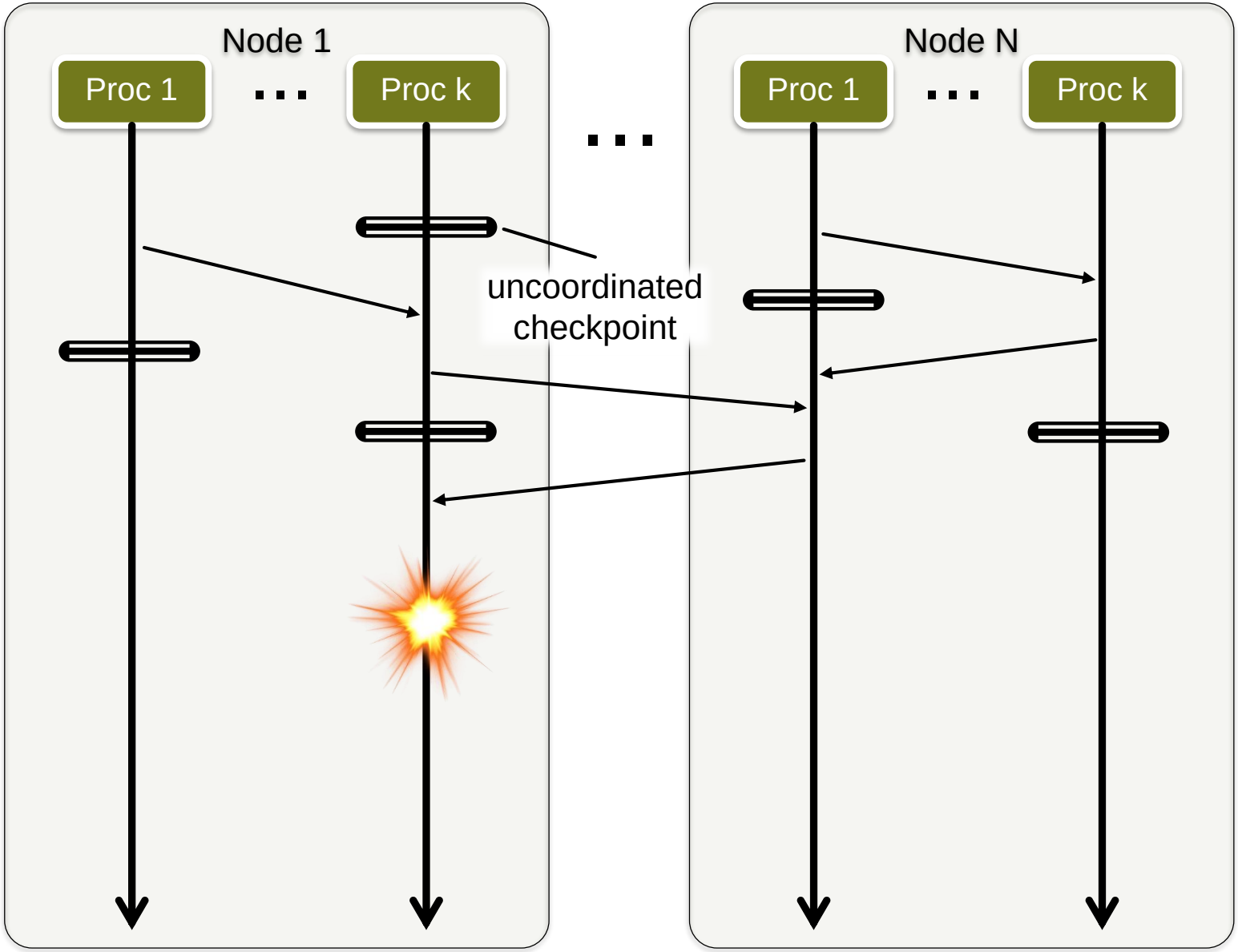

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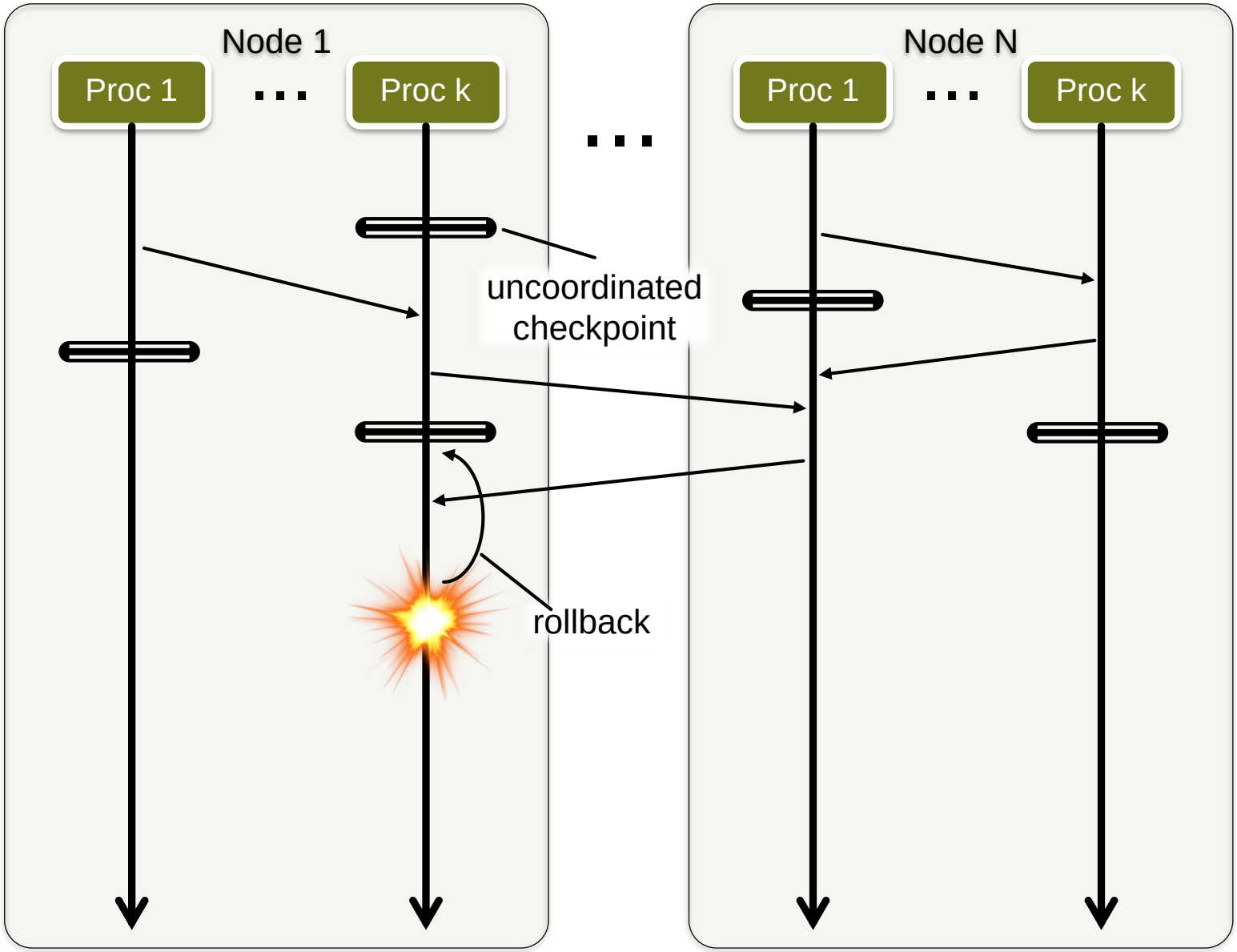

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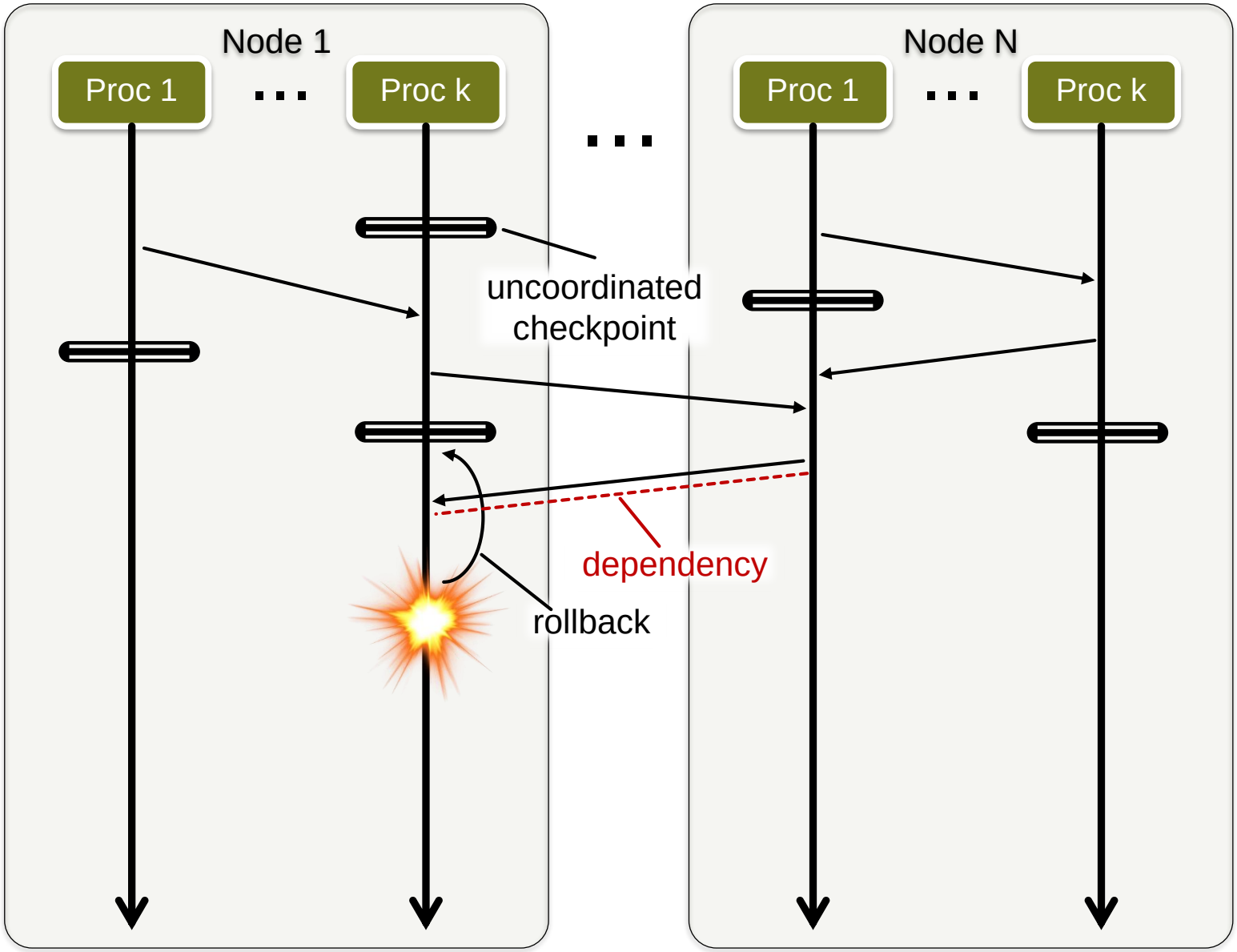

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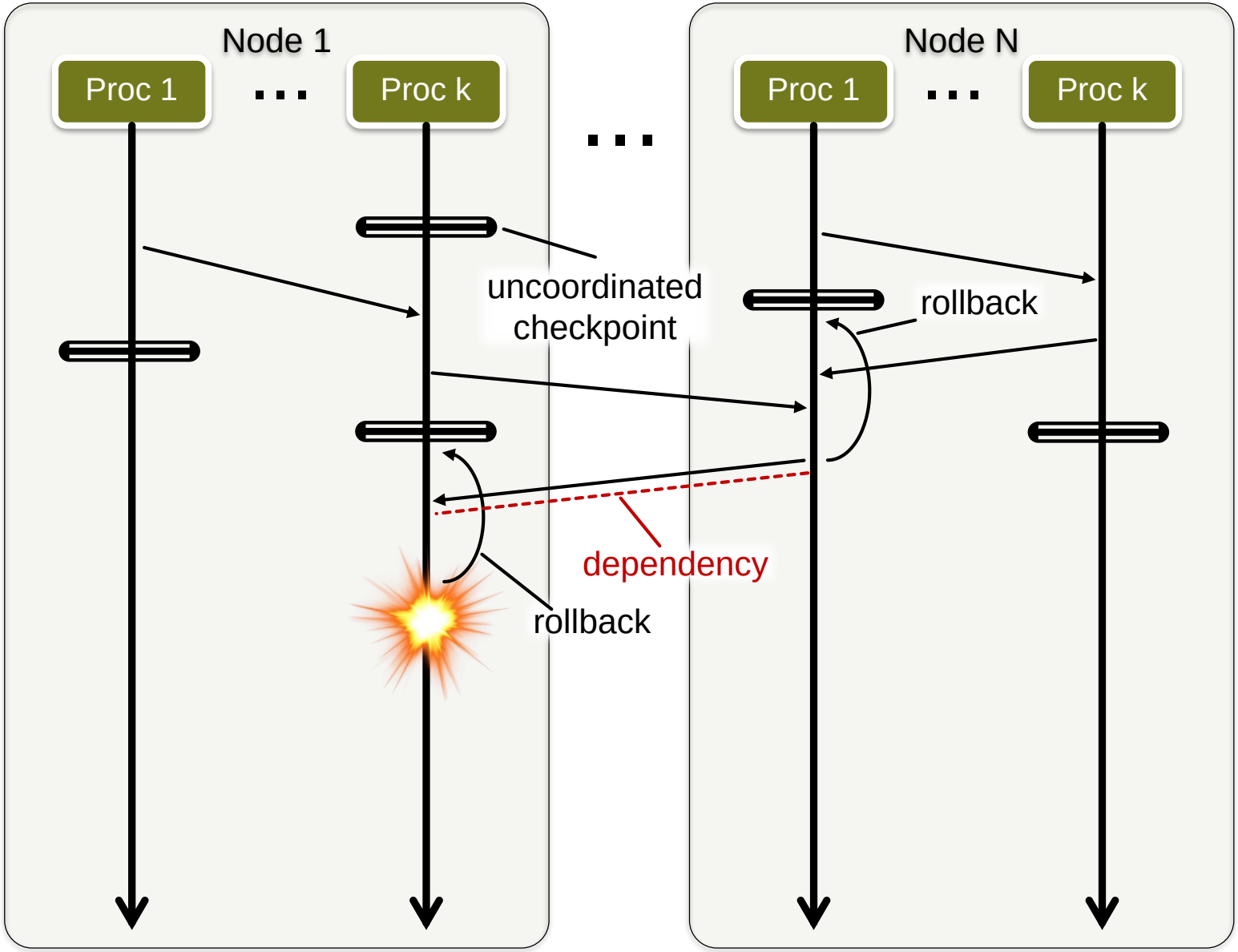

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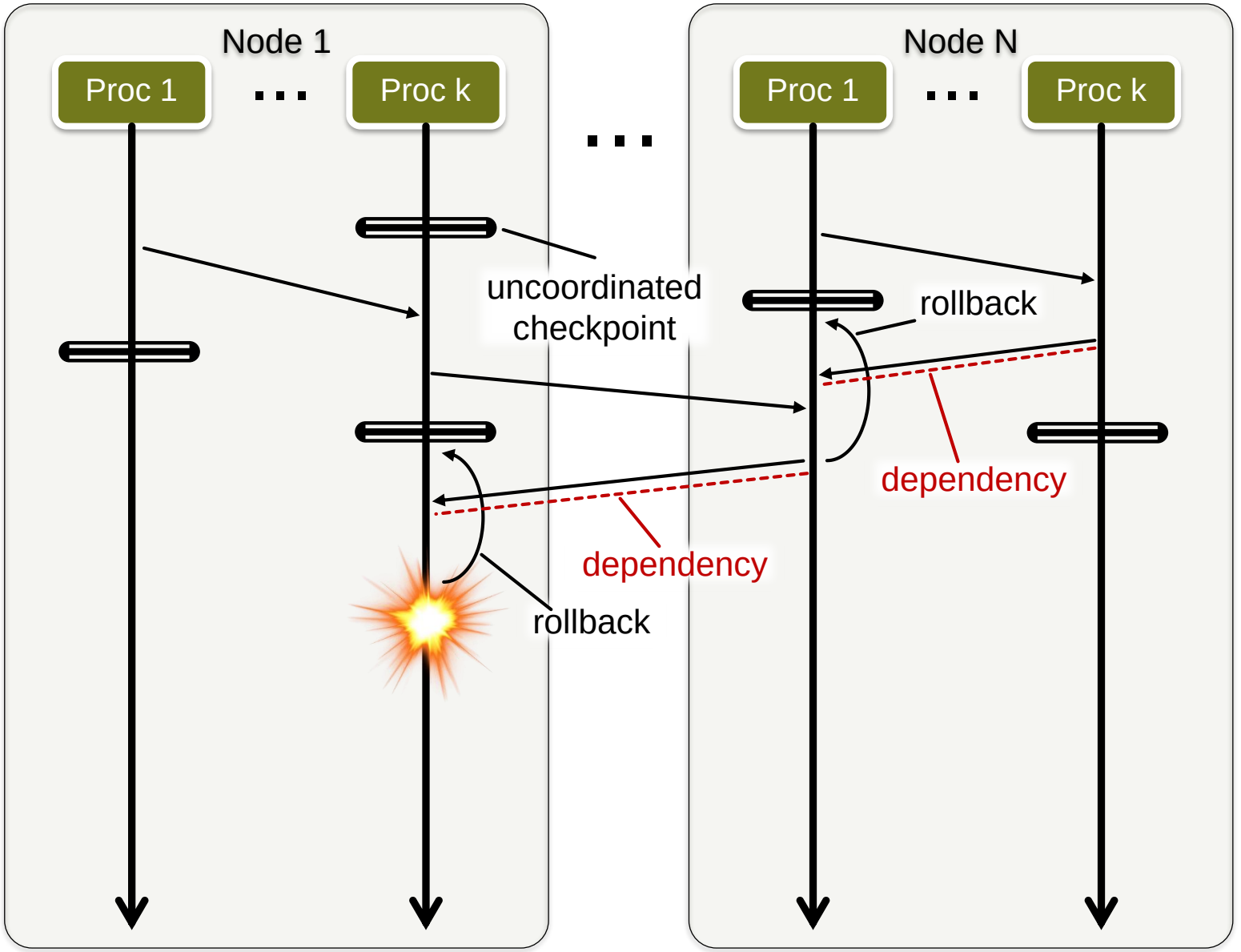

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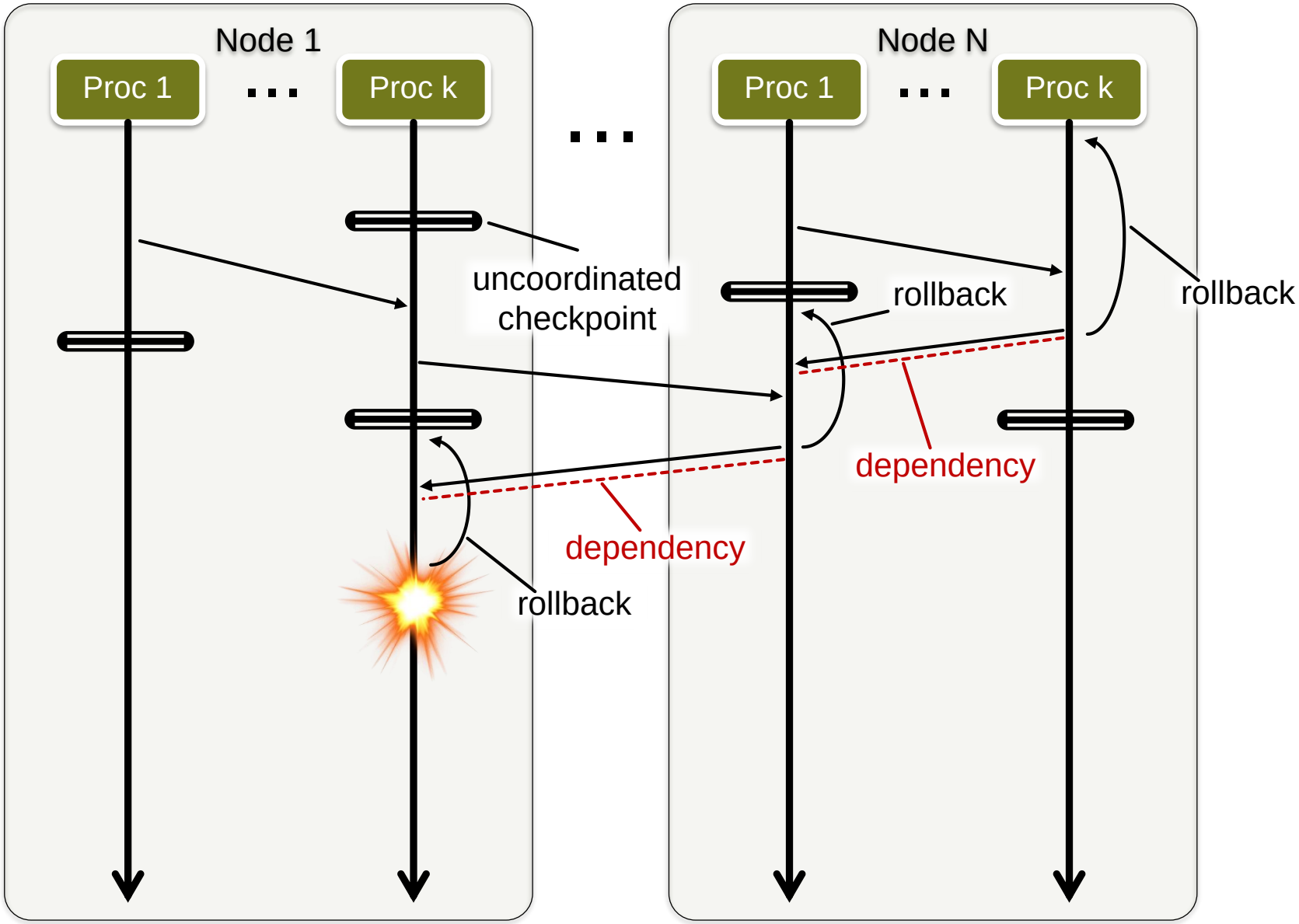

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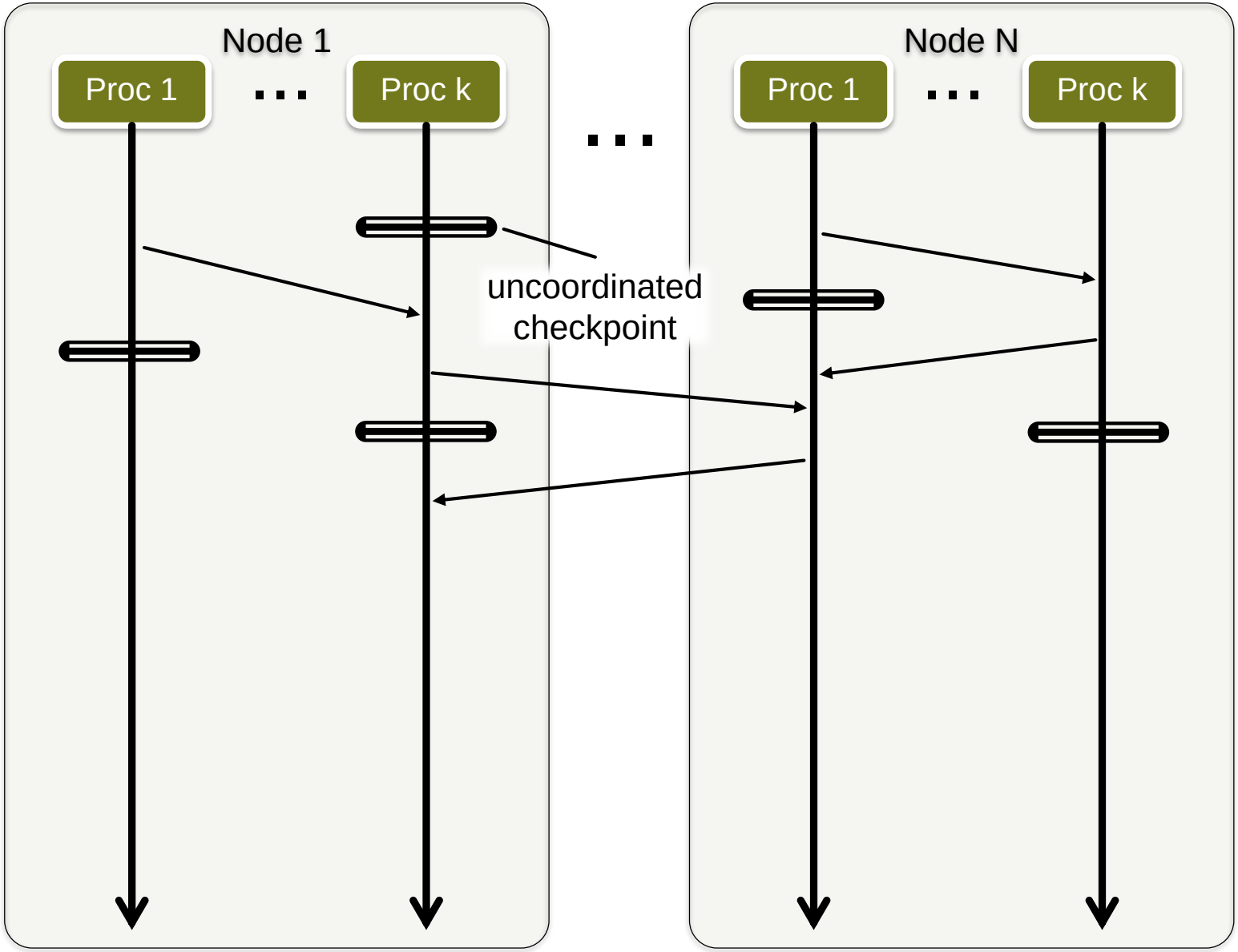

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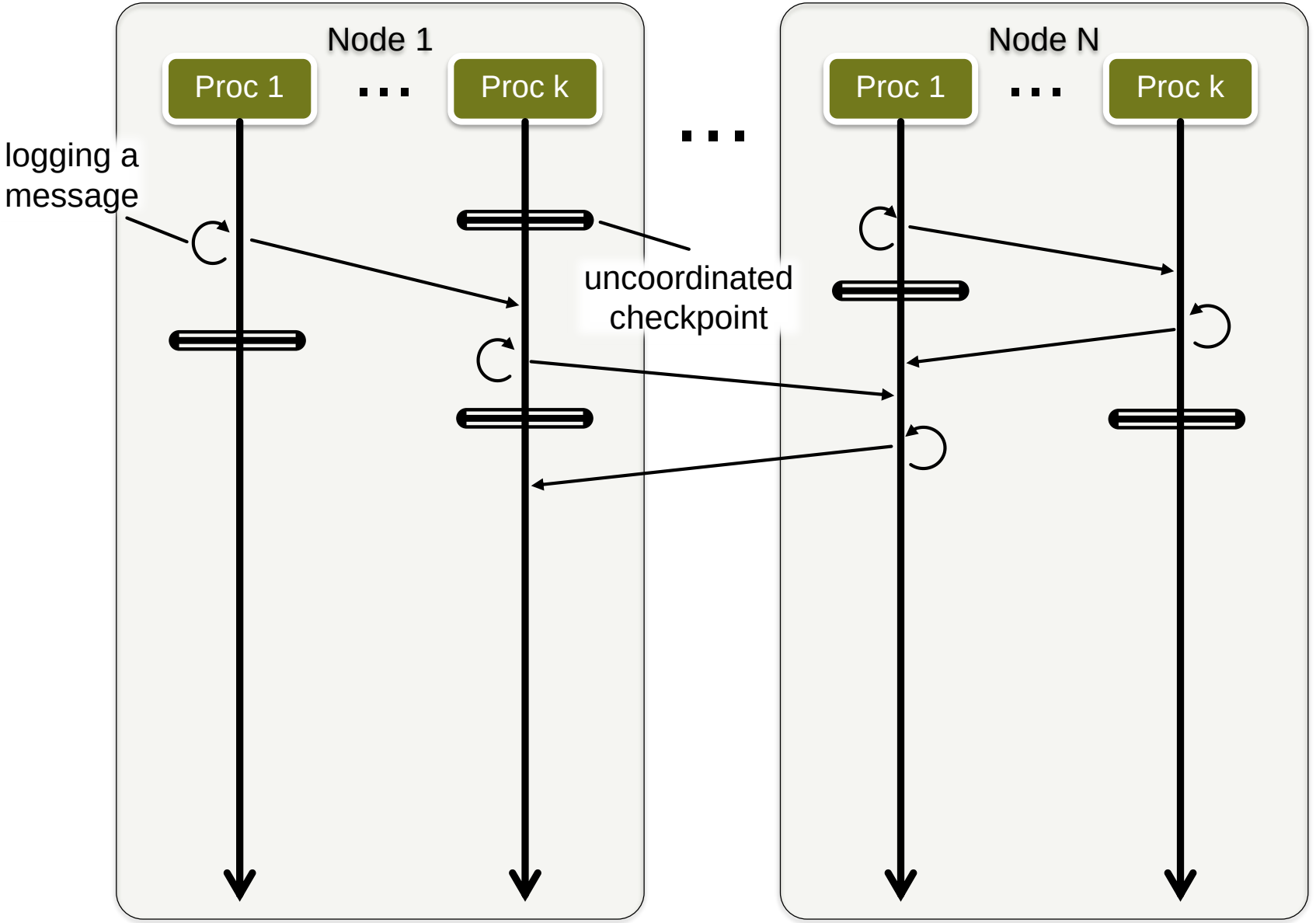

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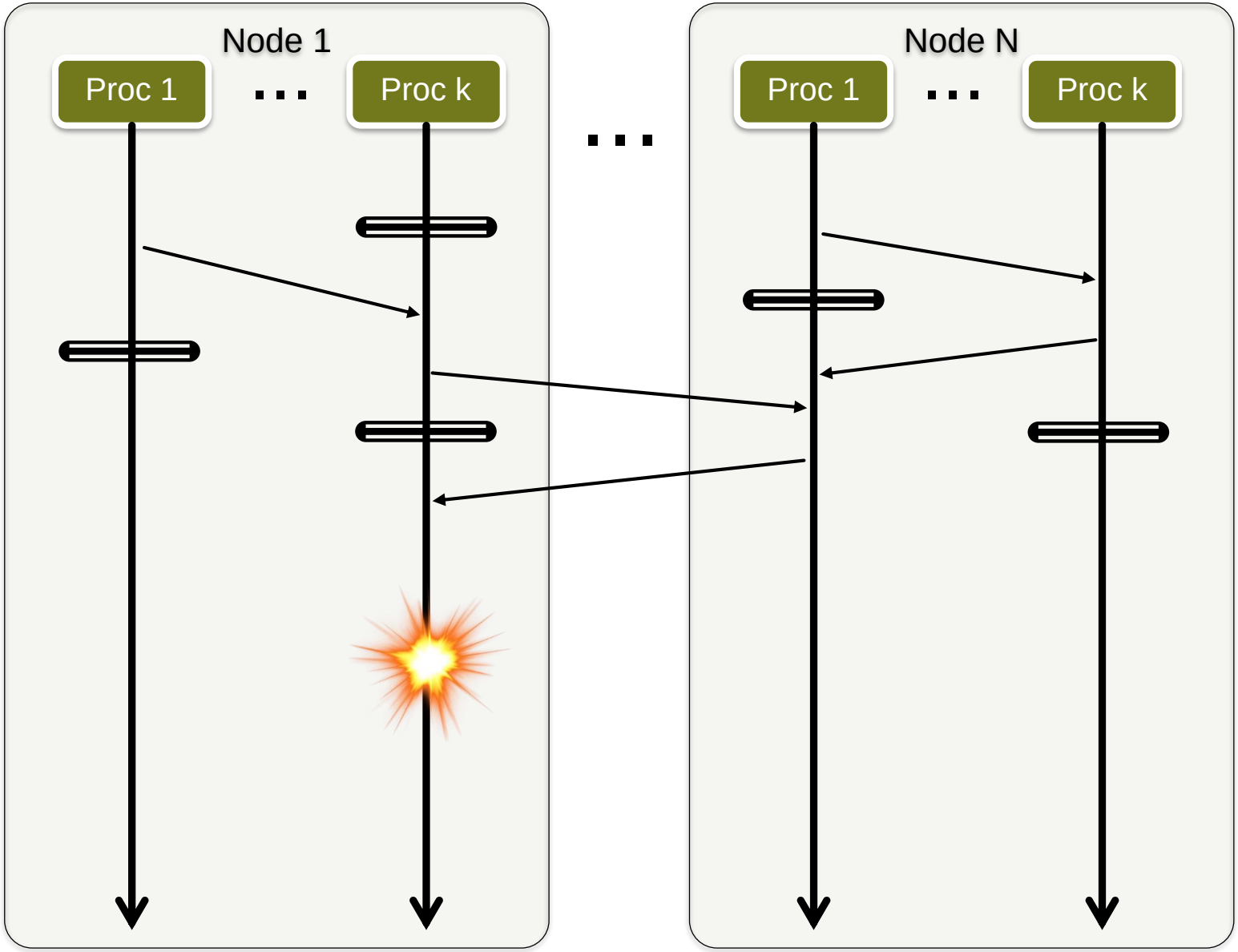

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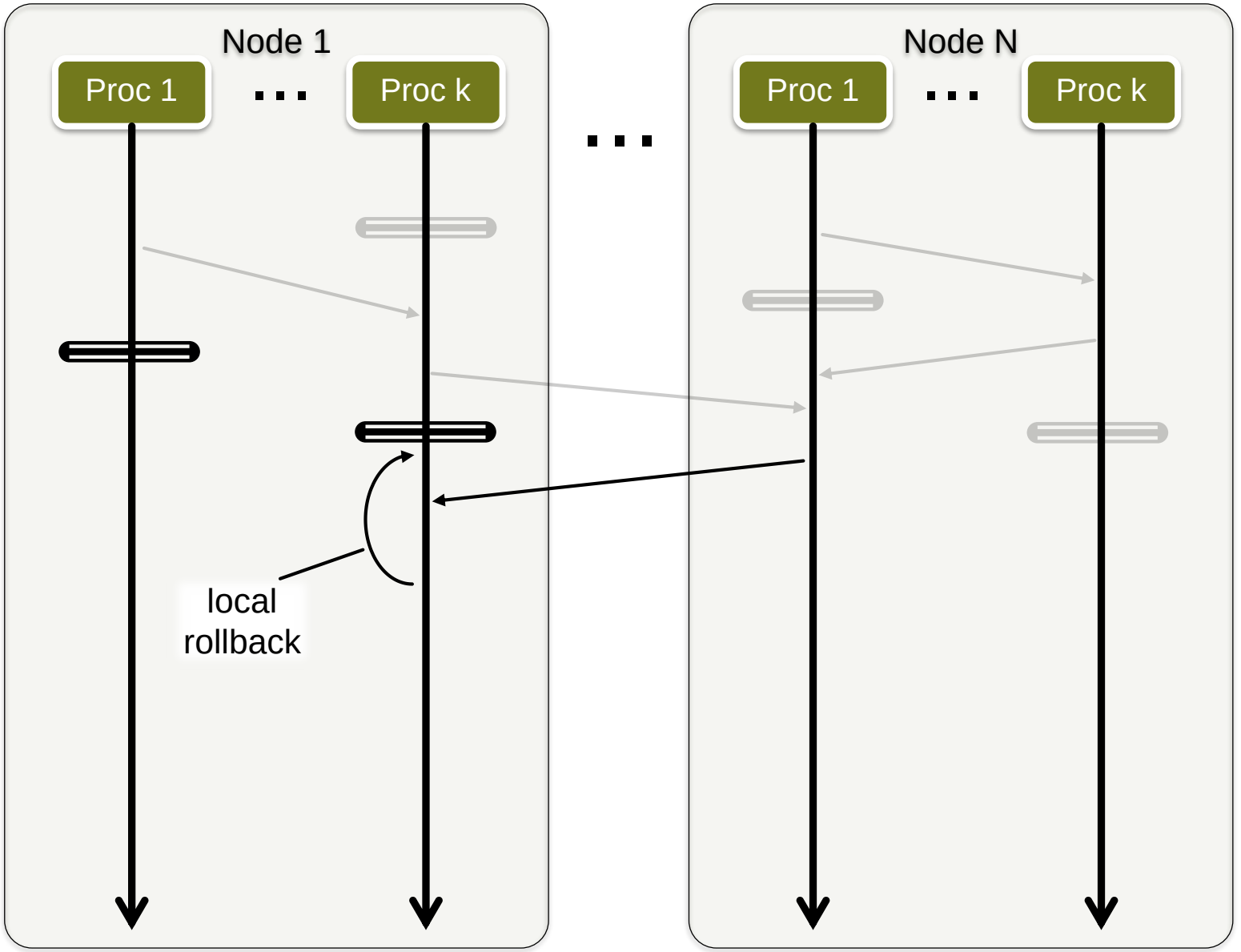

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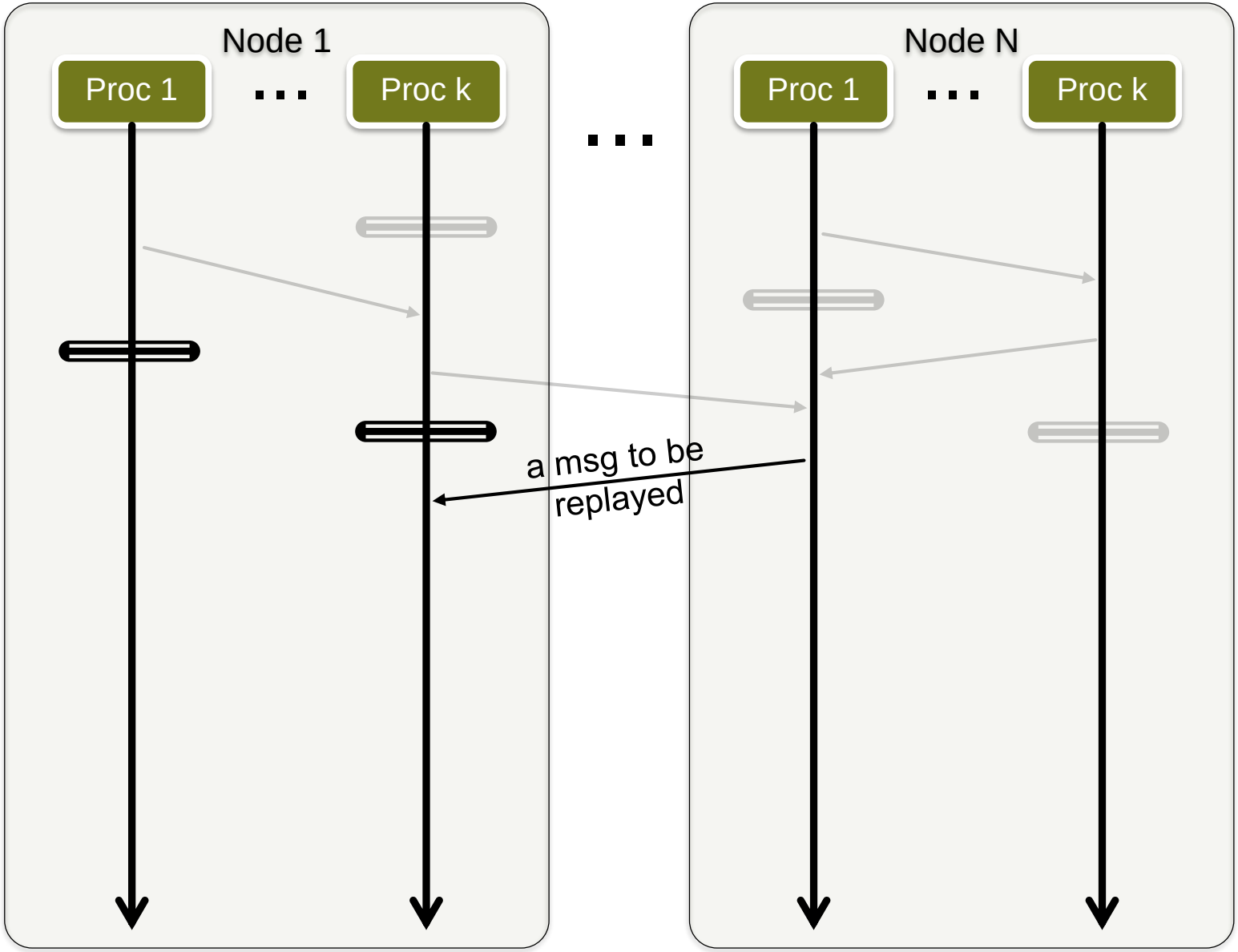

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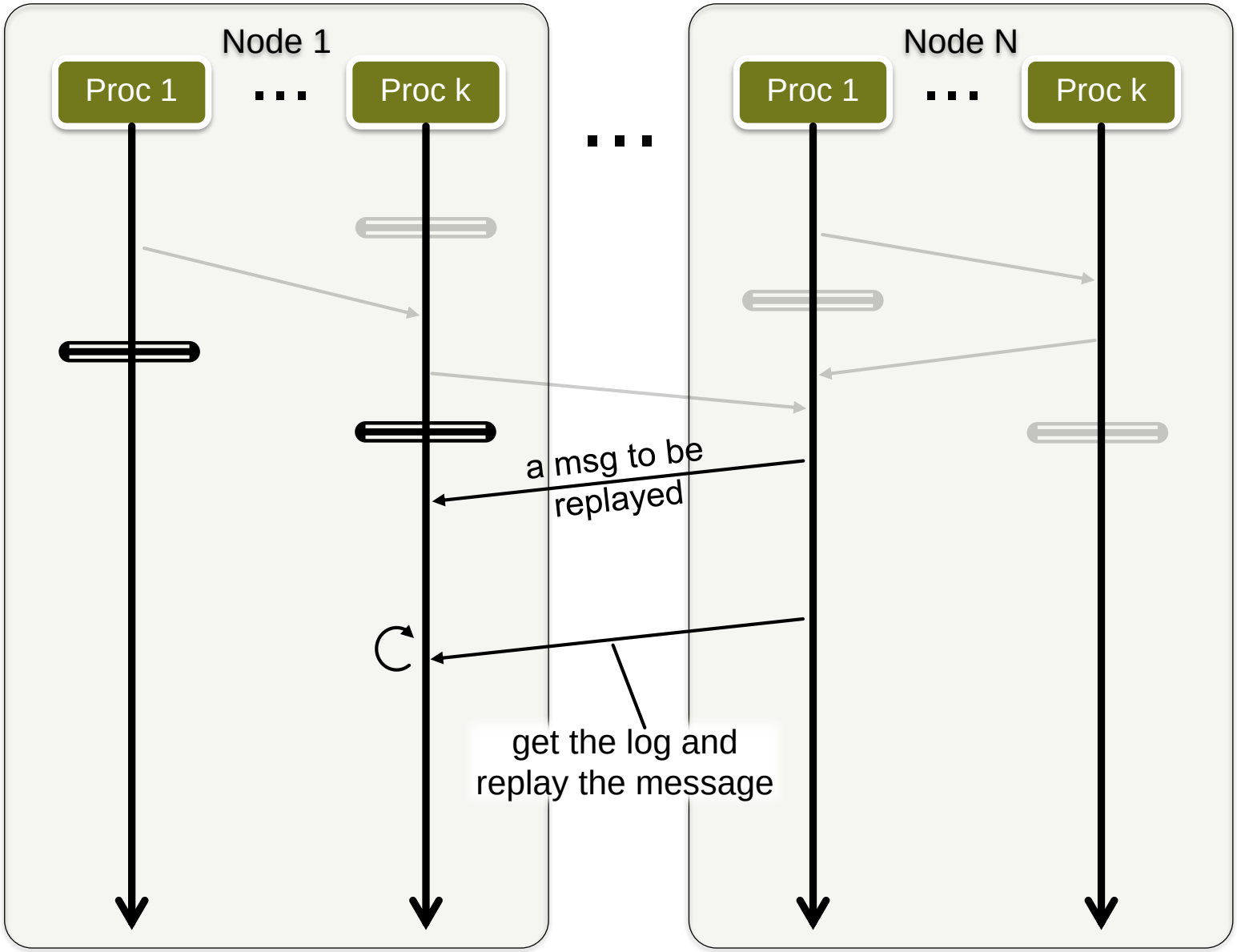

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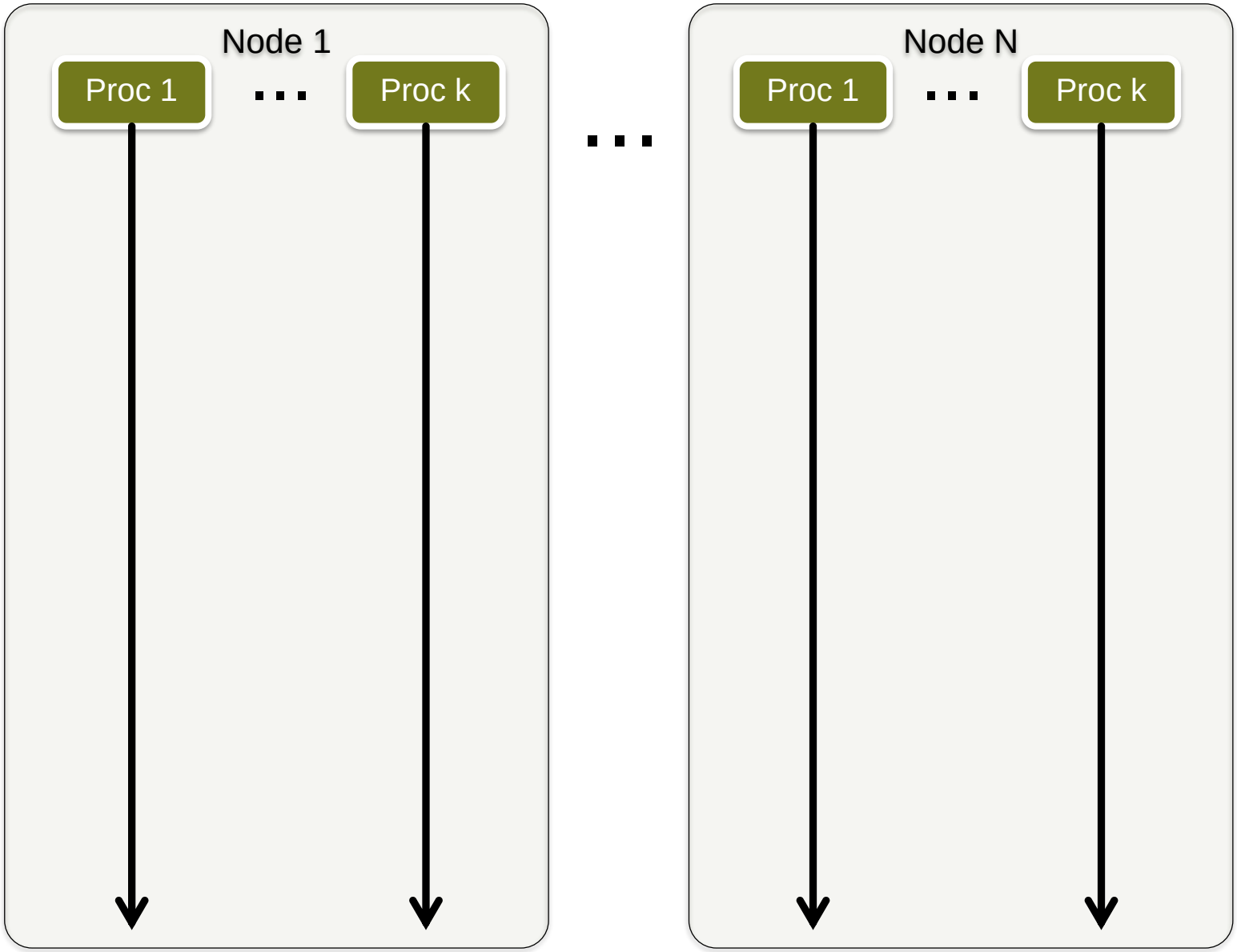

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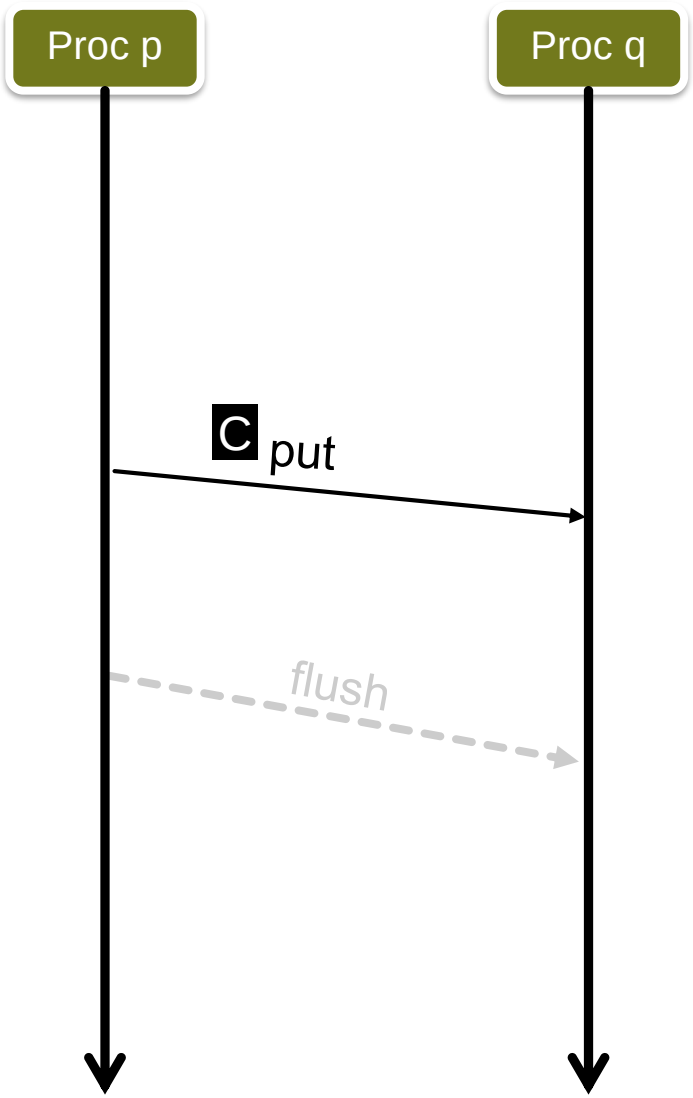

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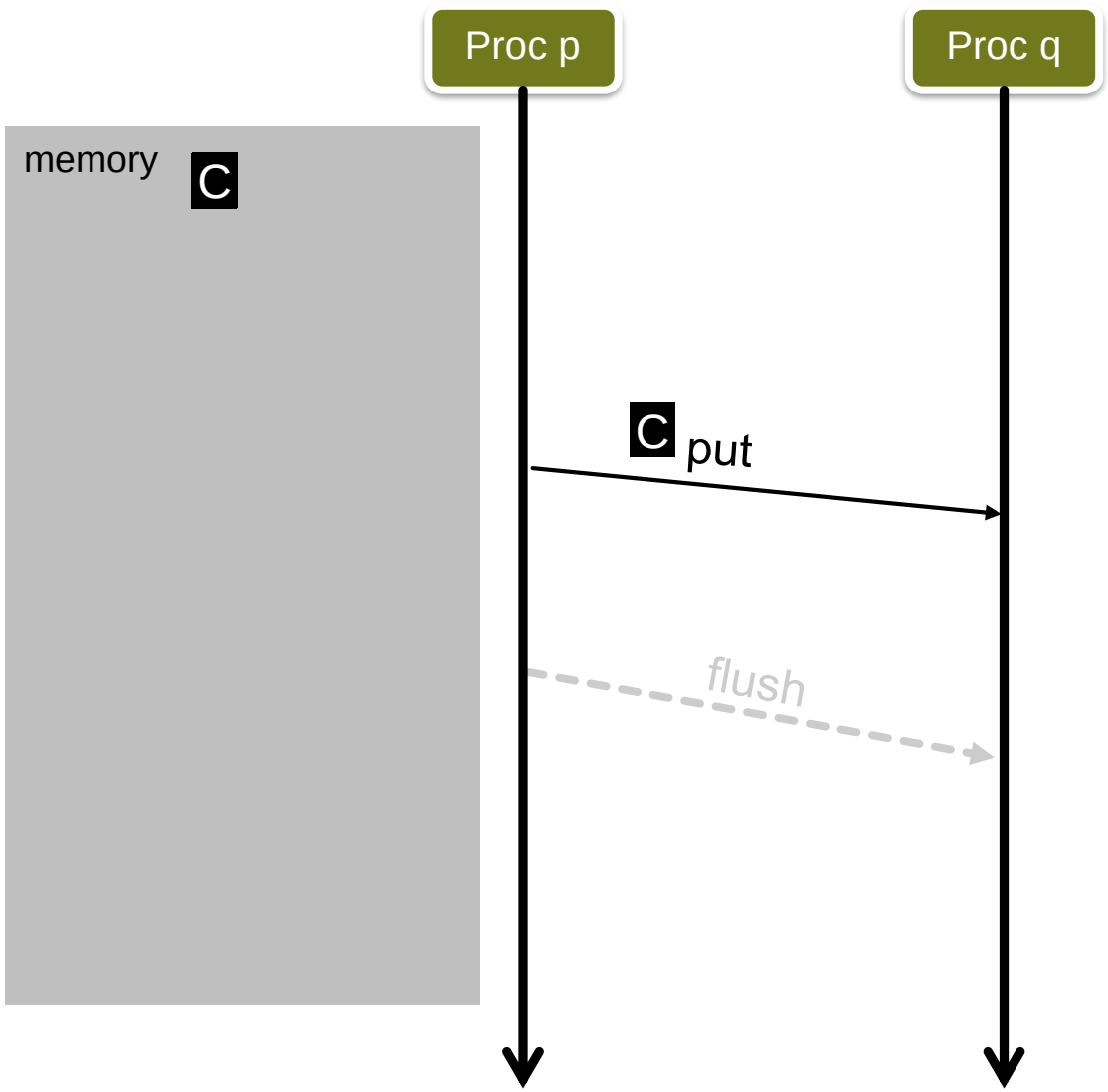

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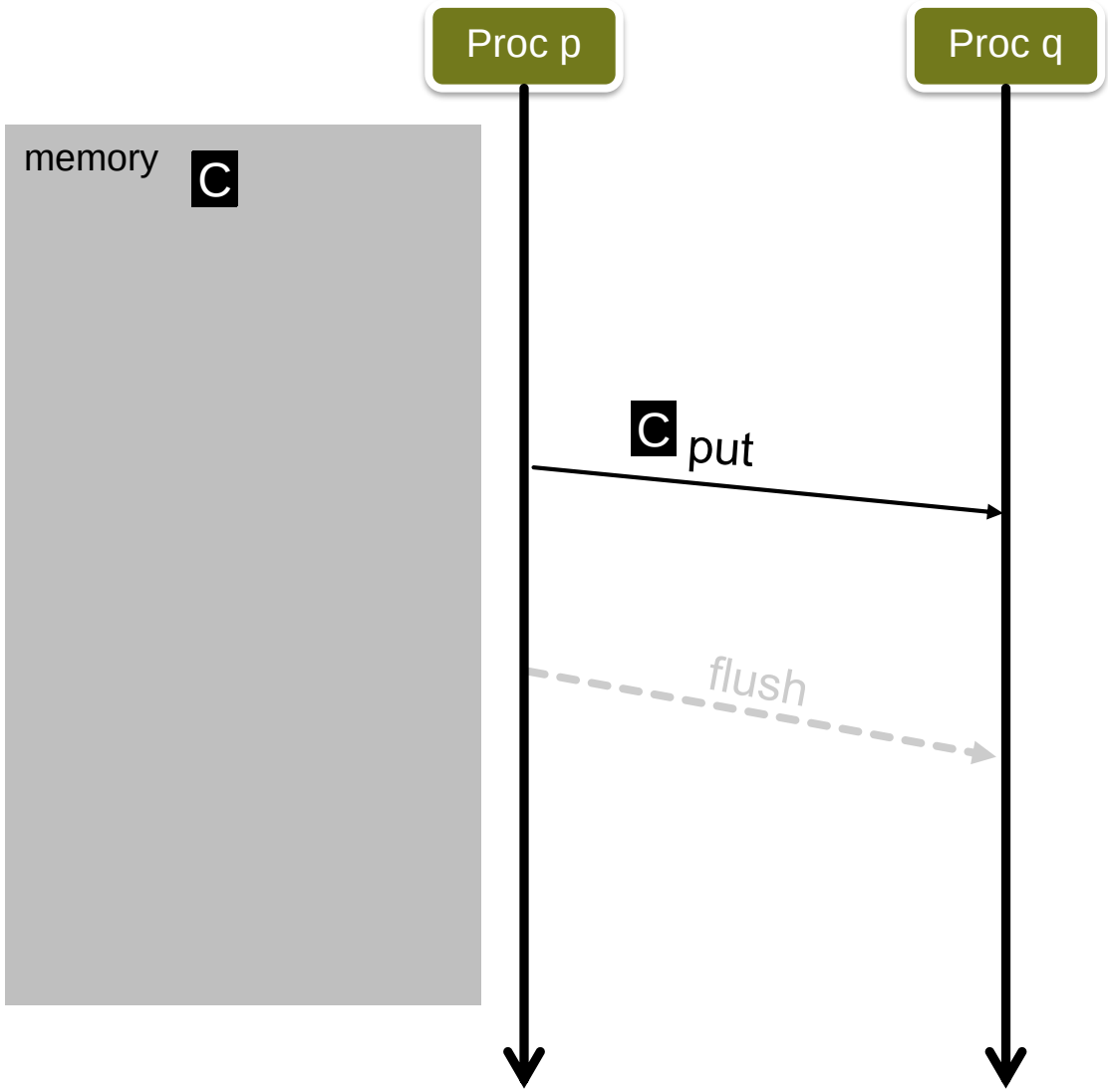

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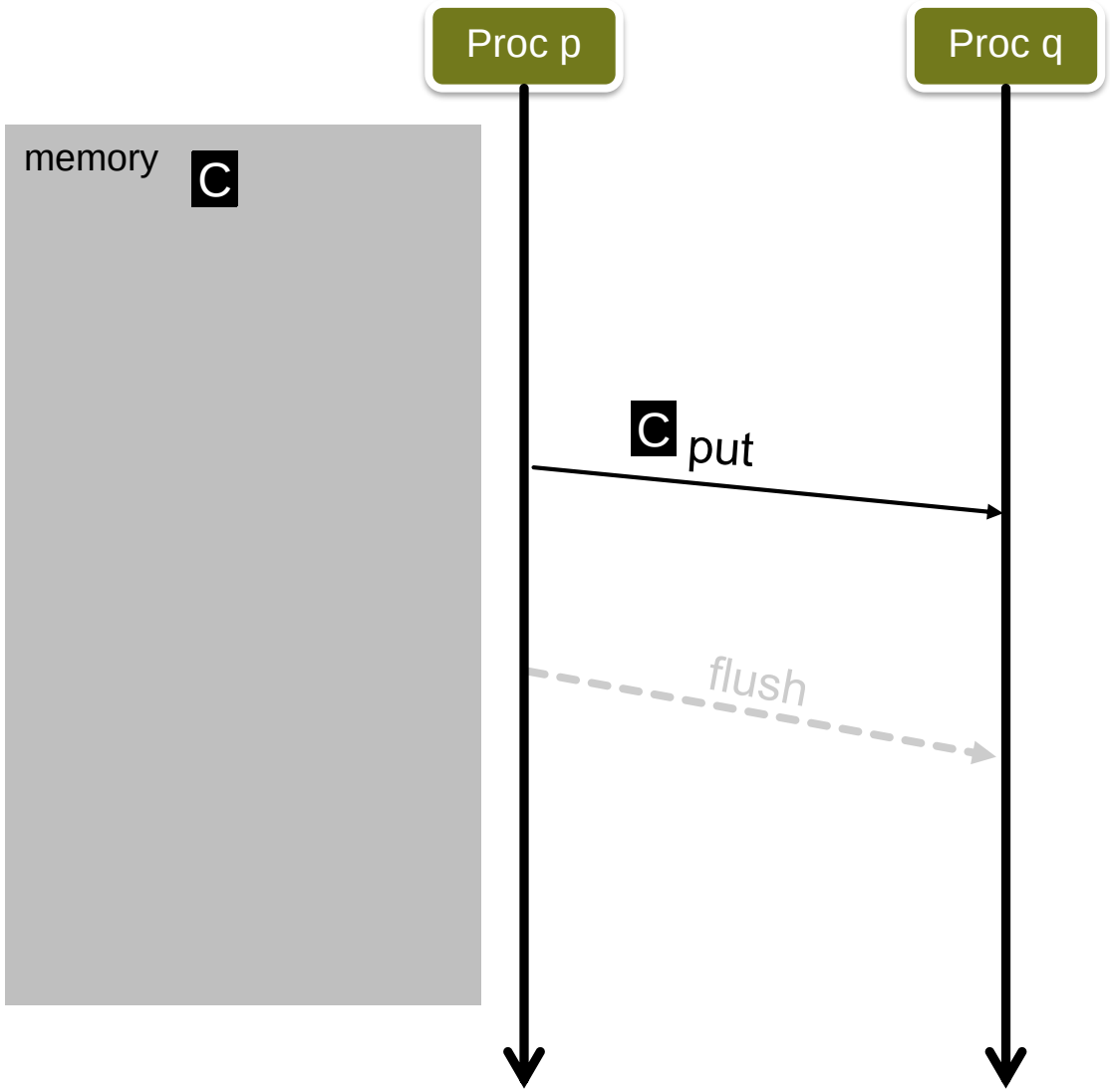

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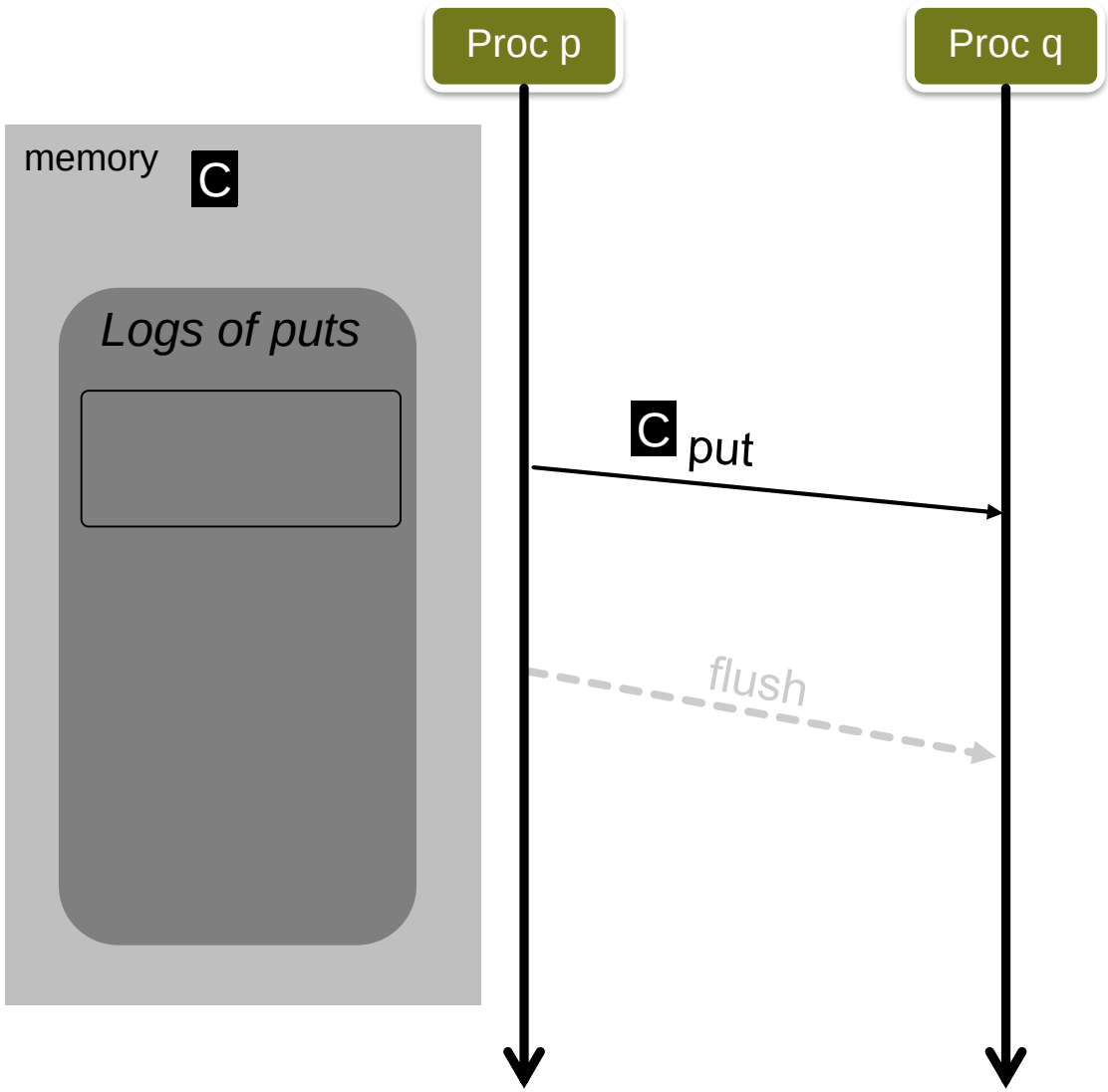

RMA: Logging Puts

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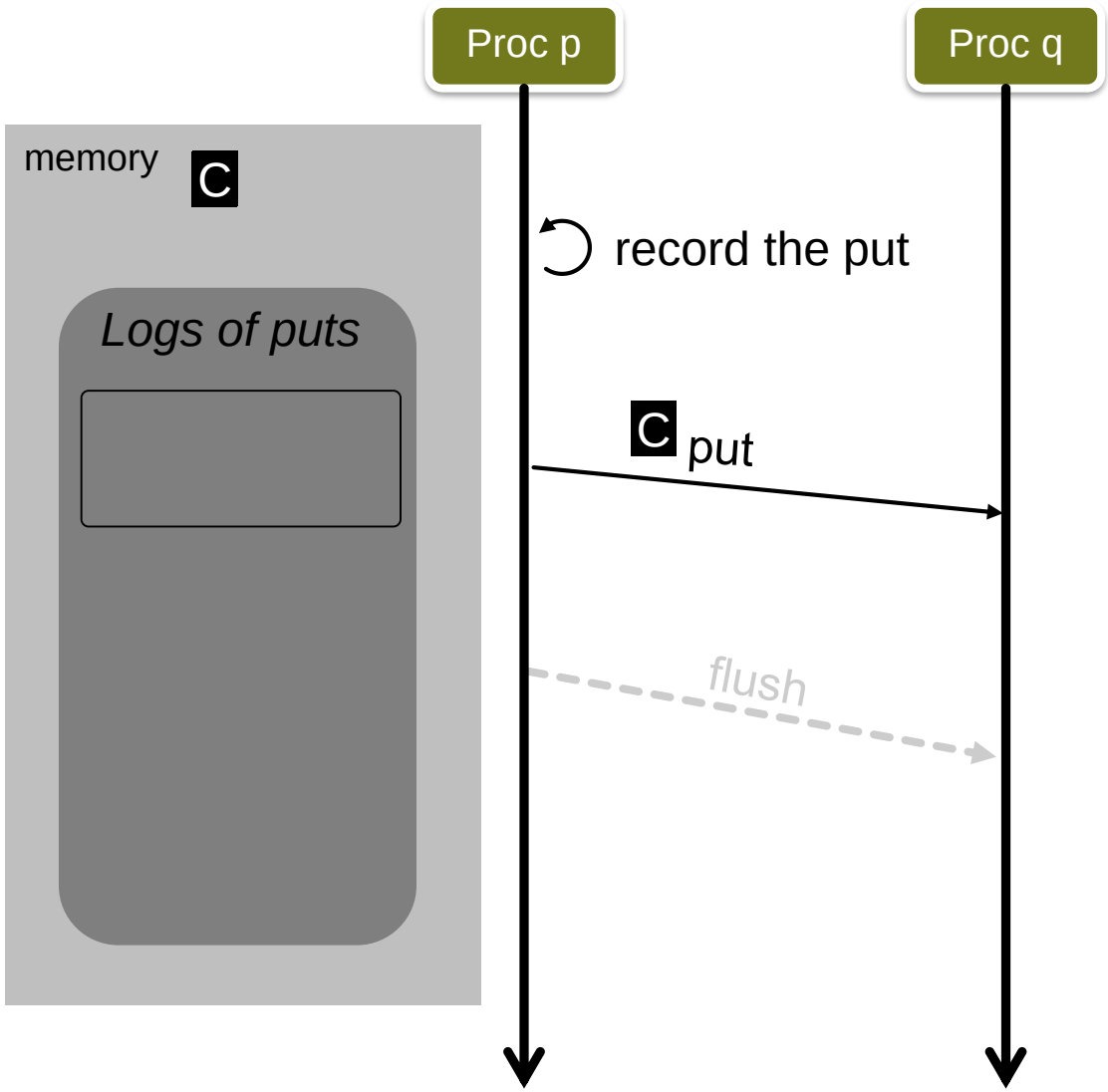

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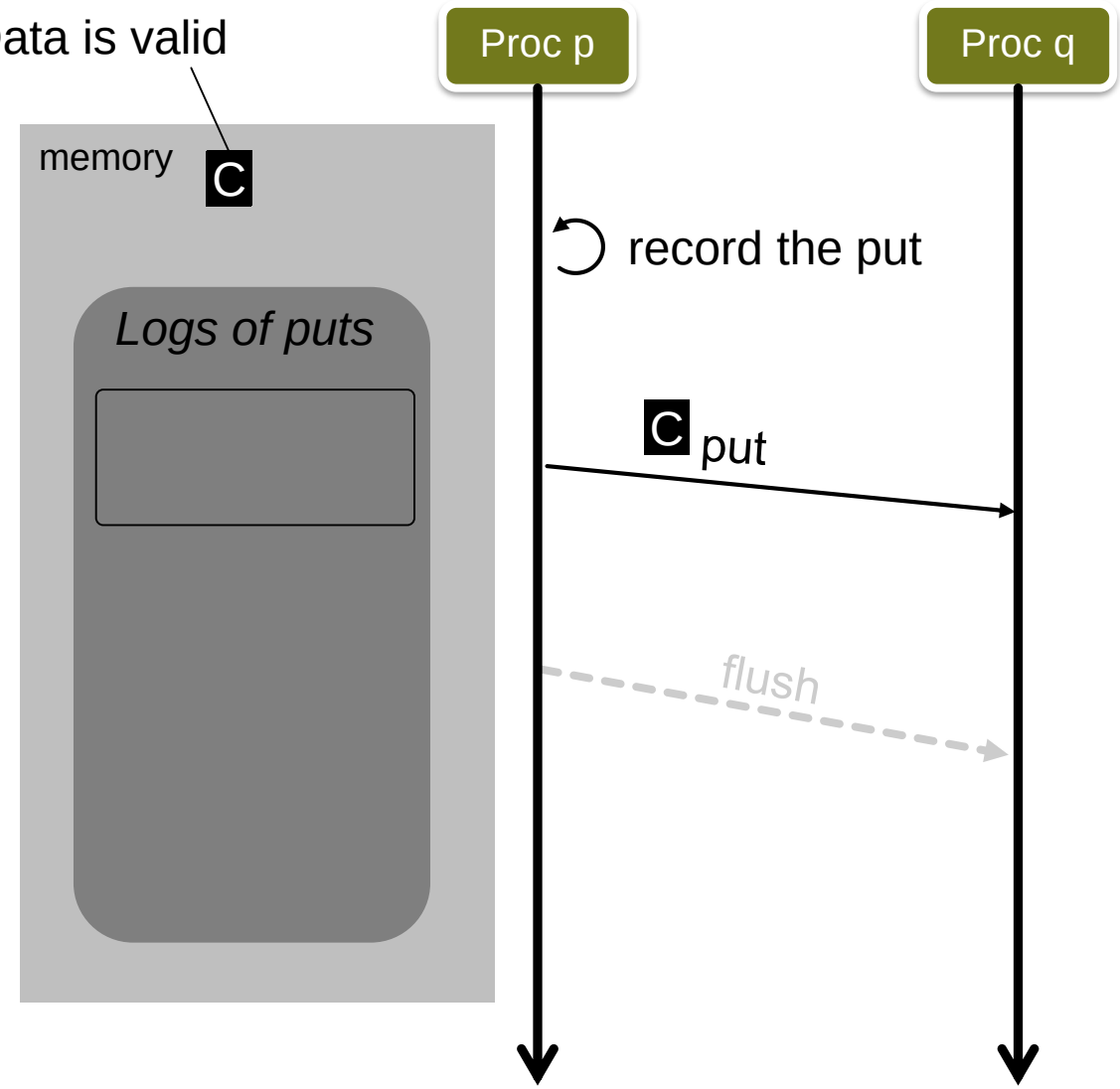

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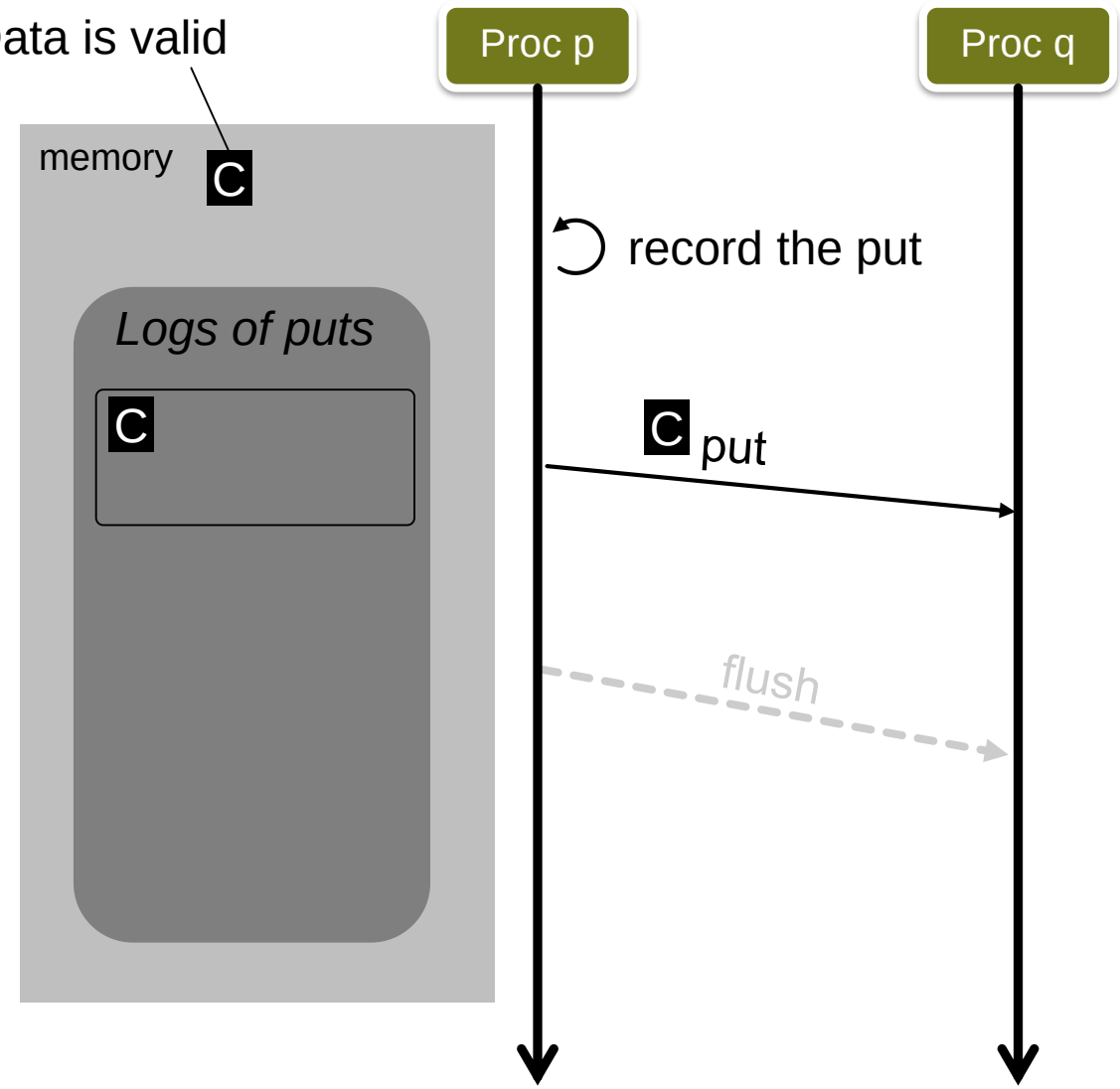

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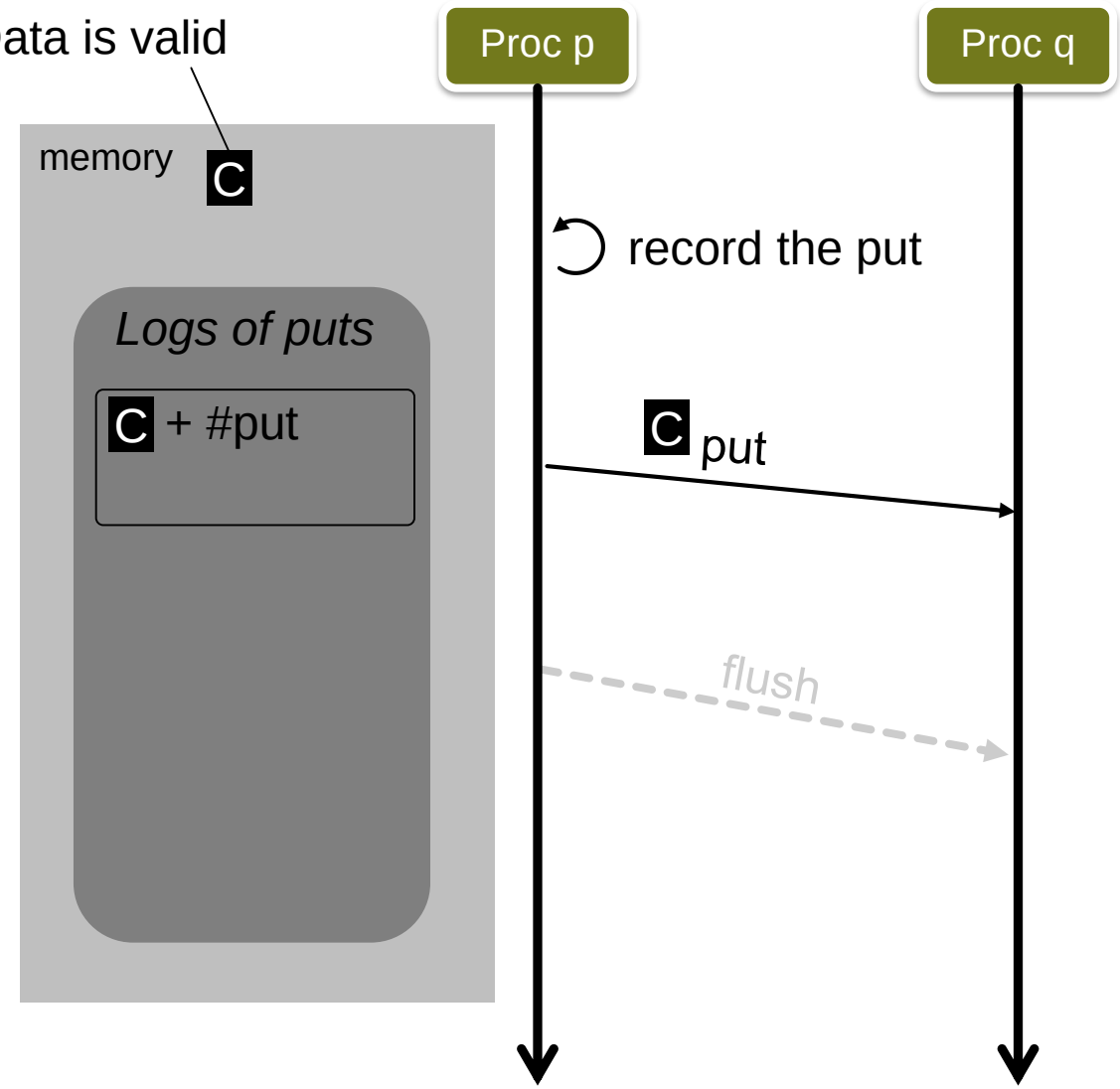

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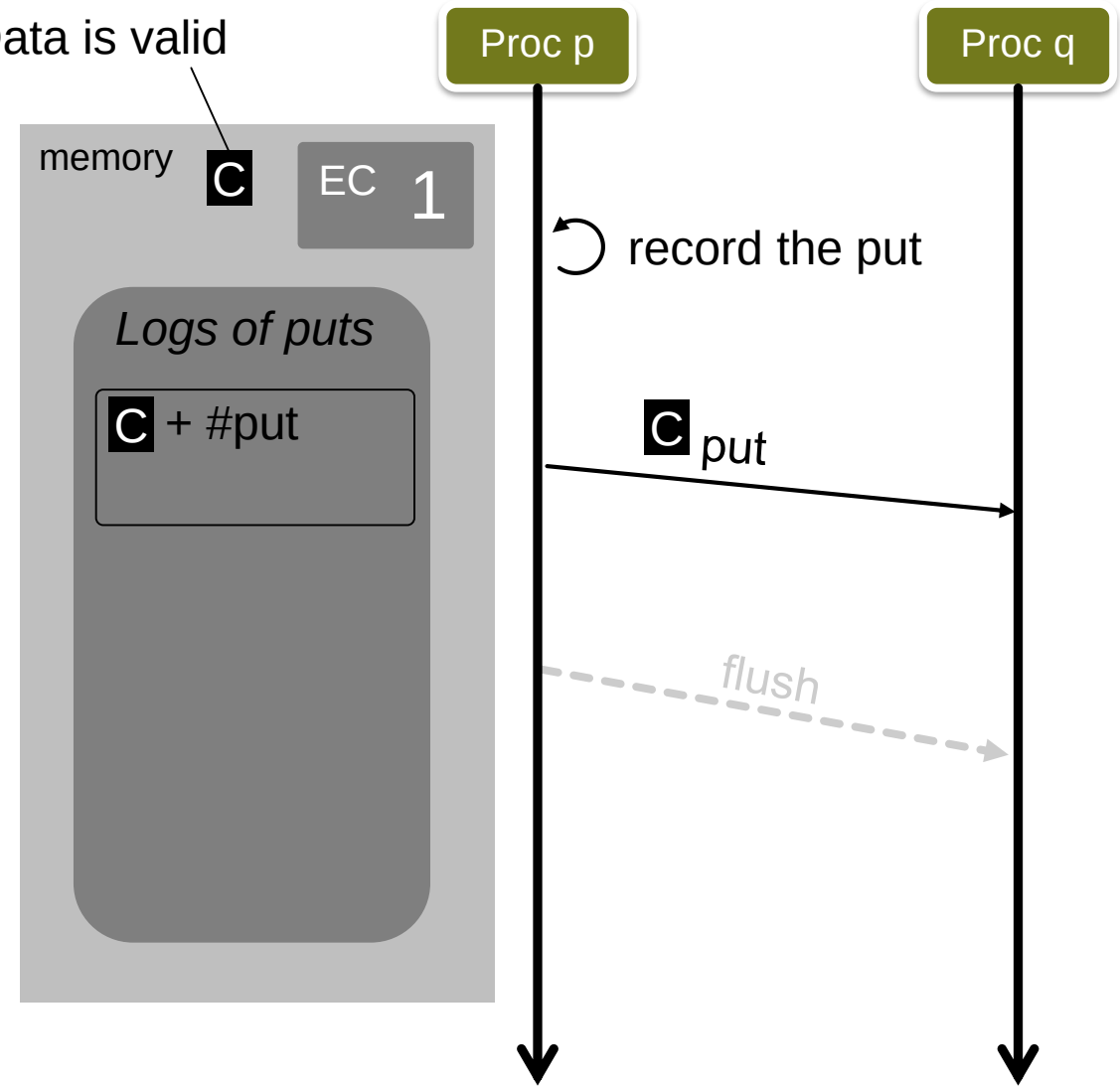

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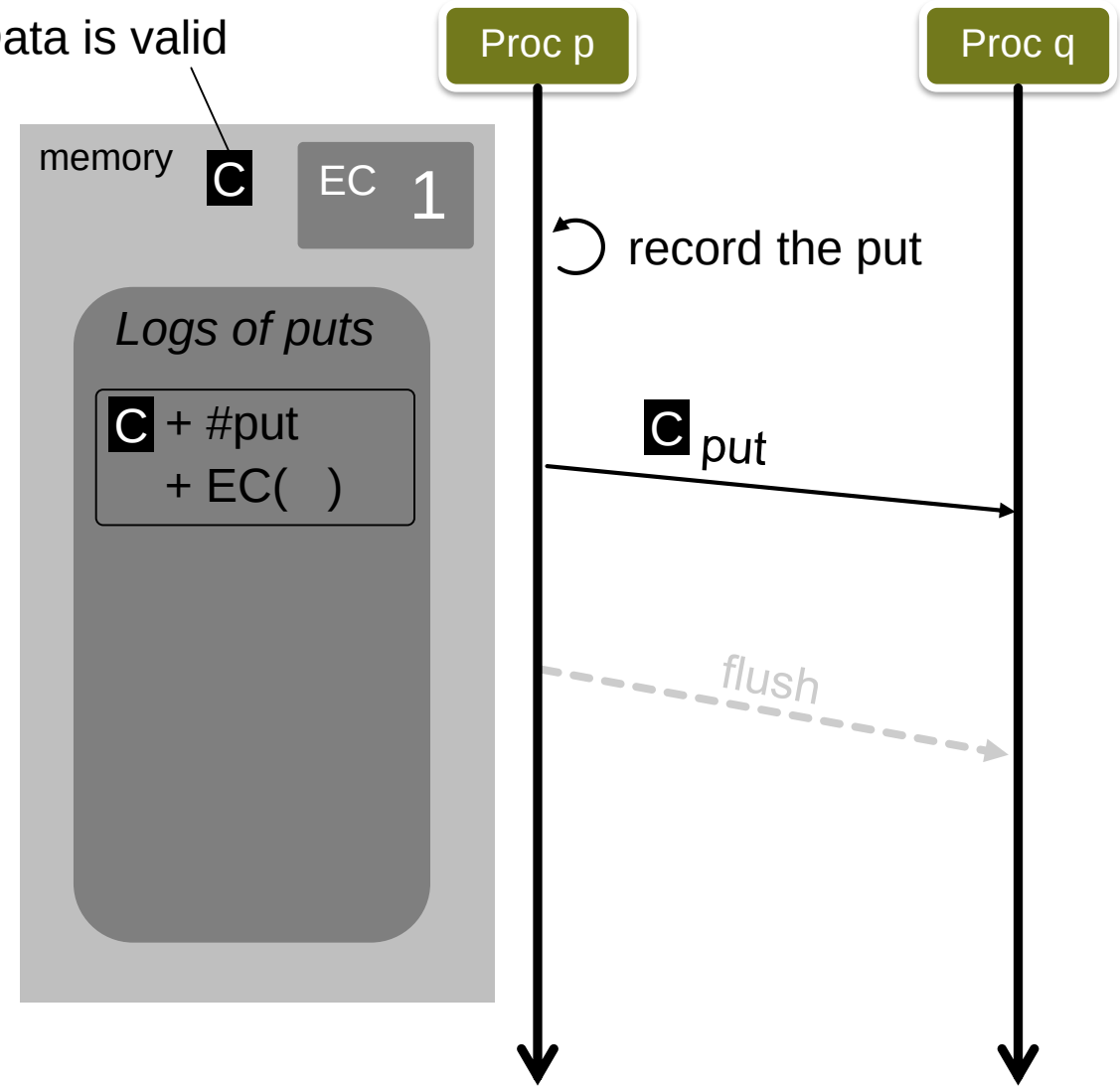

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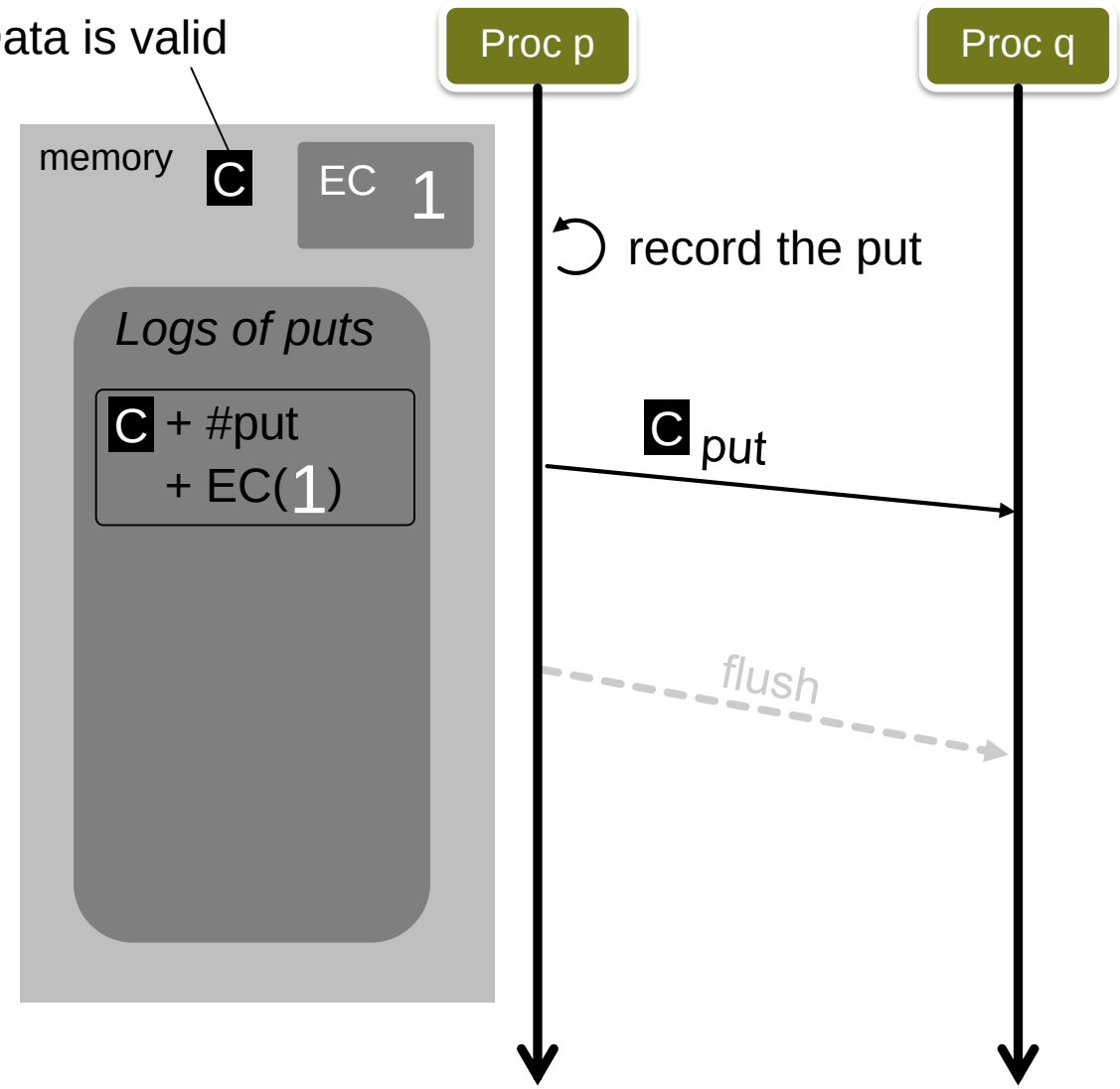

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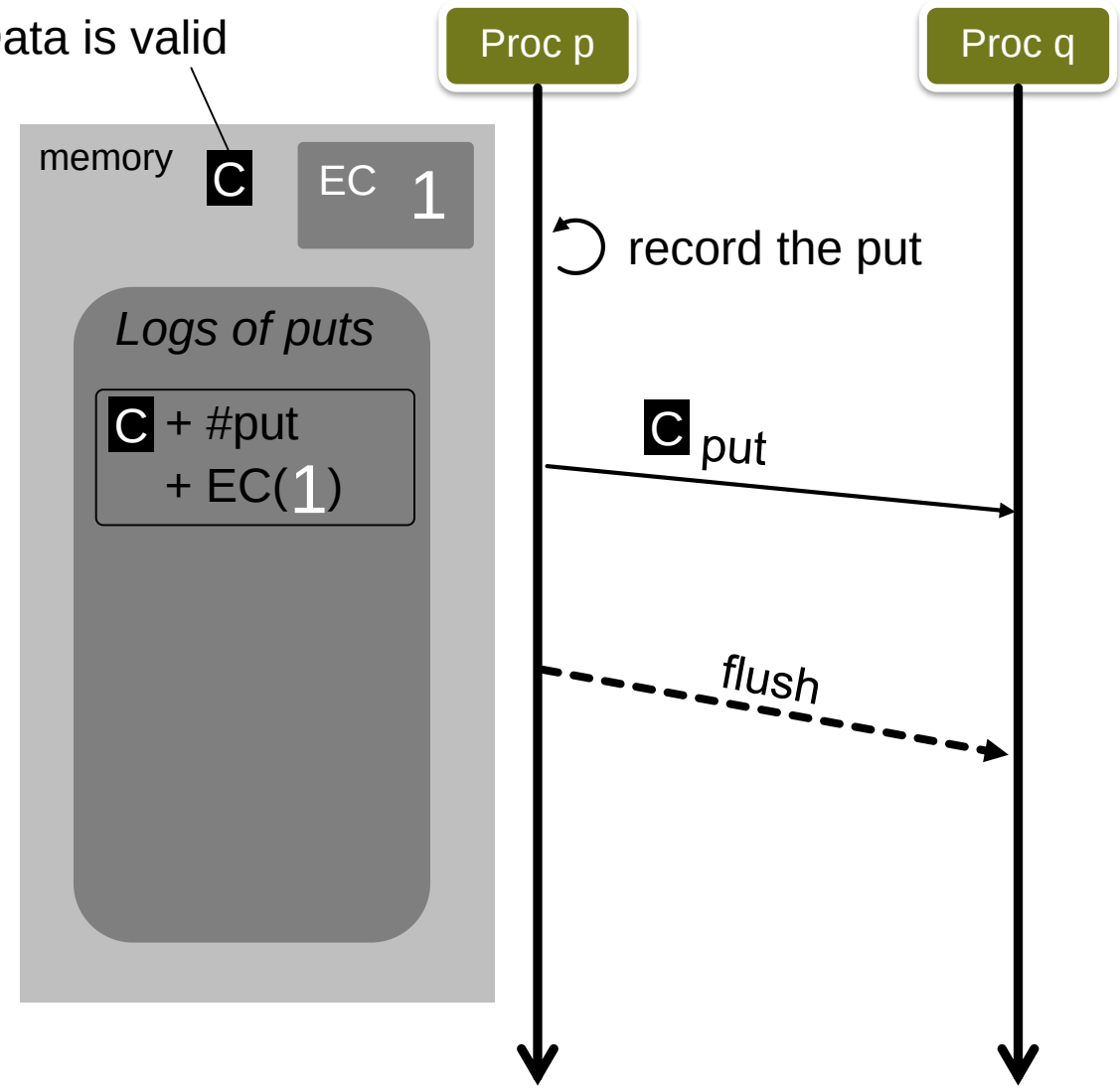

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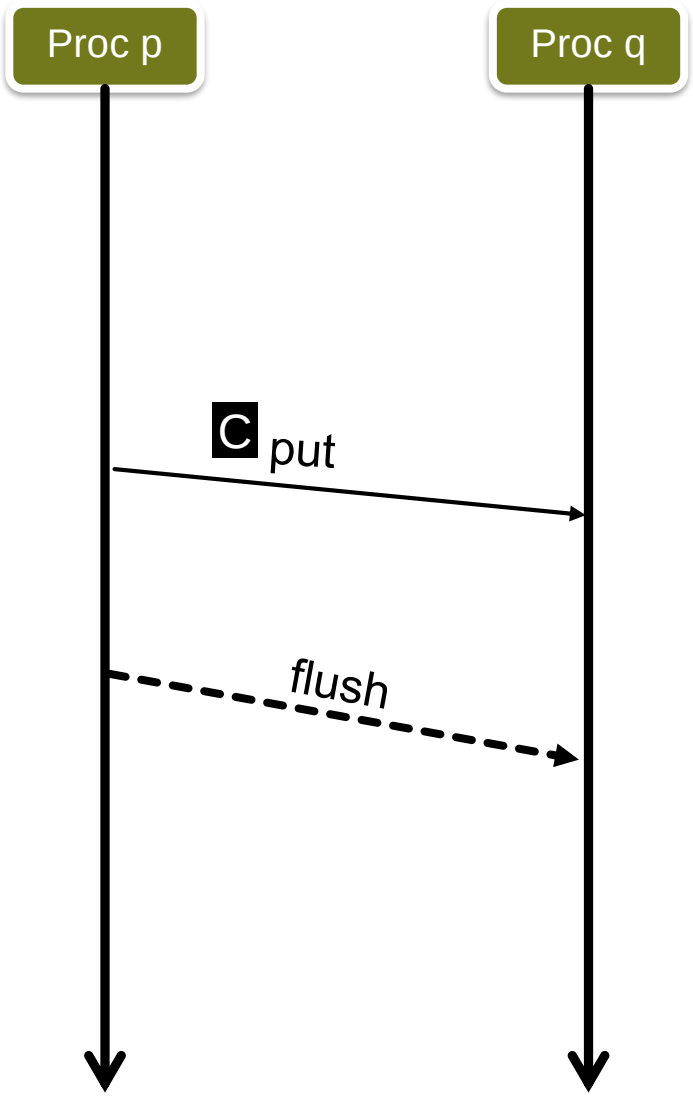

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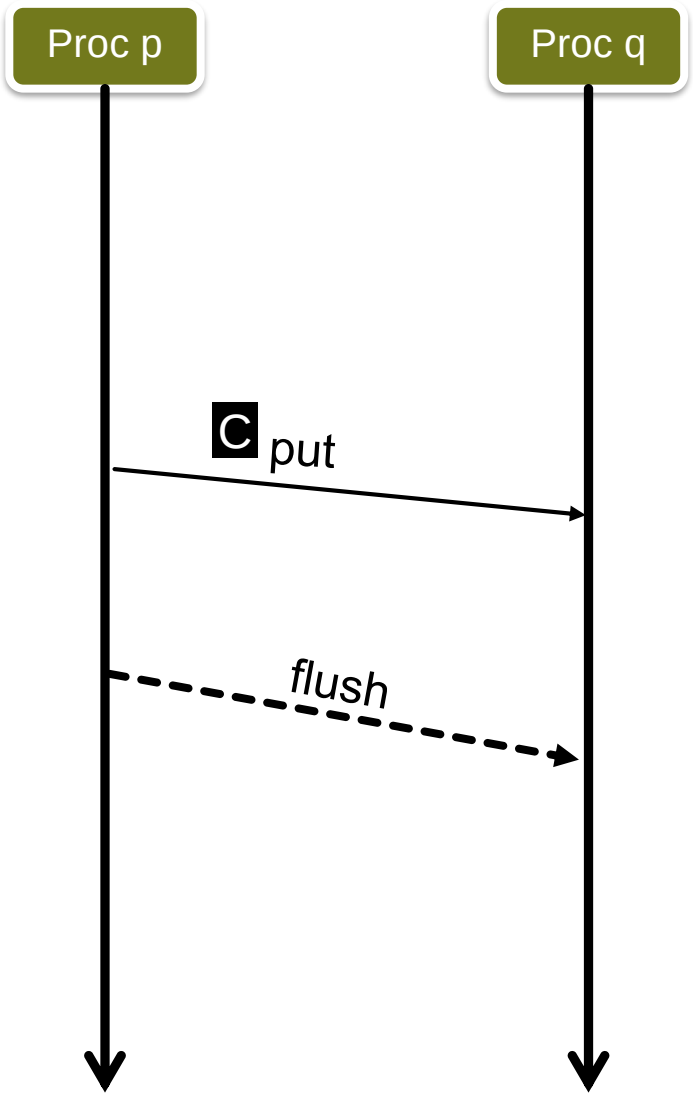

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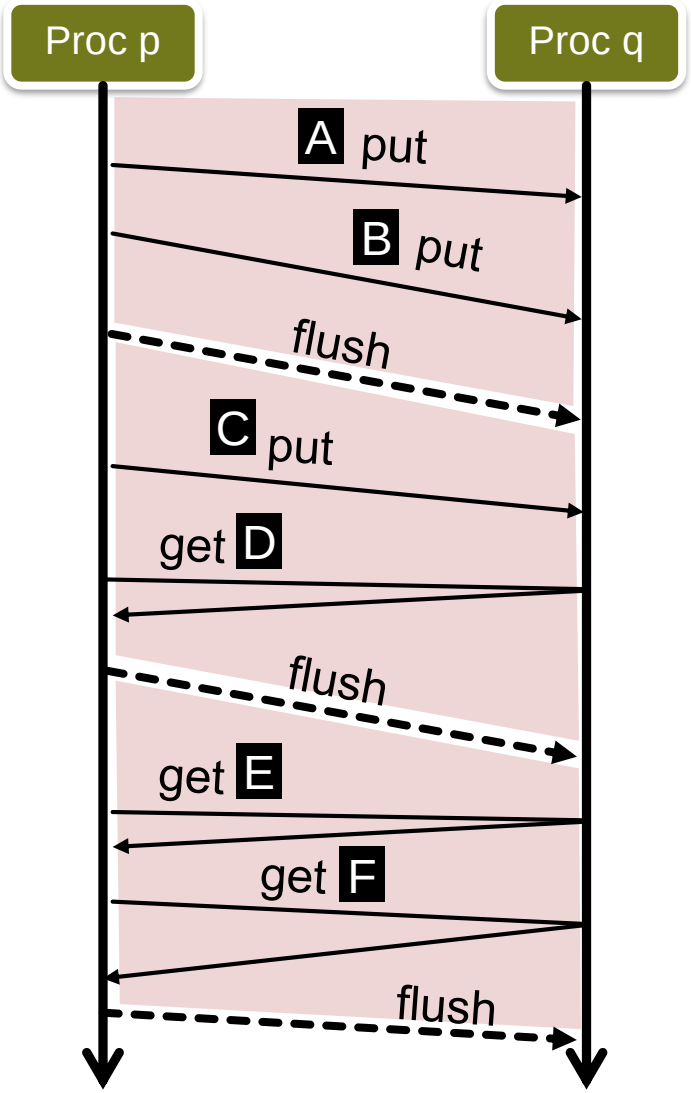

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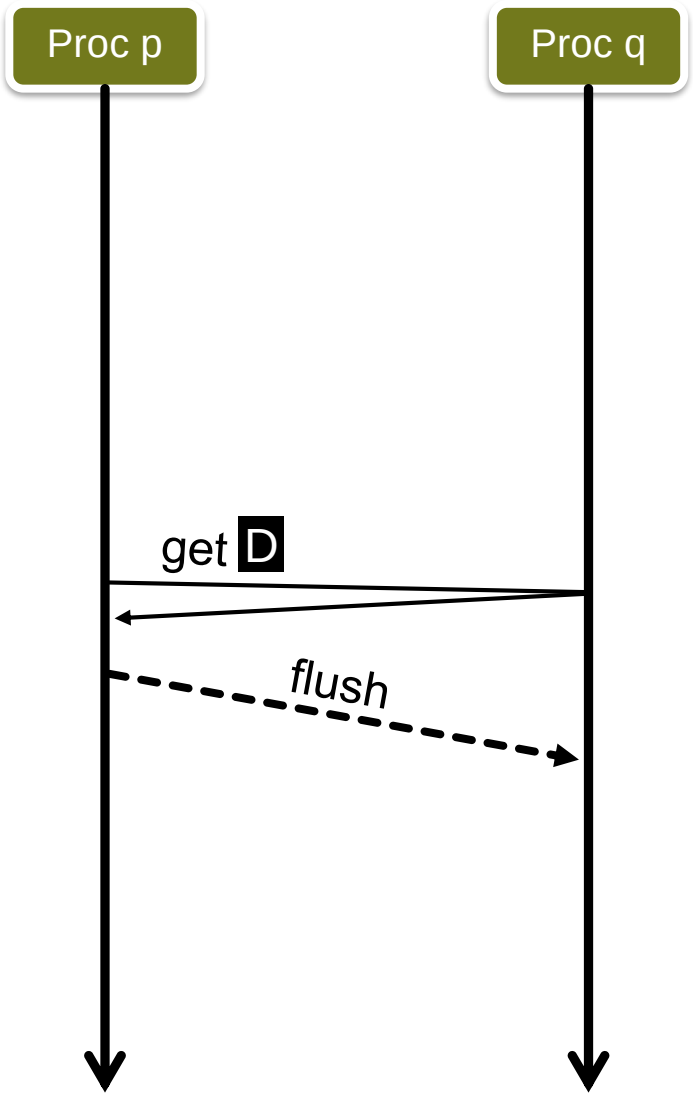

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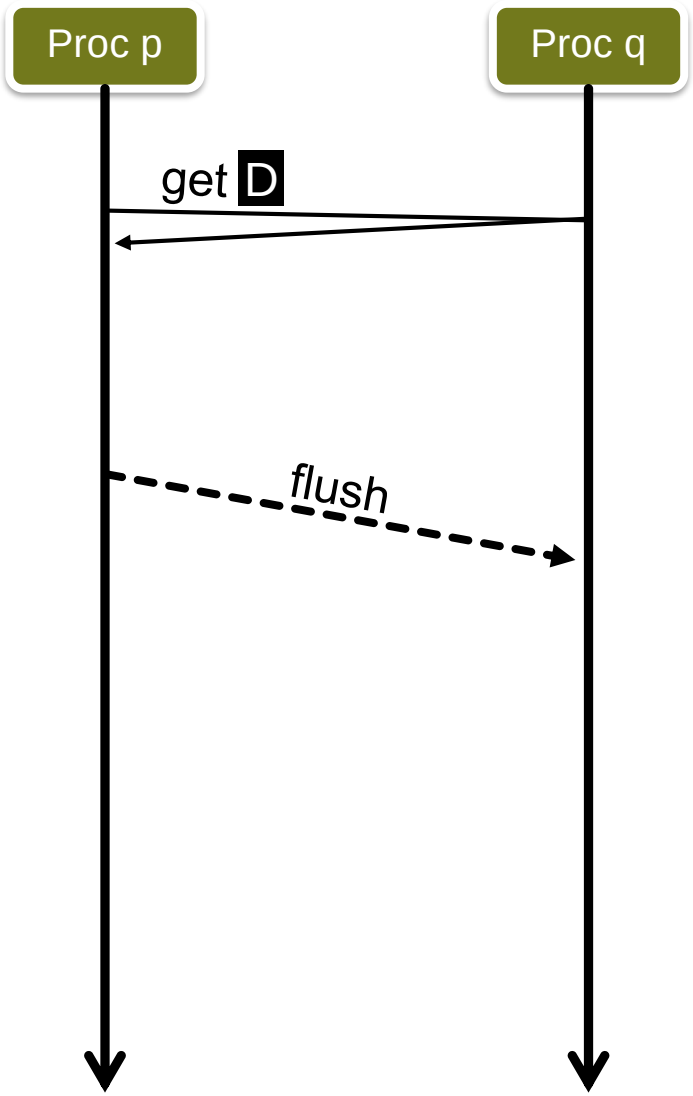

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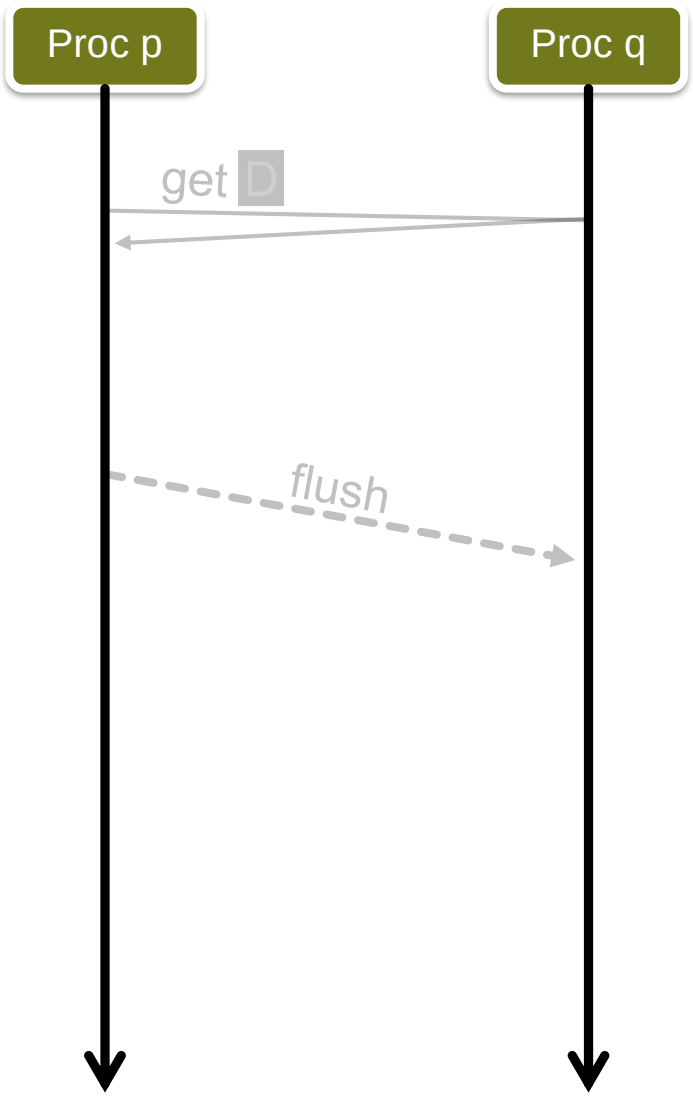

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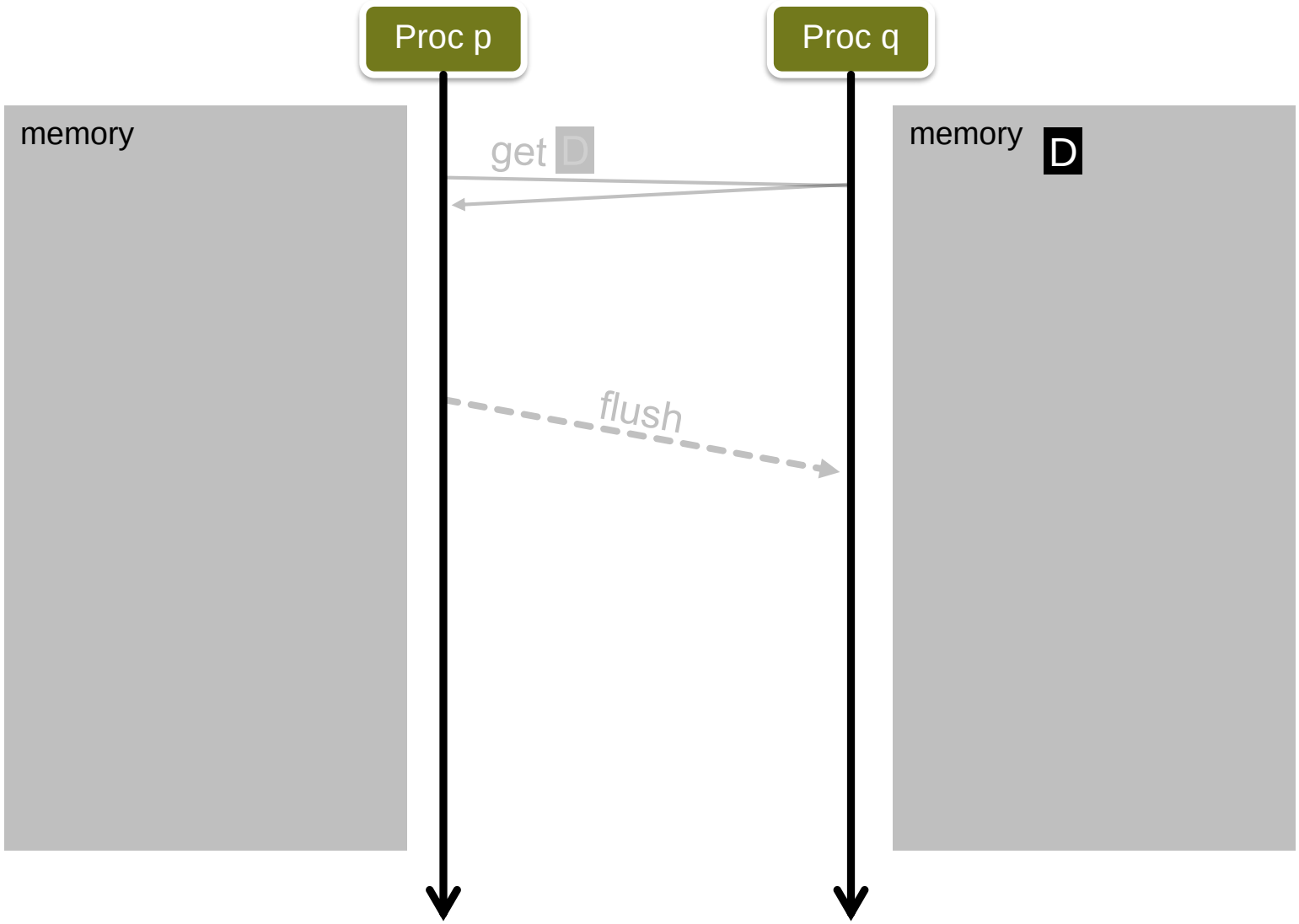

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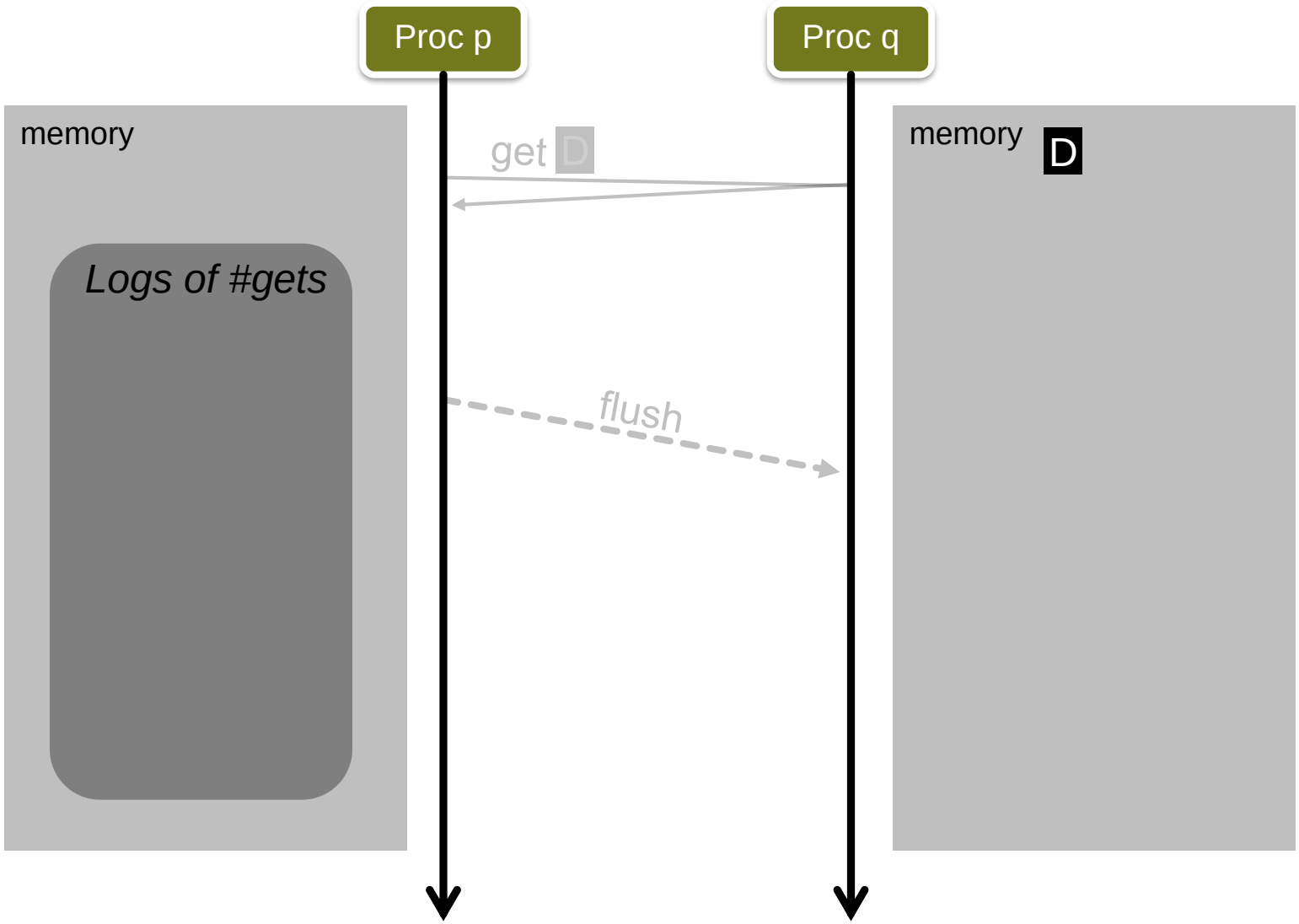

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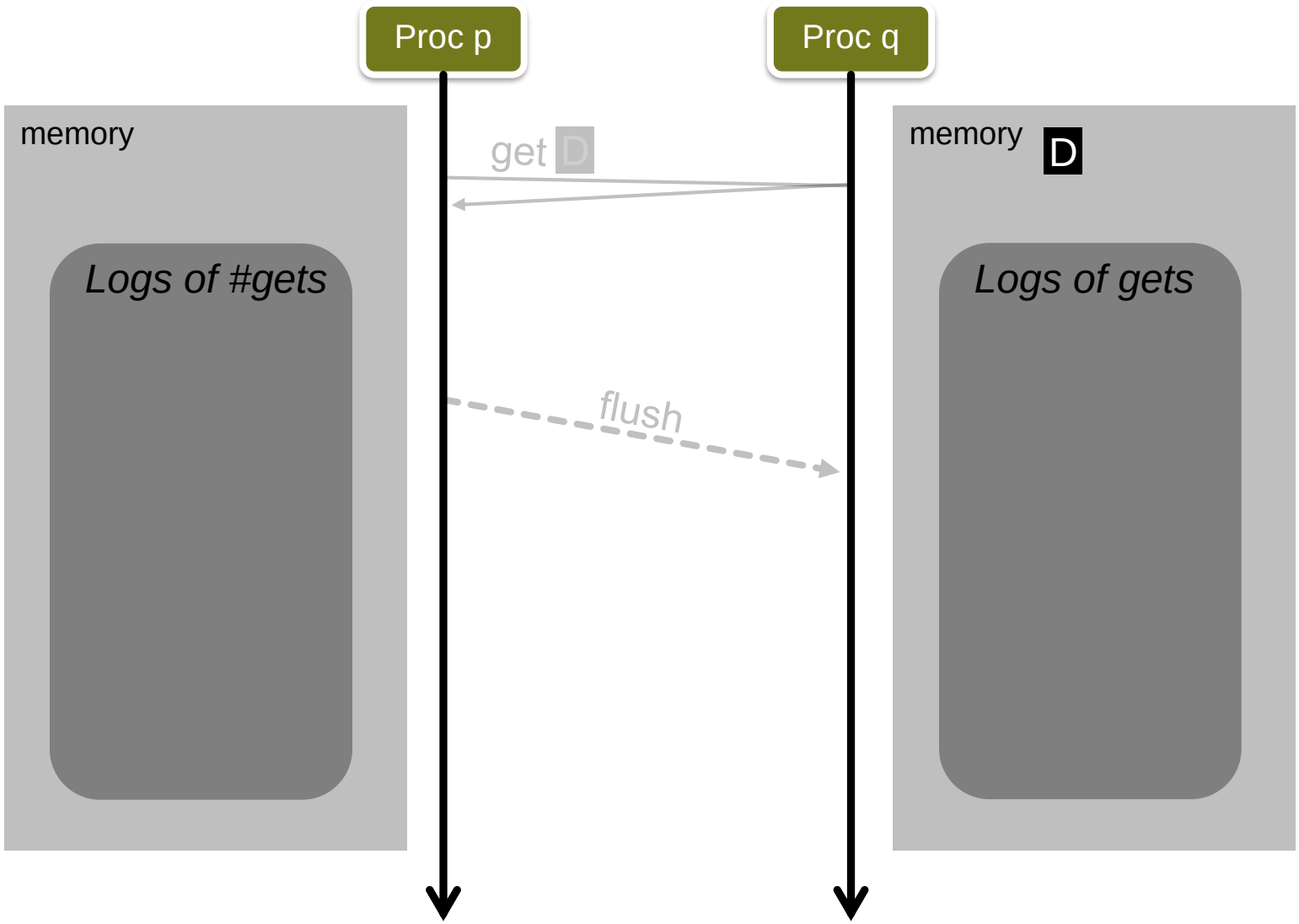

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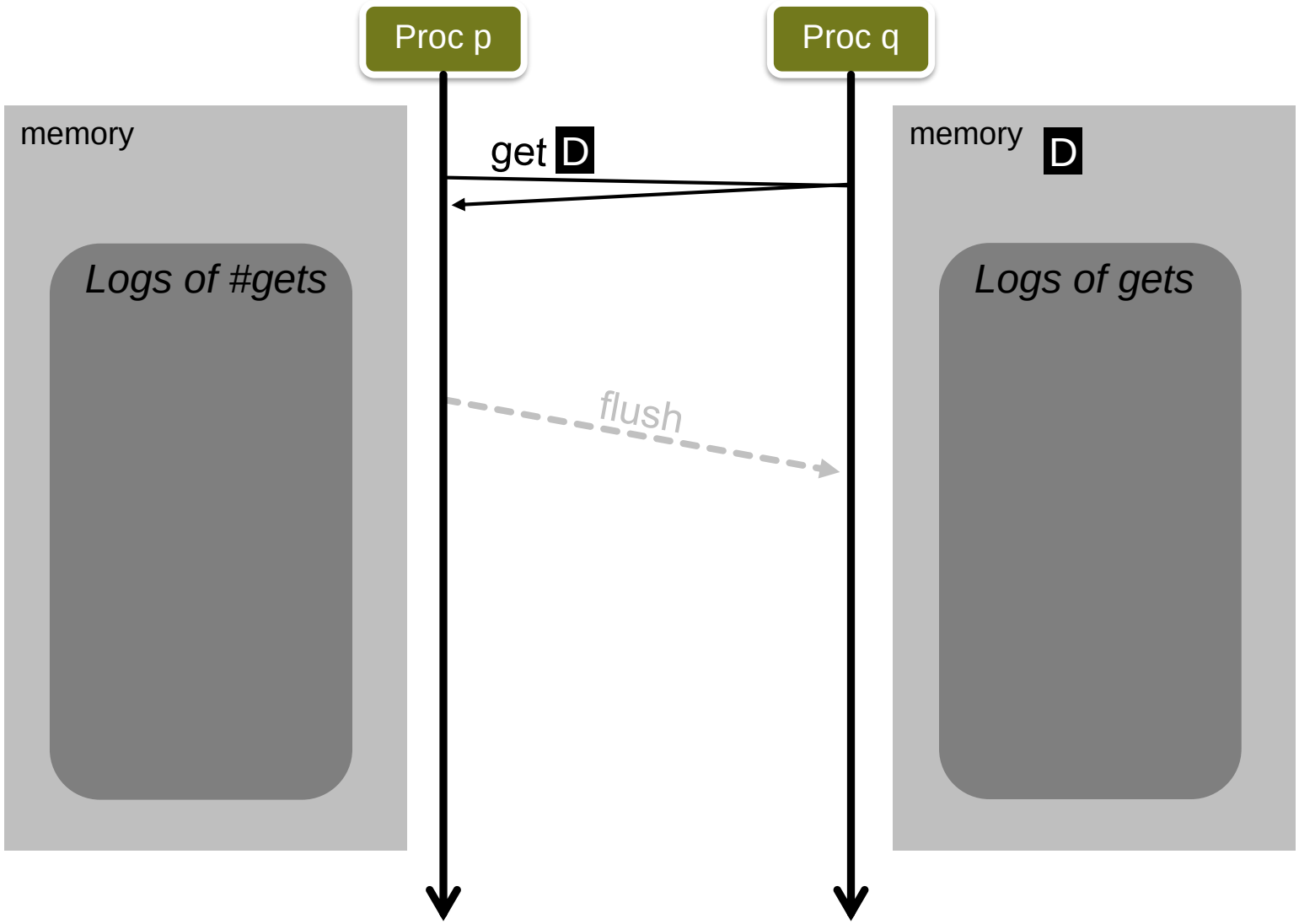

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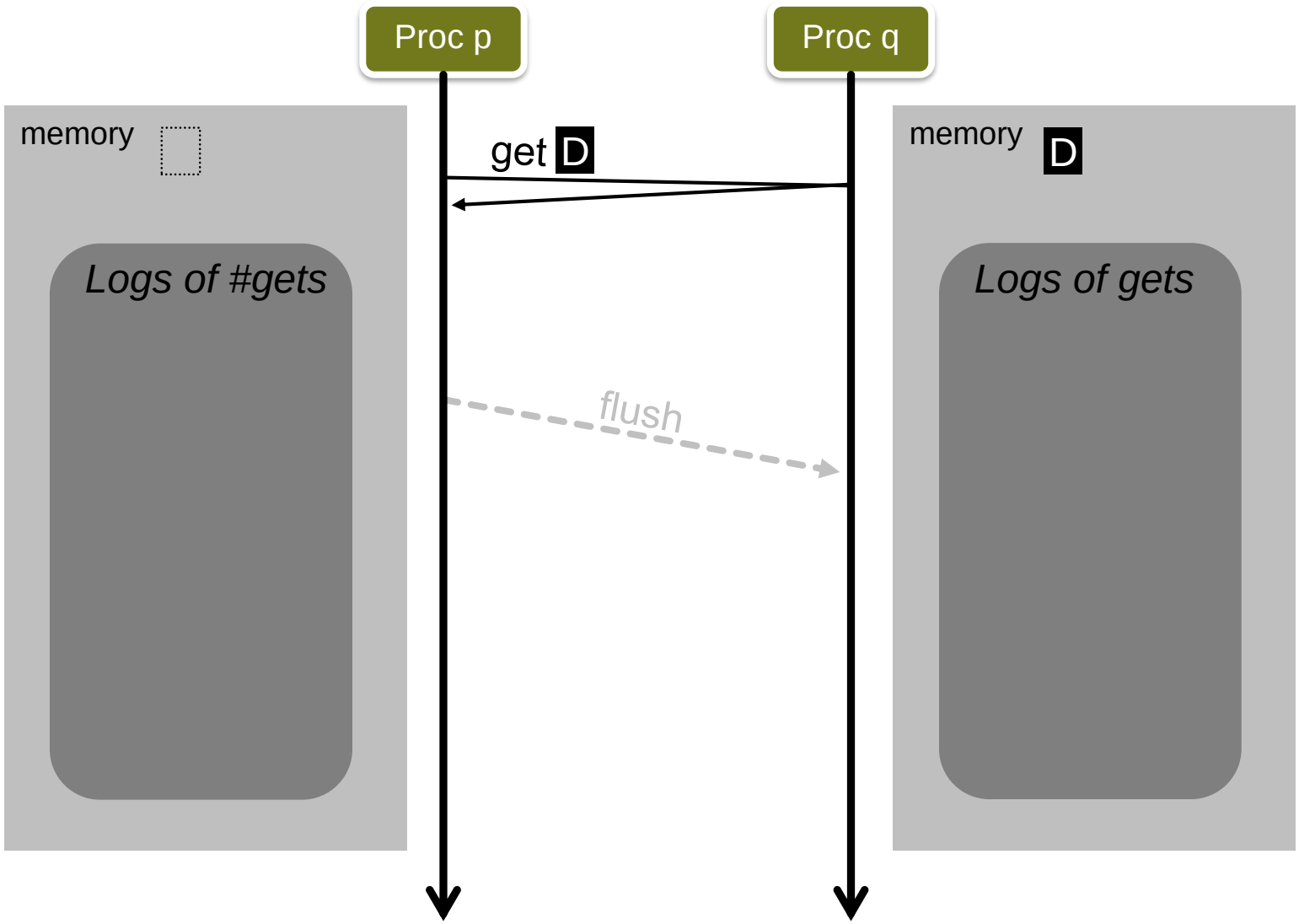

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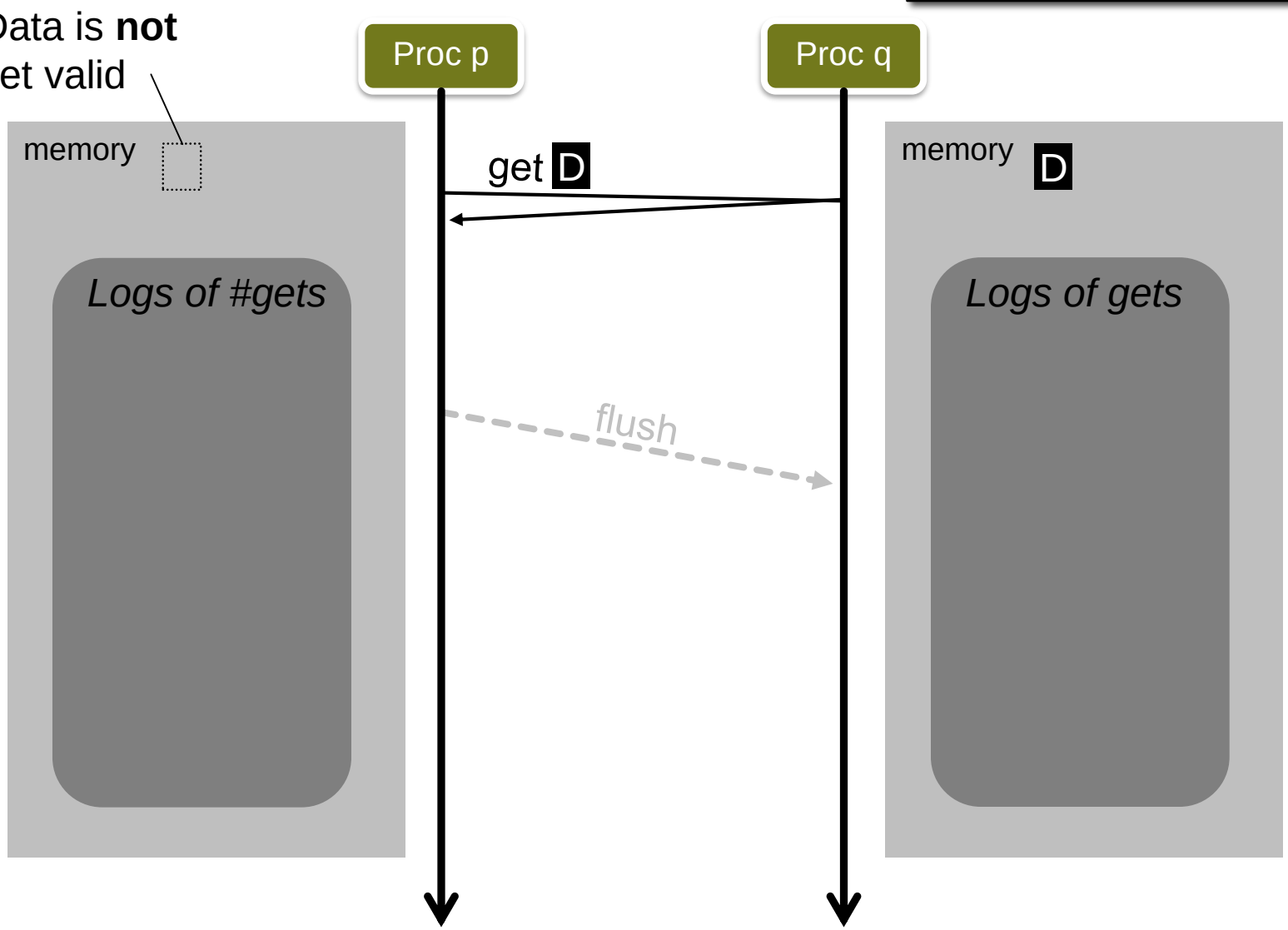

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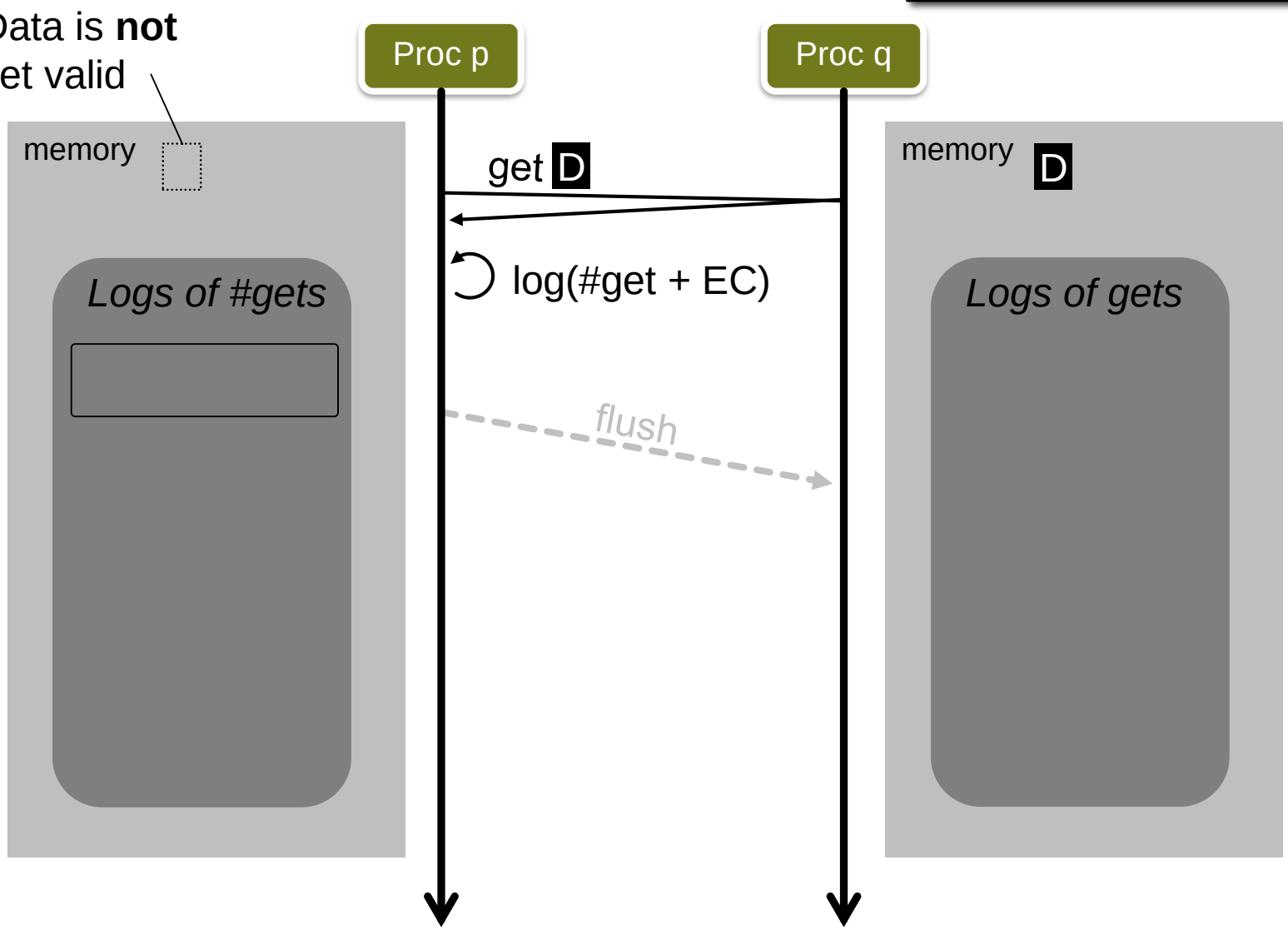

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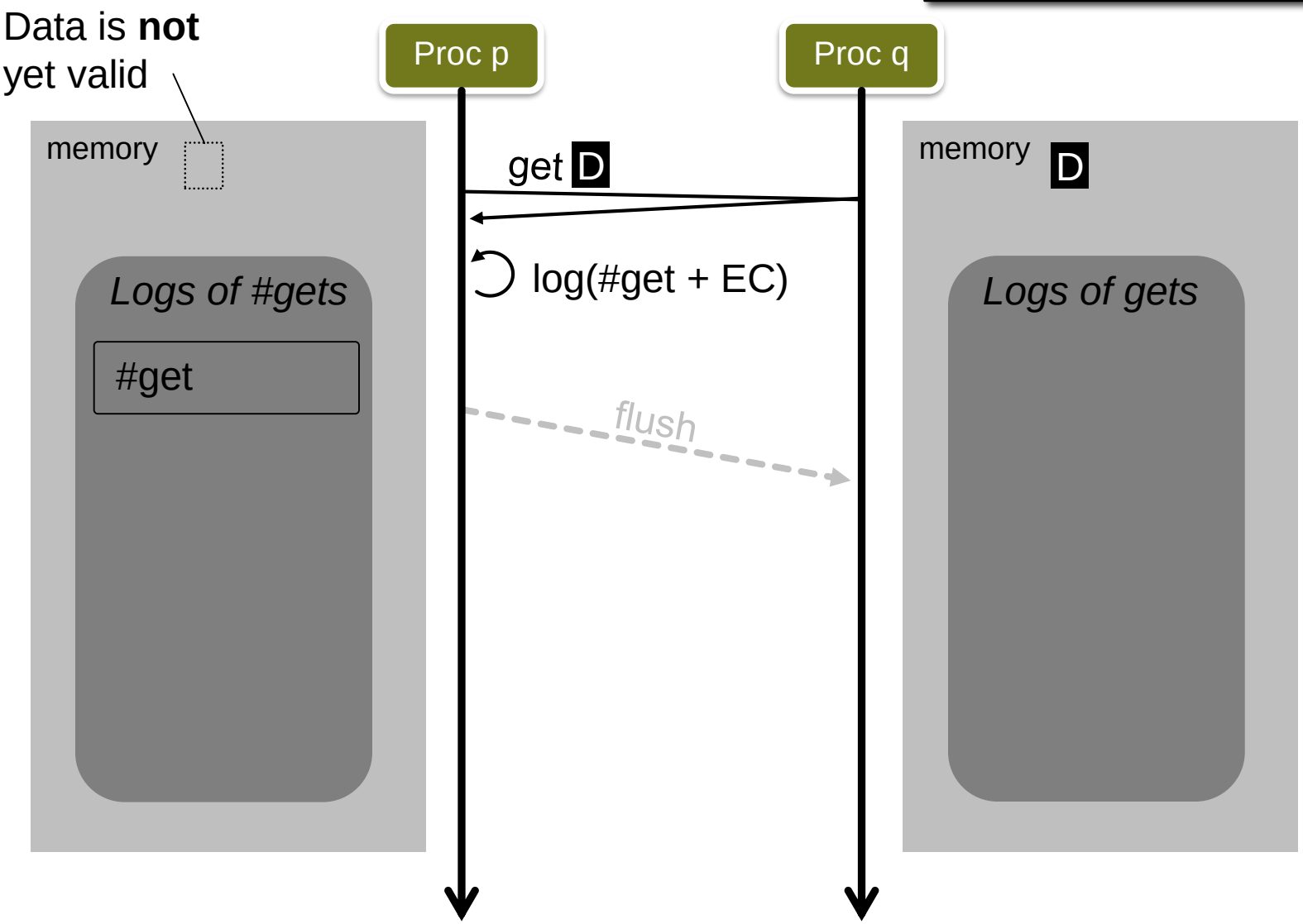

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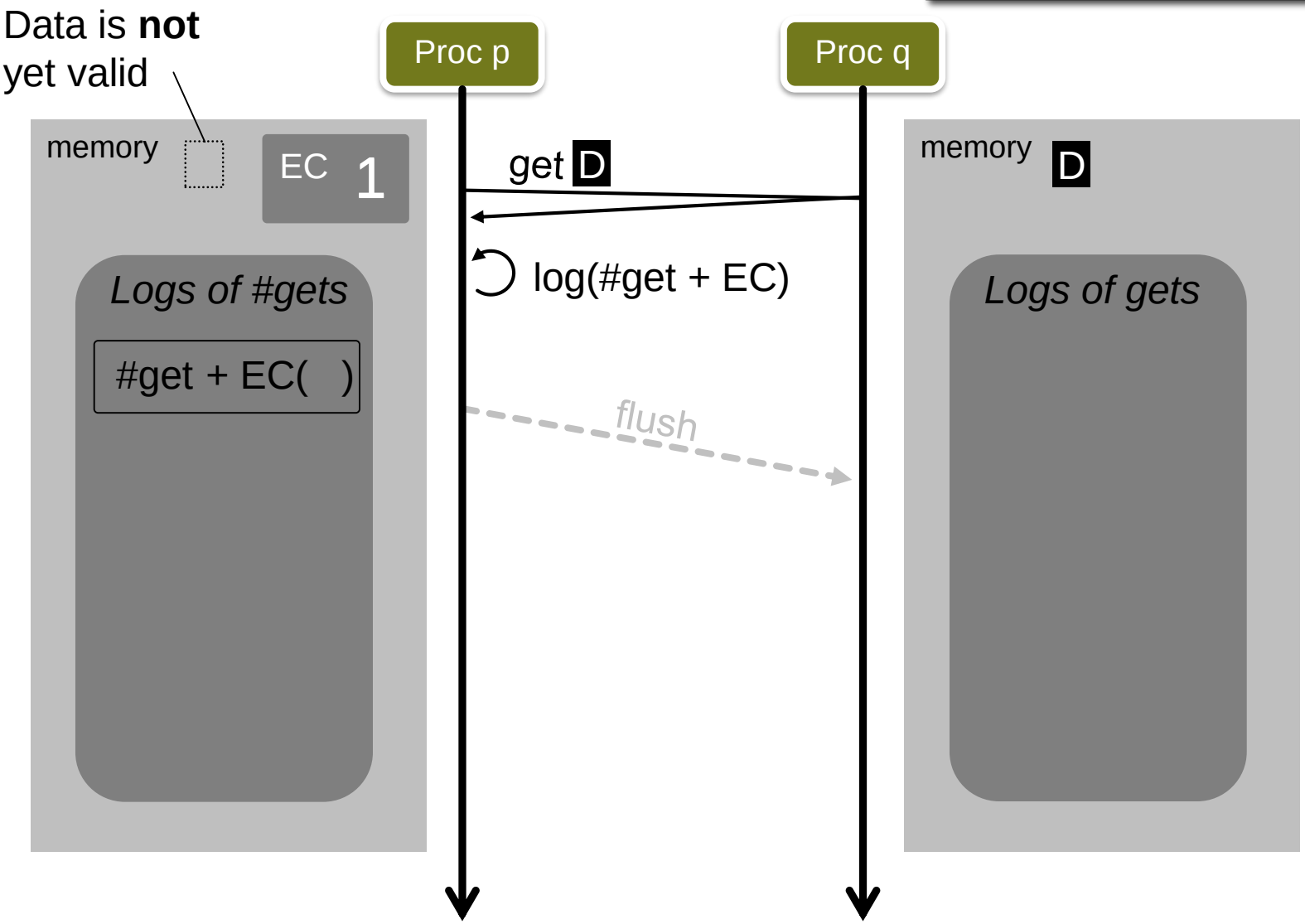

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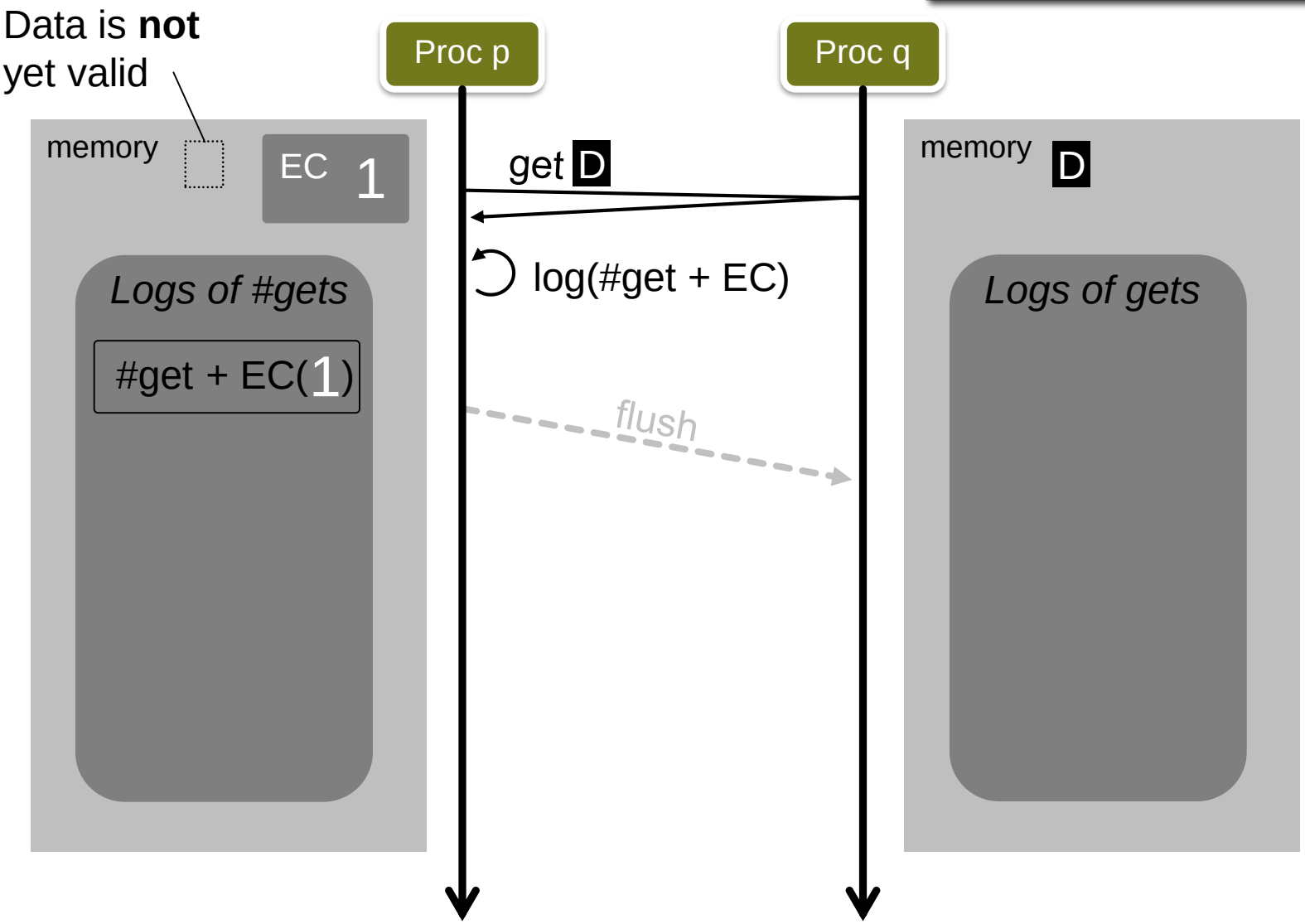

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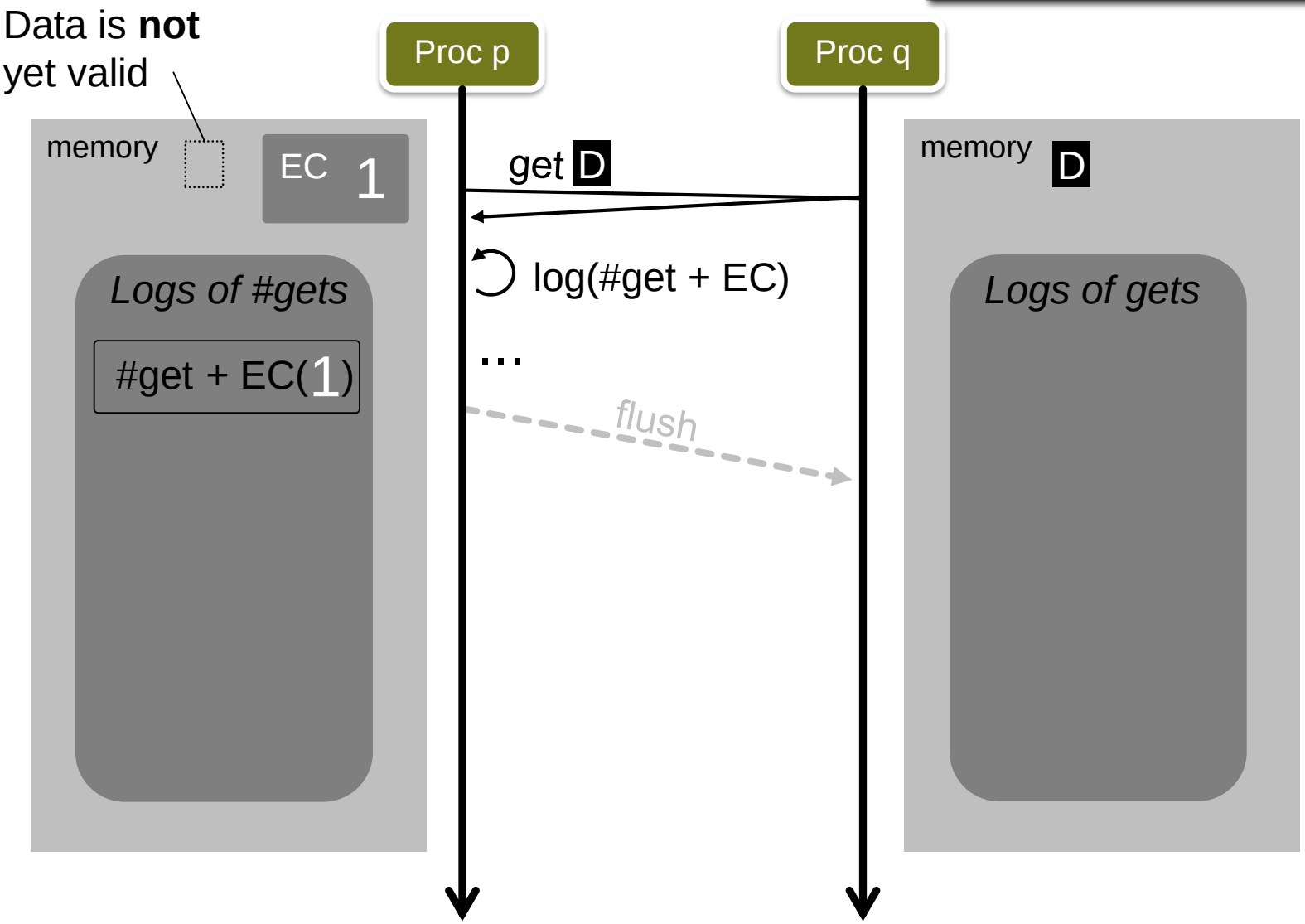

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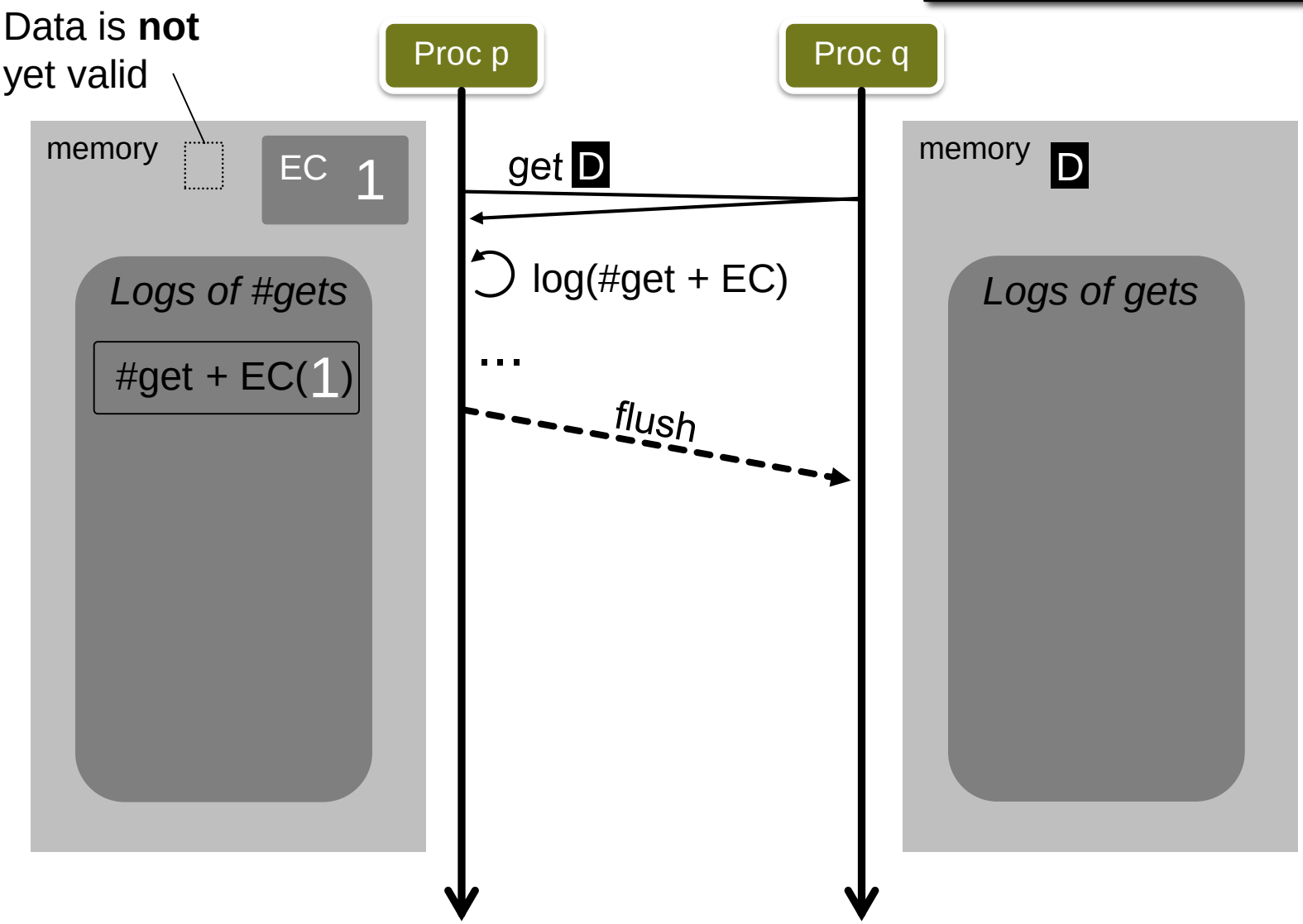

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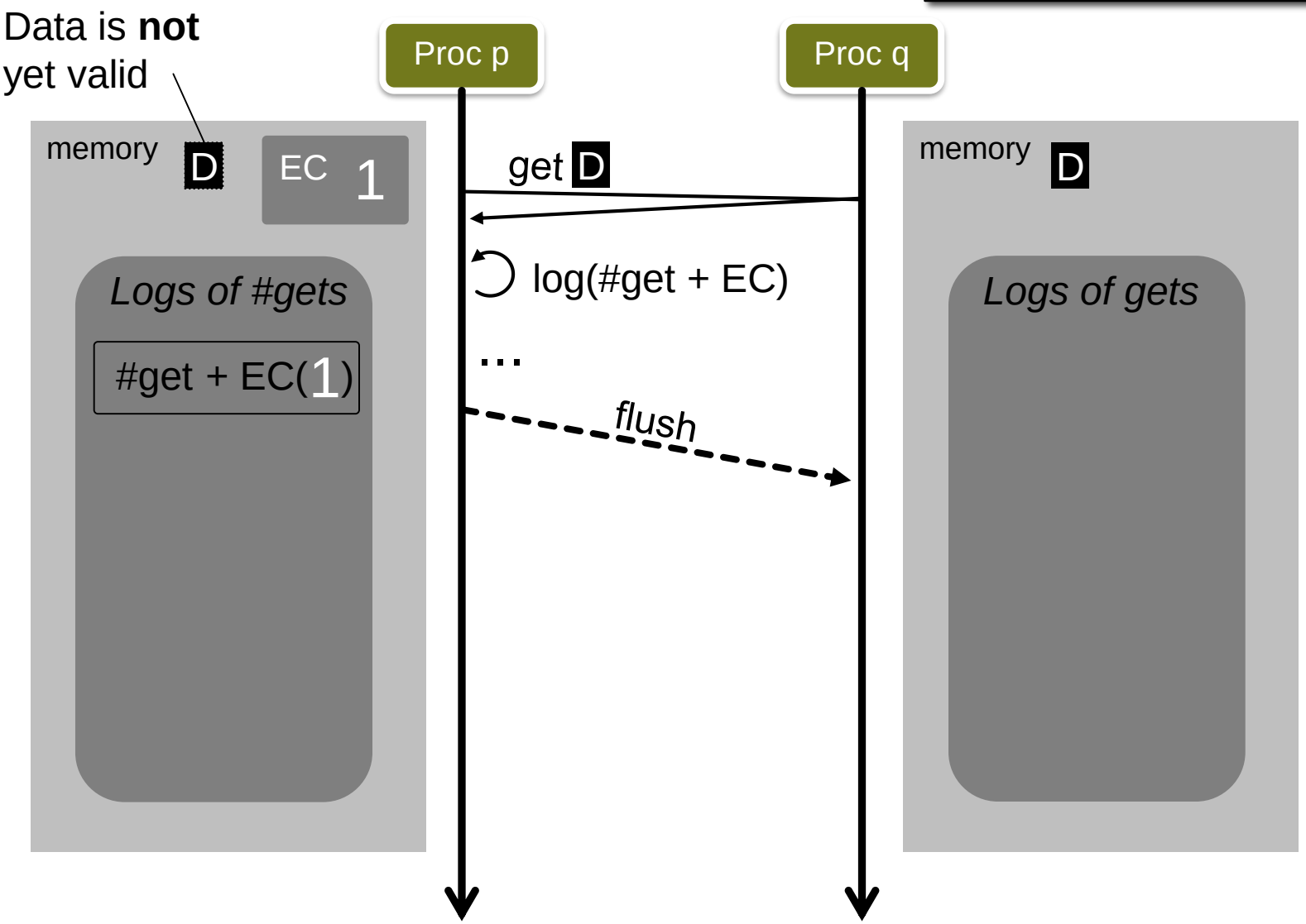

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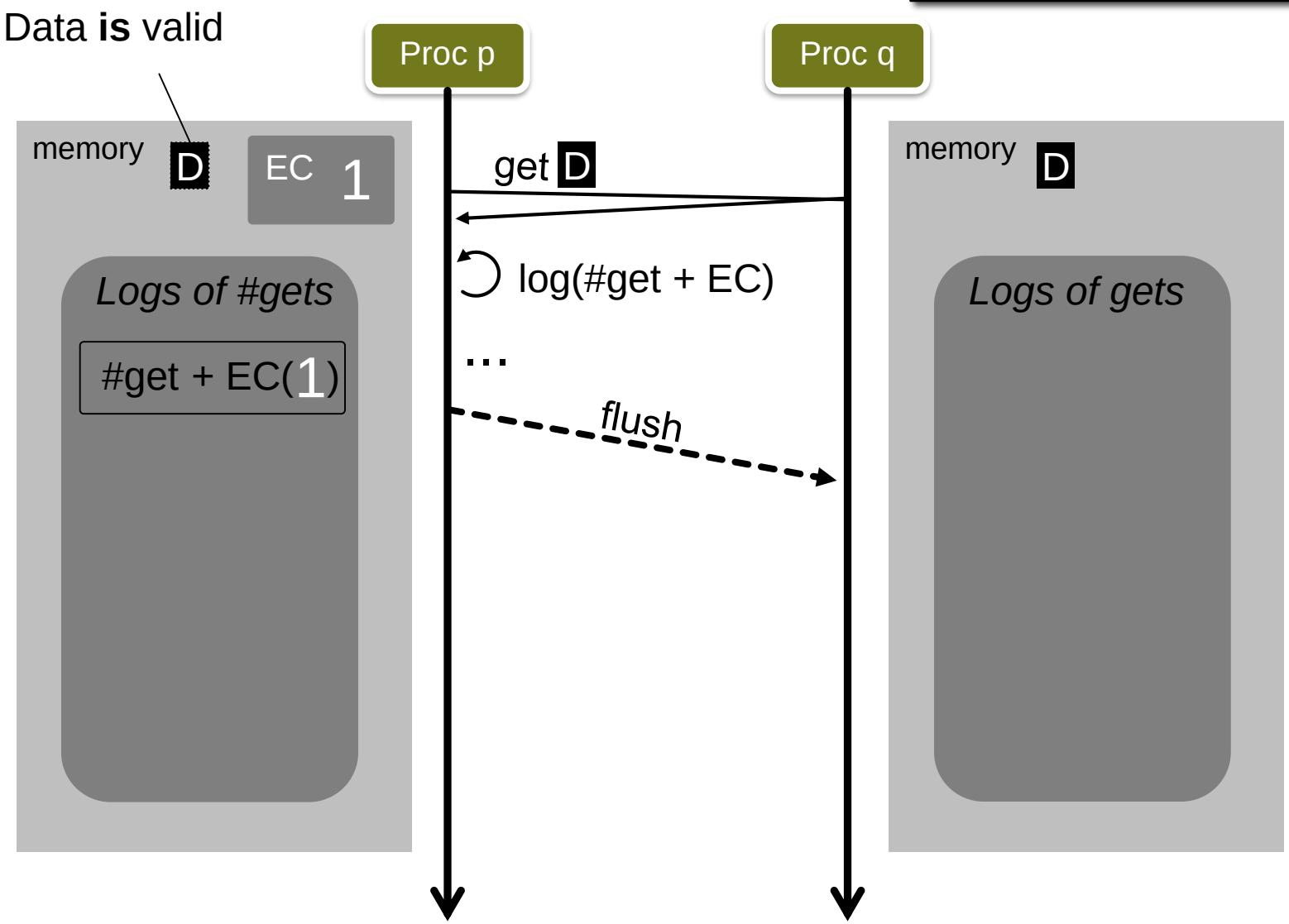

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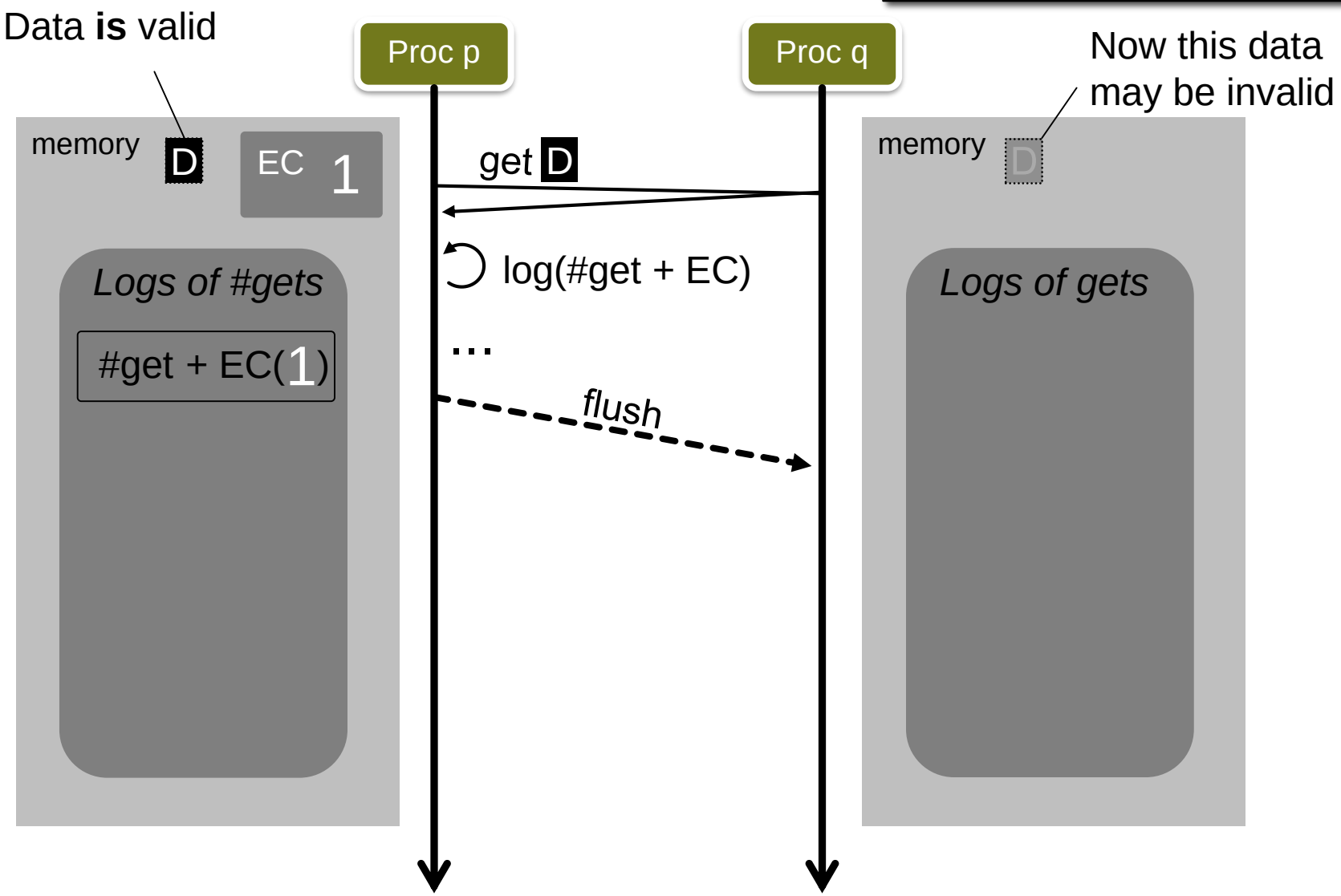

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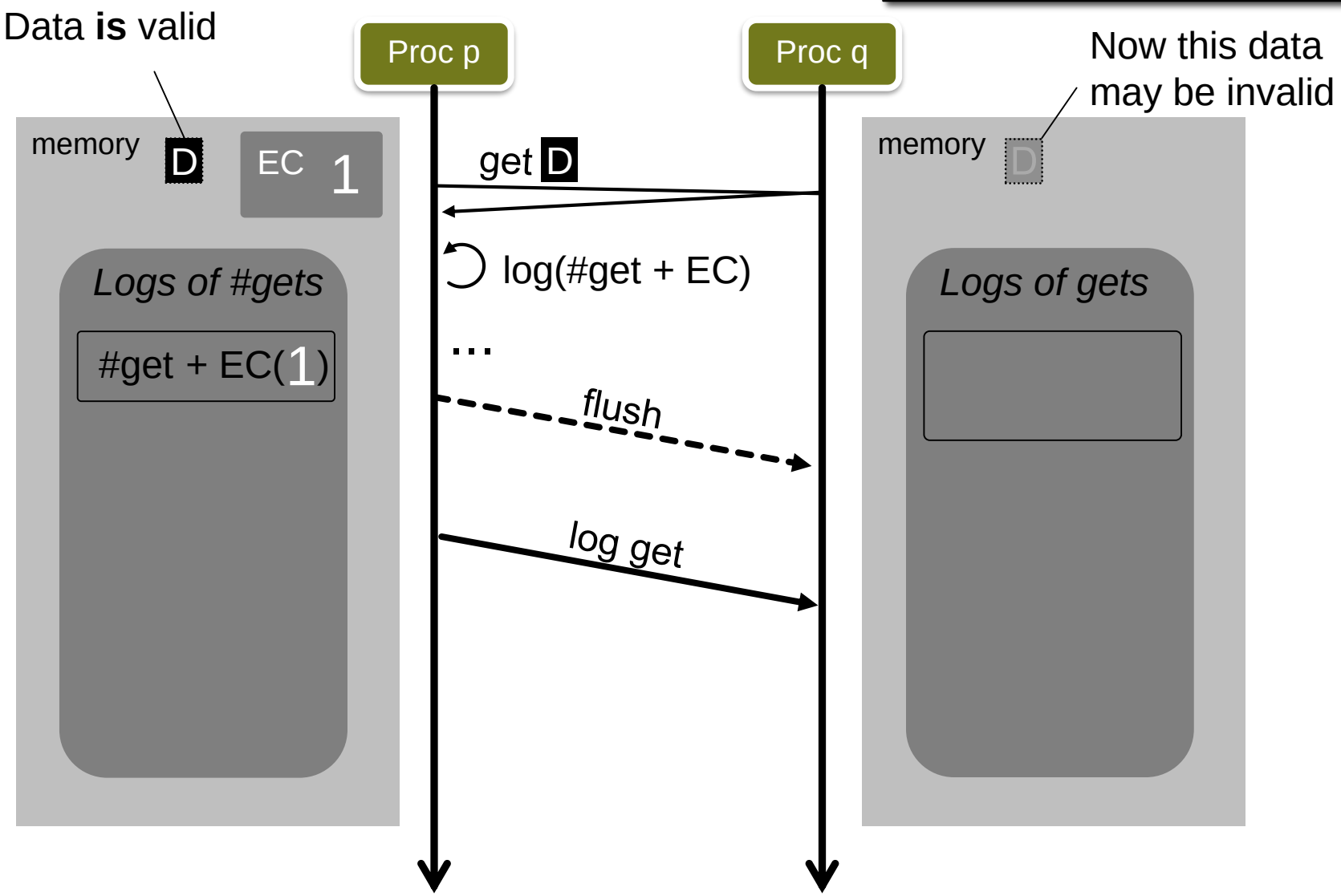

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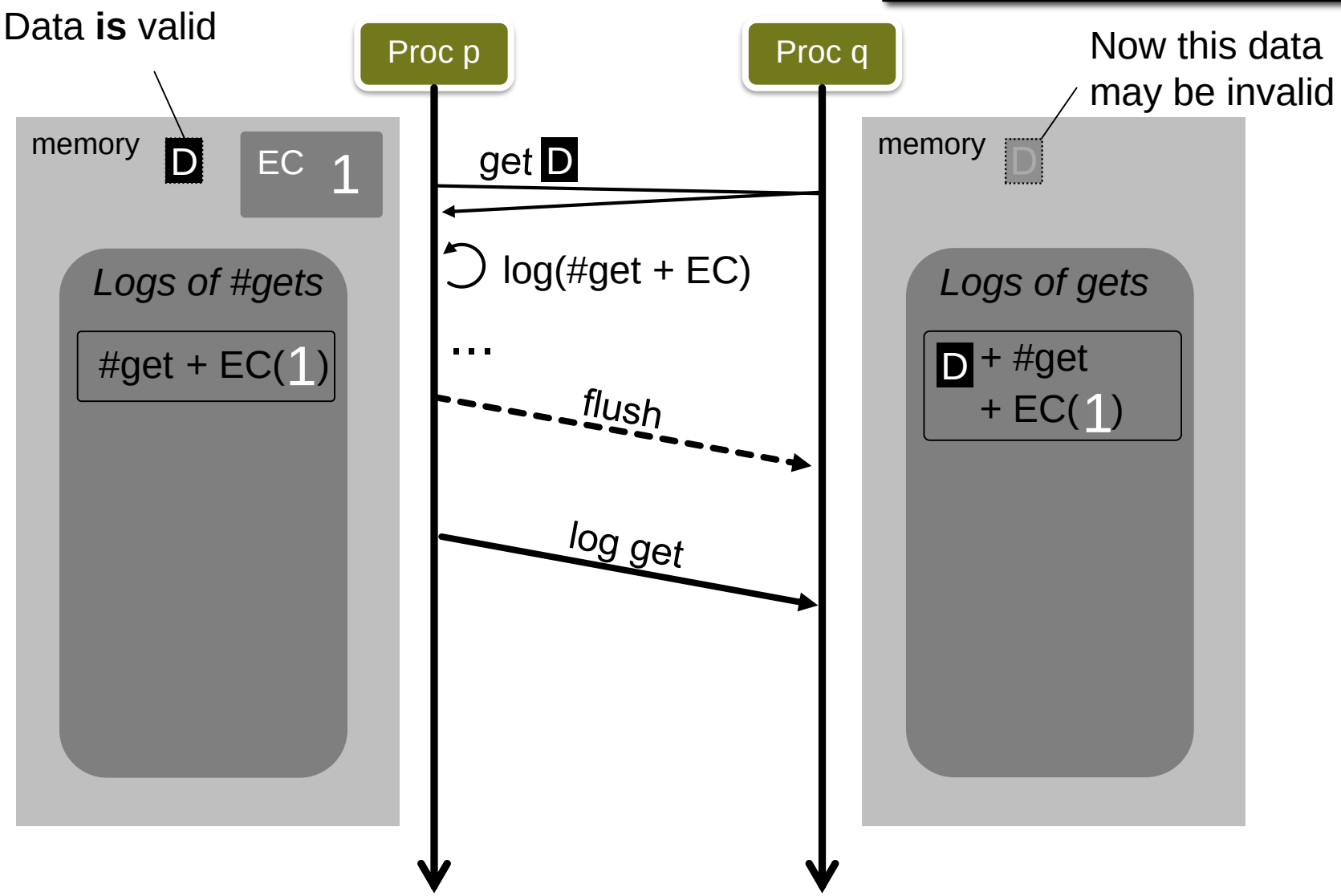

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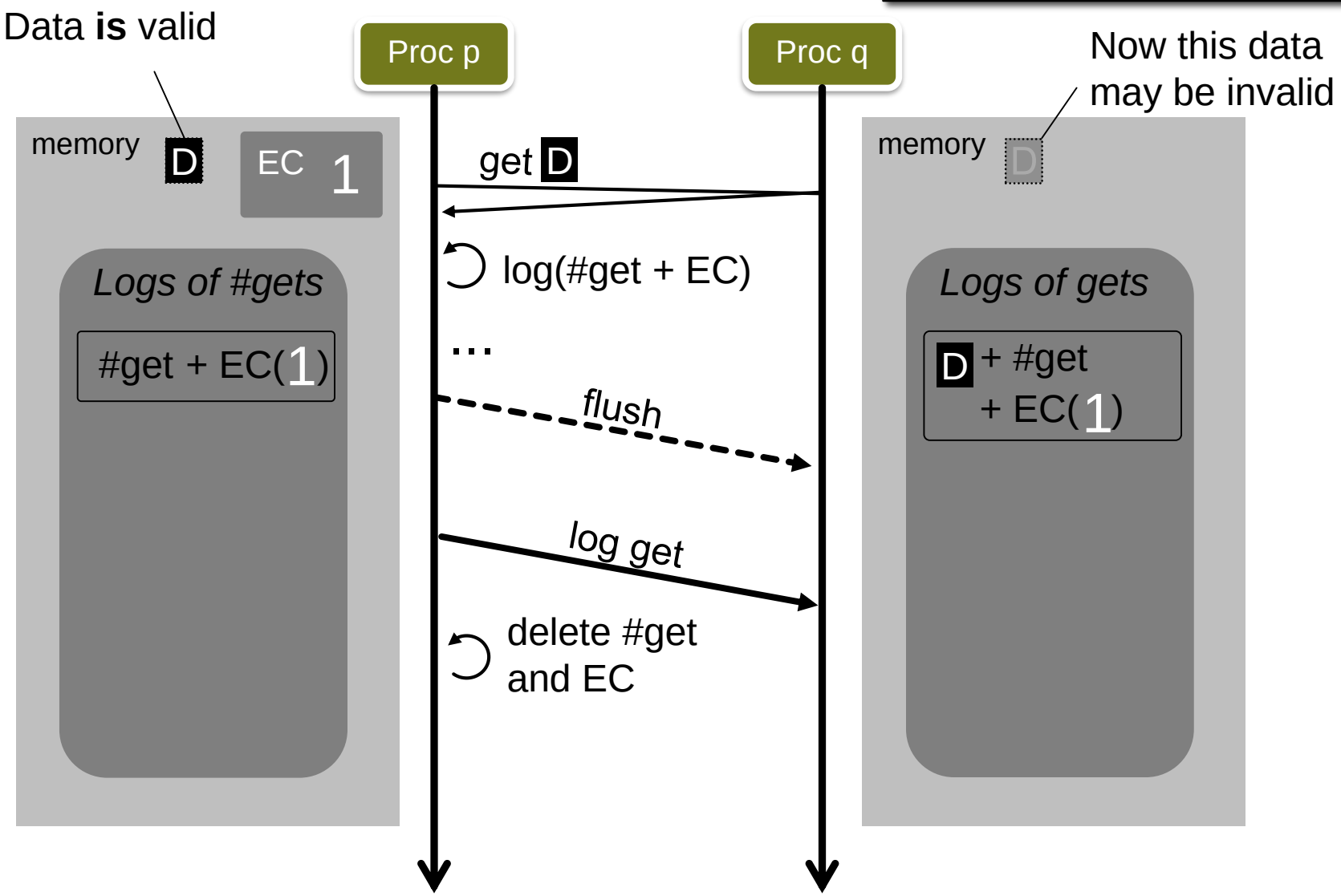

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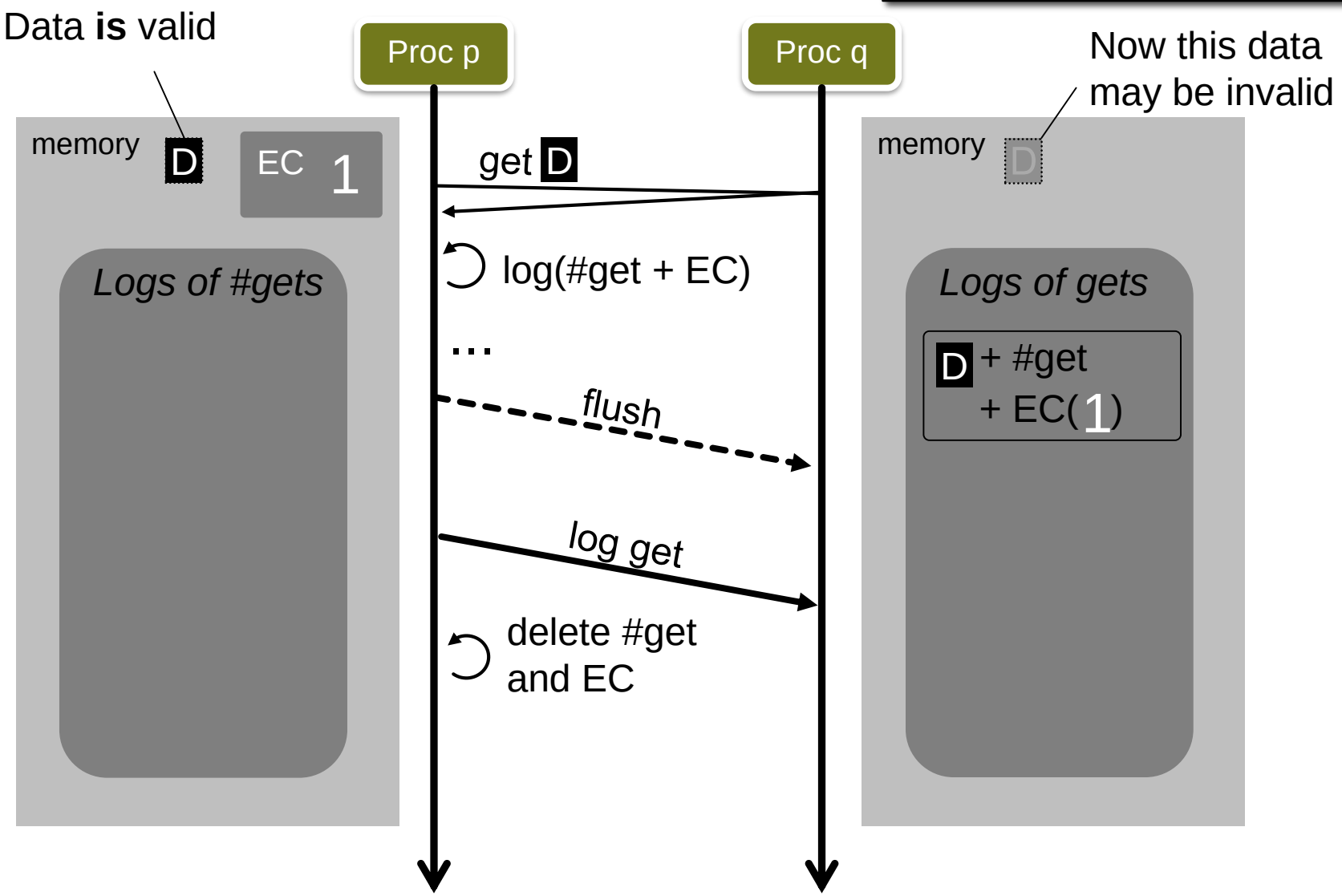

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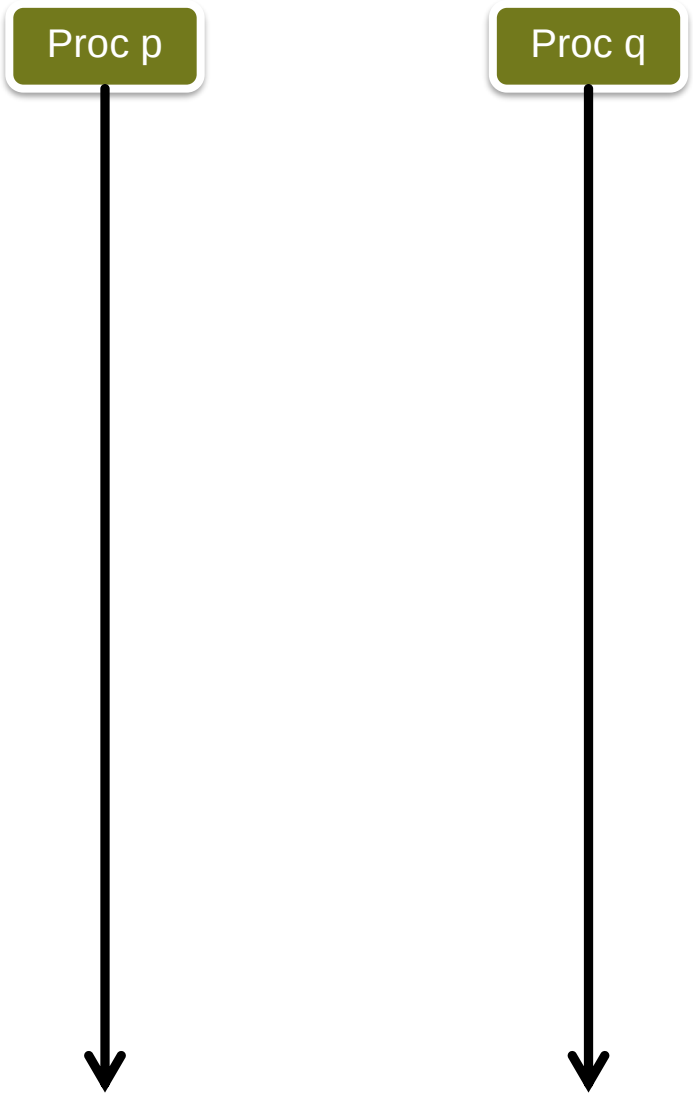


Overview of our Research

Generic model

$$\mathcal{D} = \langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co} \rangle,$$

$\mathrm{PUT}(p \rightrightarrows q)$
$\mathrm{GET}(p \leftrightarrows q)$

MPI-2 PGAS

CC in RMA

MP vs. RMA

Schemes

Recovery in RMA

Basic scheme

Extended RMA semantics

Proofs

Theorem 4.2. *The recove rithm 2 preserves the* $\xrightarrow{cohb}$ *or ferred to as the* gsync order*).*

Deadlock freedom
Correct recovery

Holistic fault-tolerance library

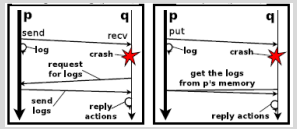
Design

Checkpoints on demand

Optimizations

Performance

UC in RMA



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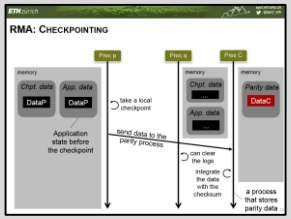
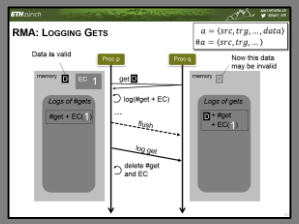


Checkpointing schemes



Logging accesses

Topology-awareness

$$\langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \mathcal{H}, \mathcal{G}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co}, \mathcal{M} \rangle$$

Model extensions

Distribution of processes

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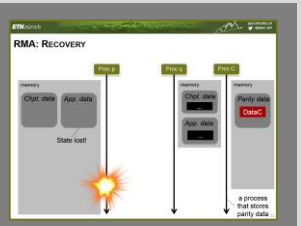

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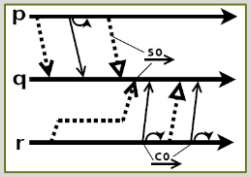

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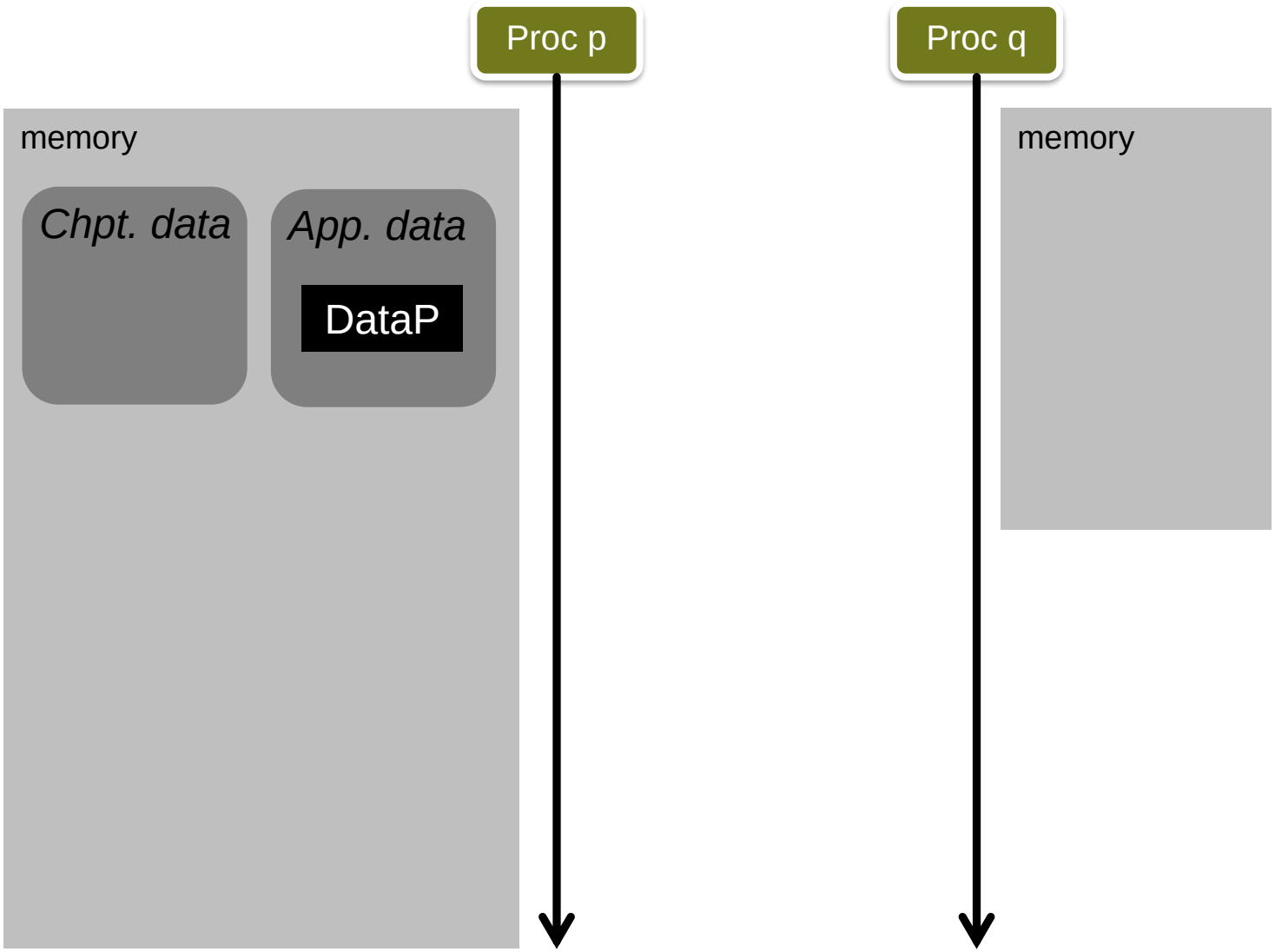

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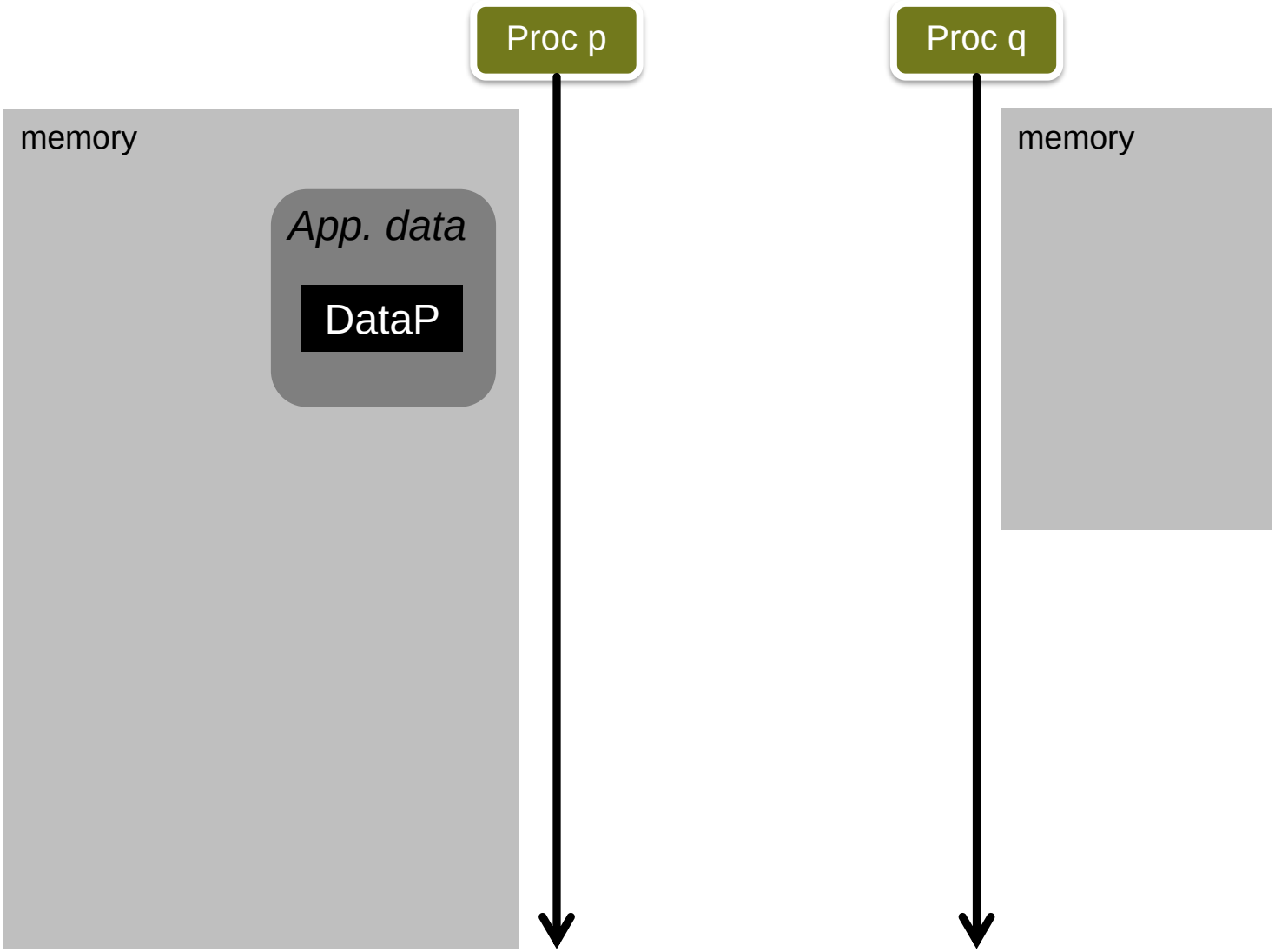

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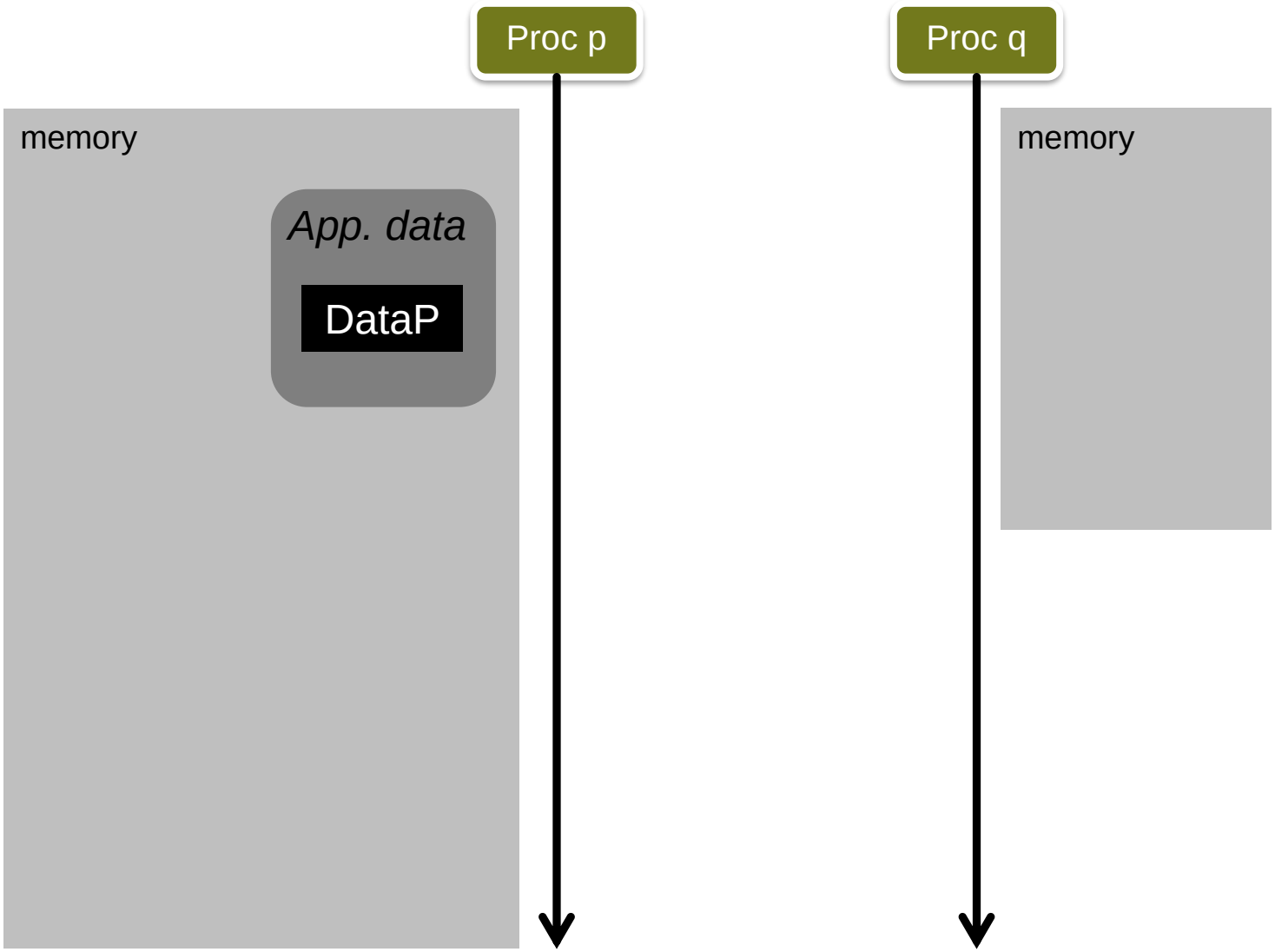

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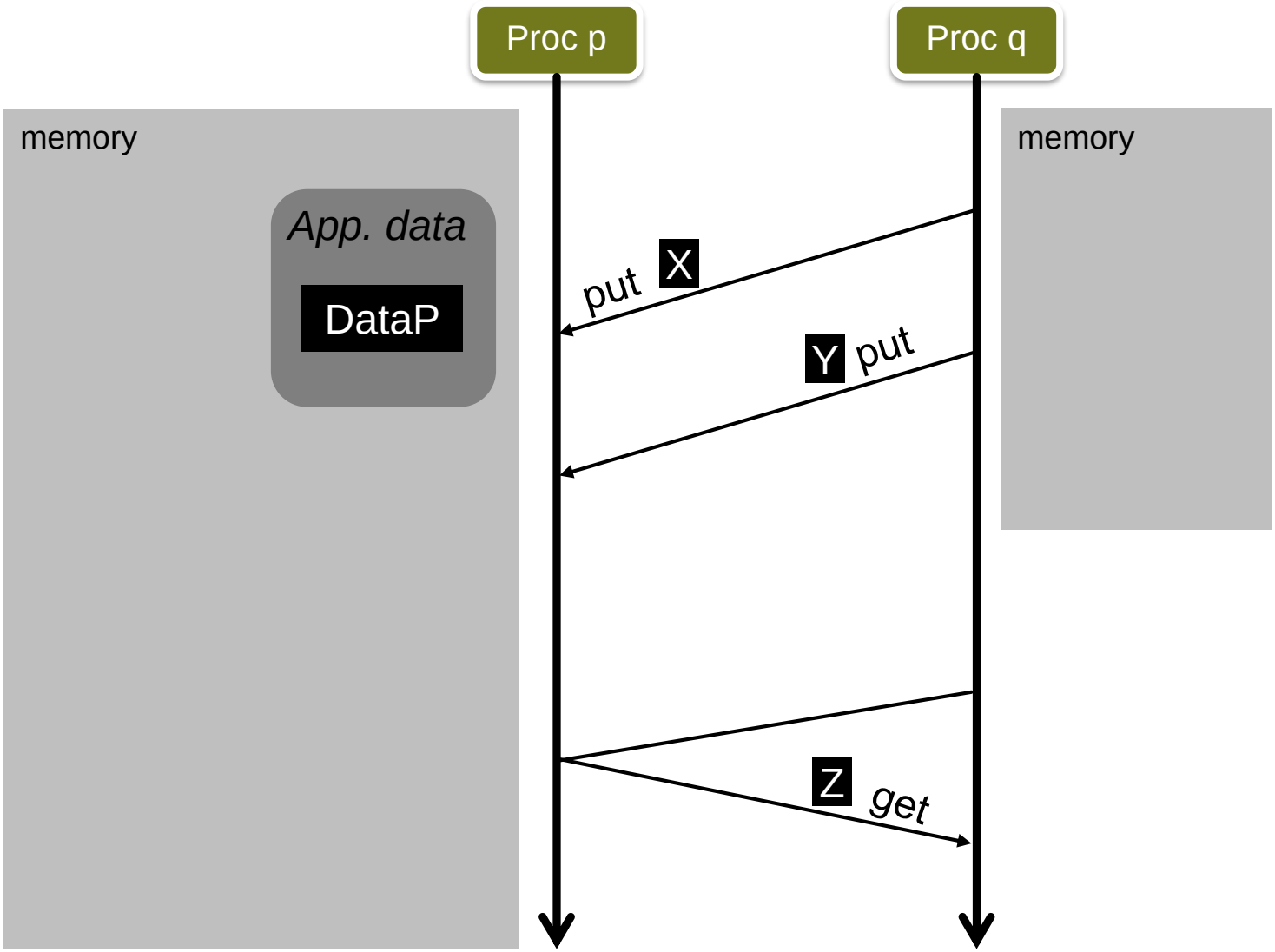

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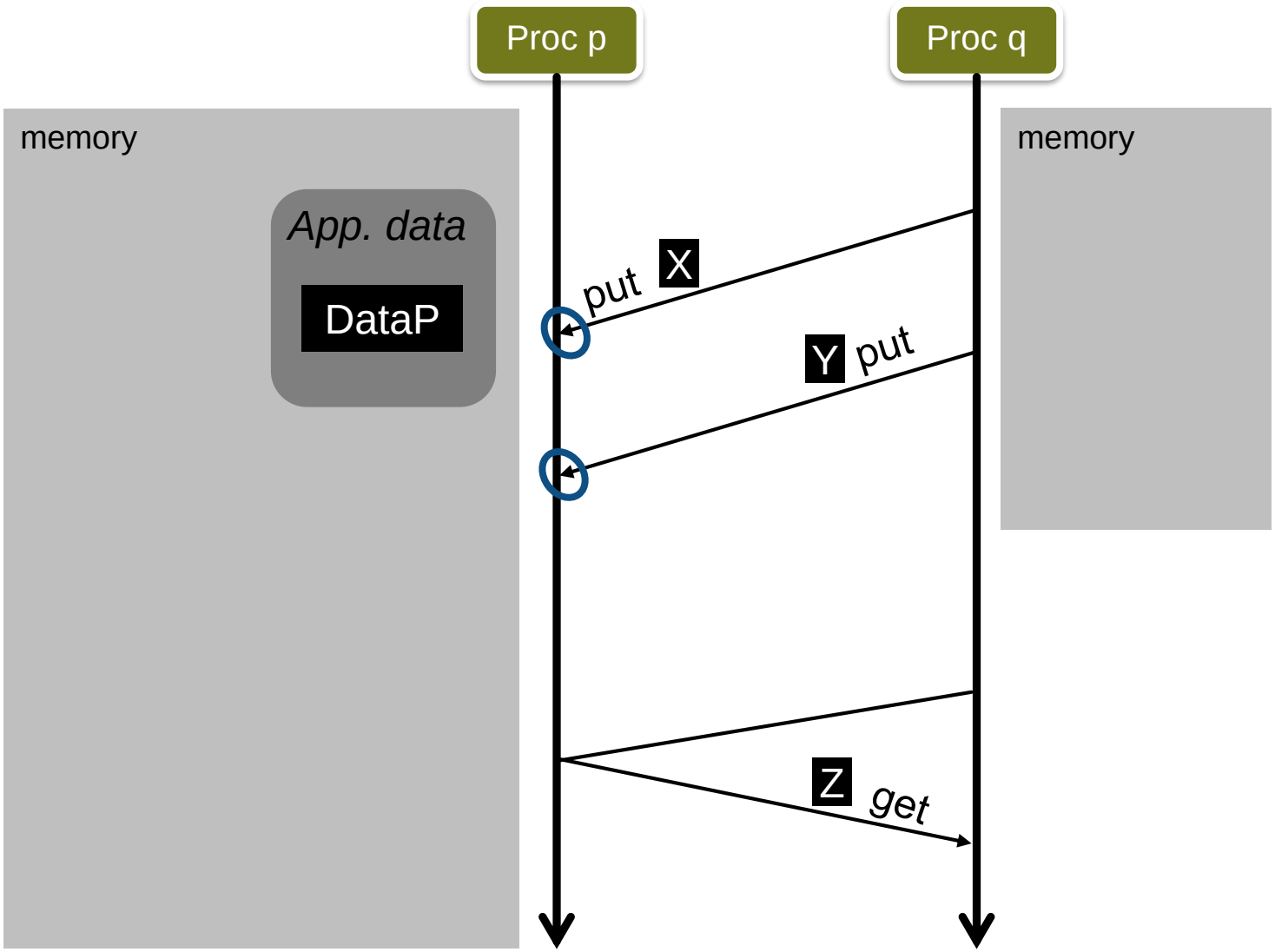

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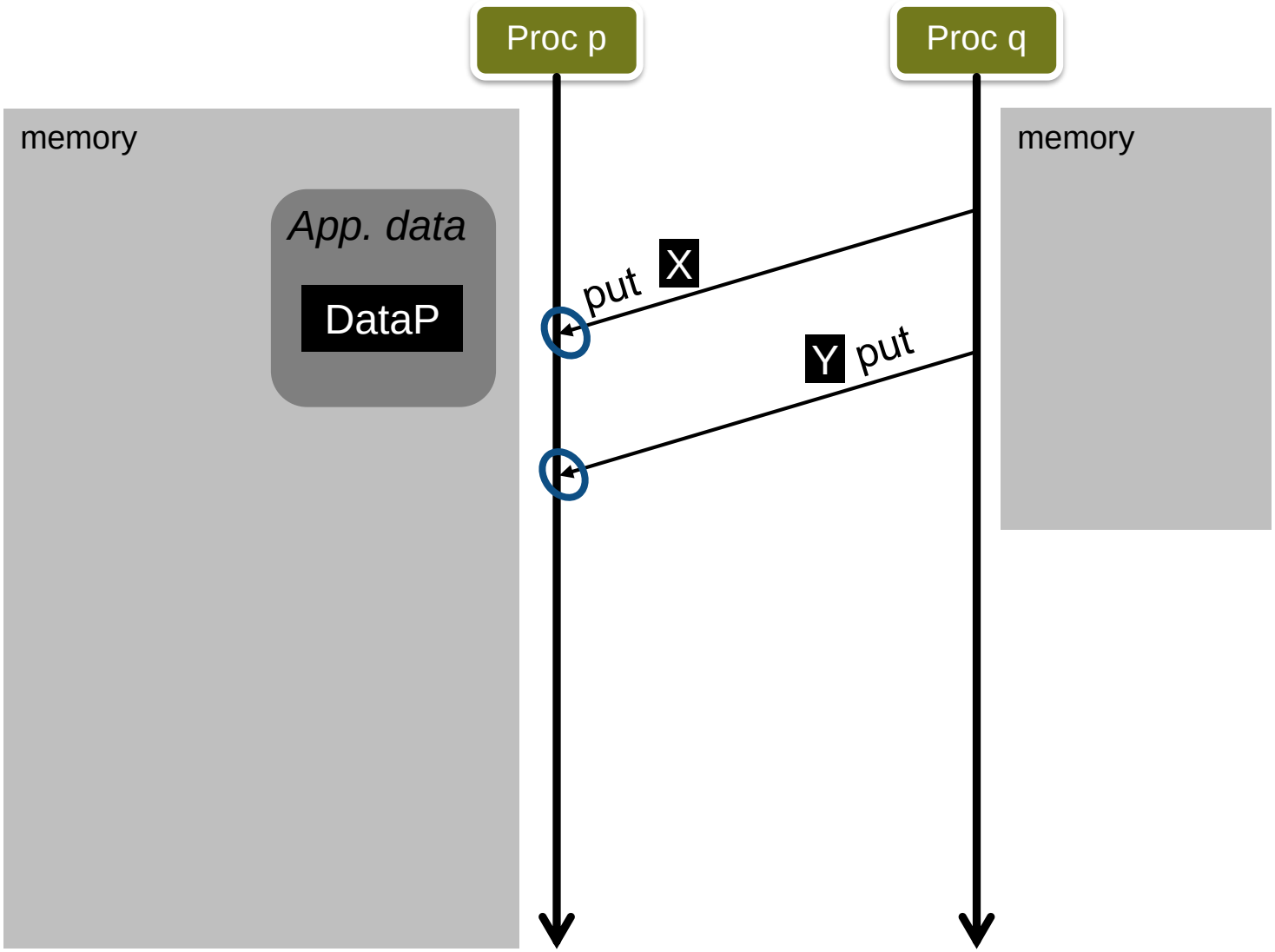

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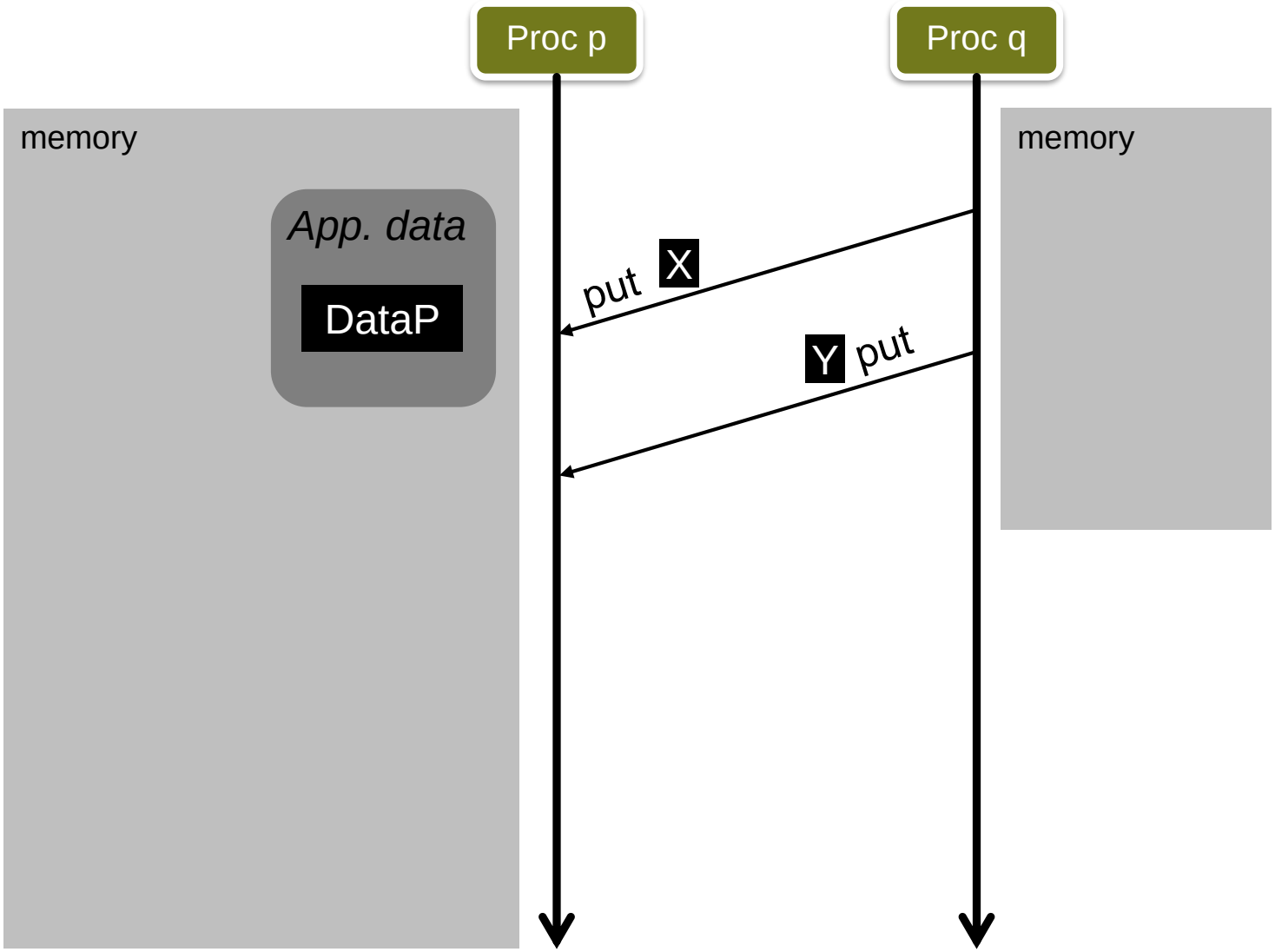

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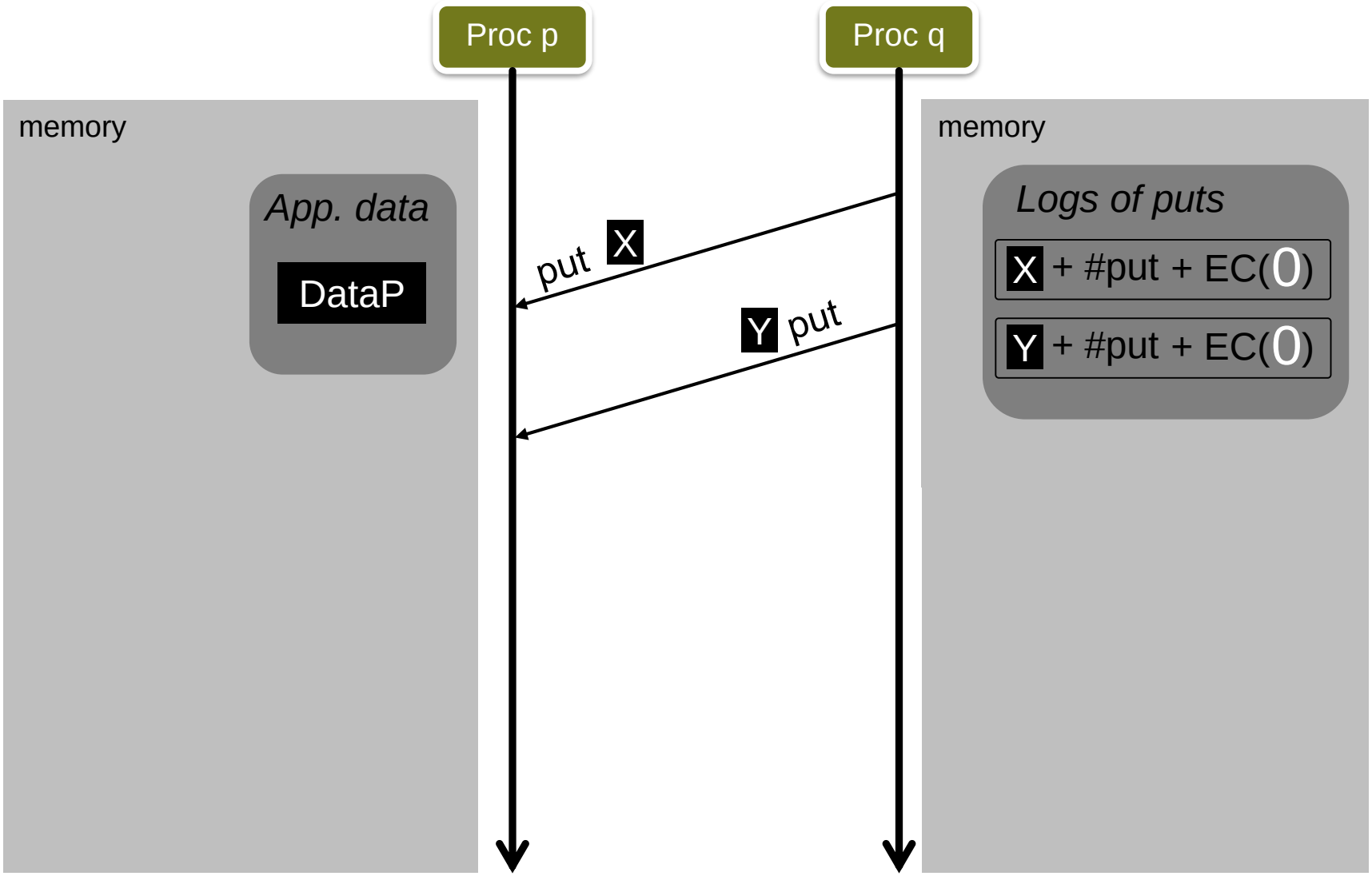

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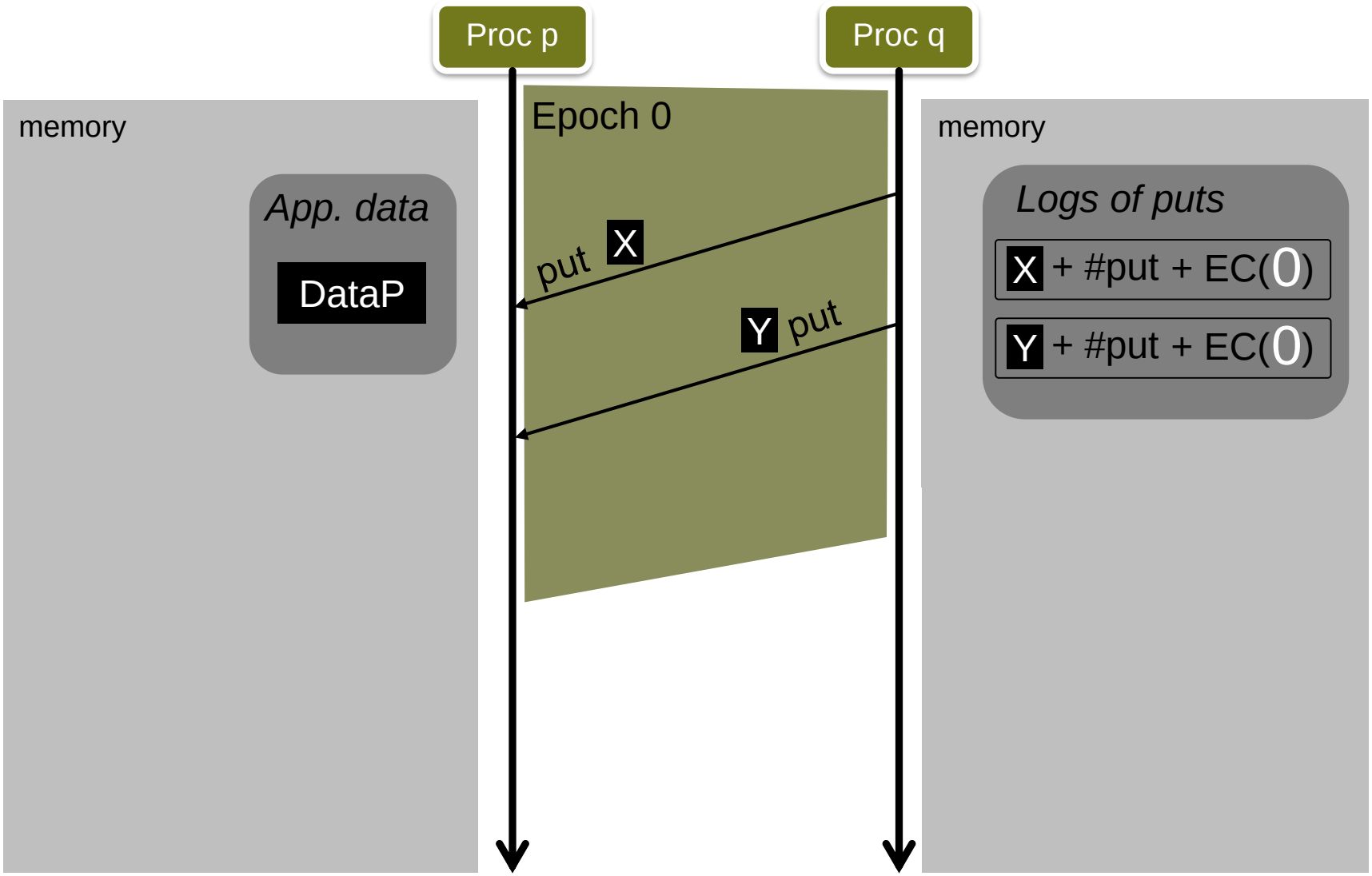

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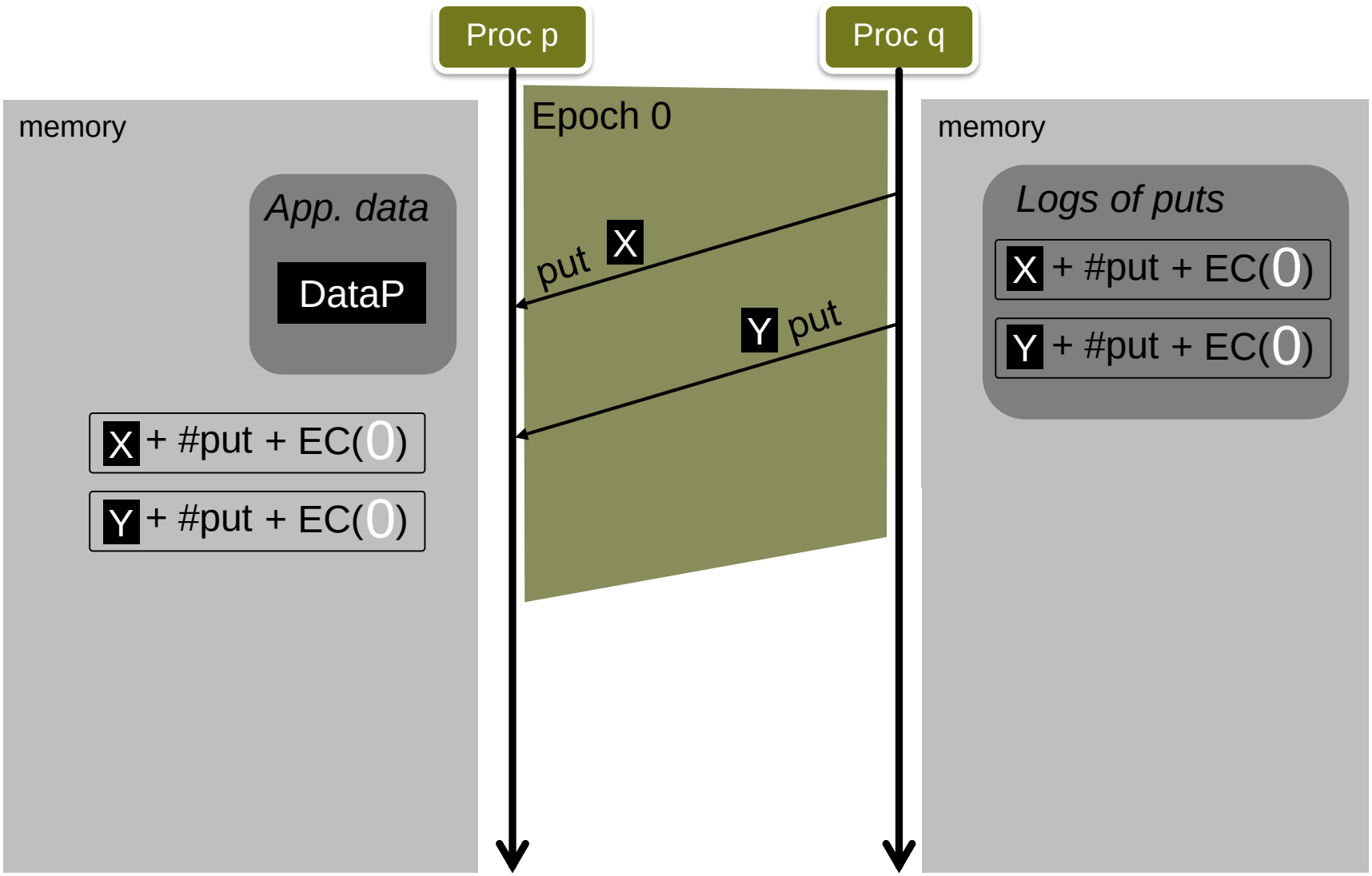

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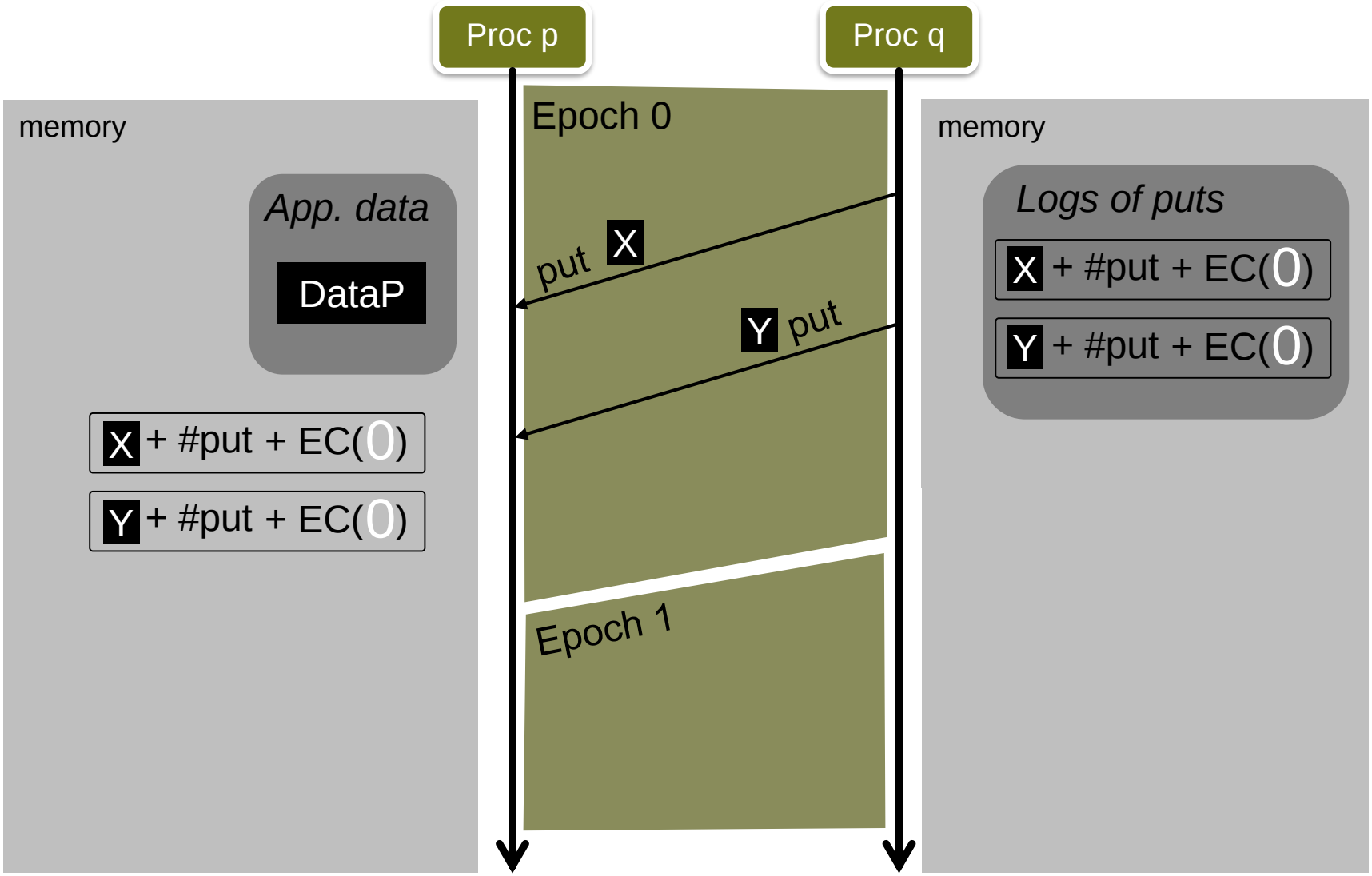

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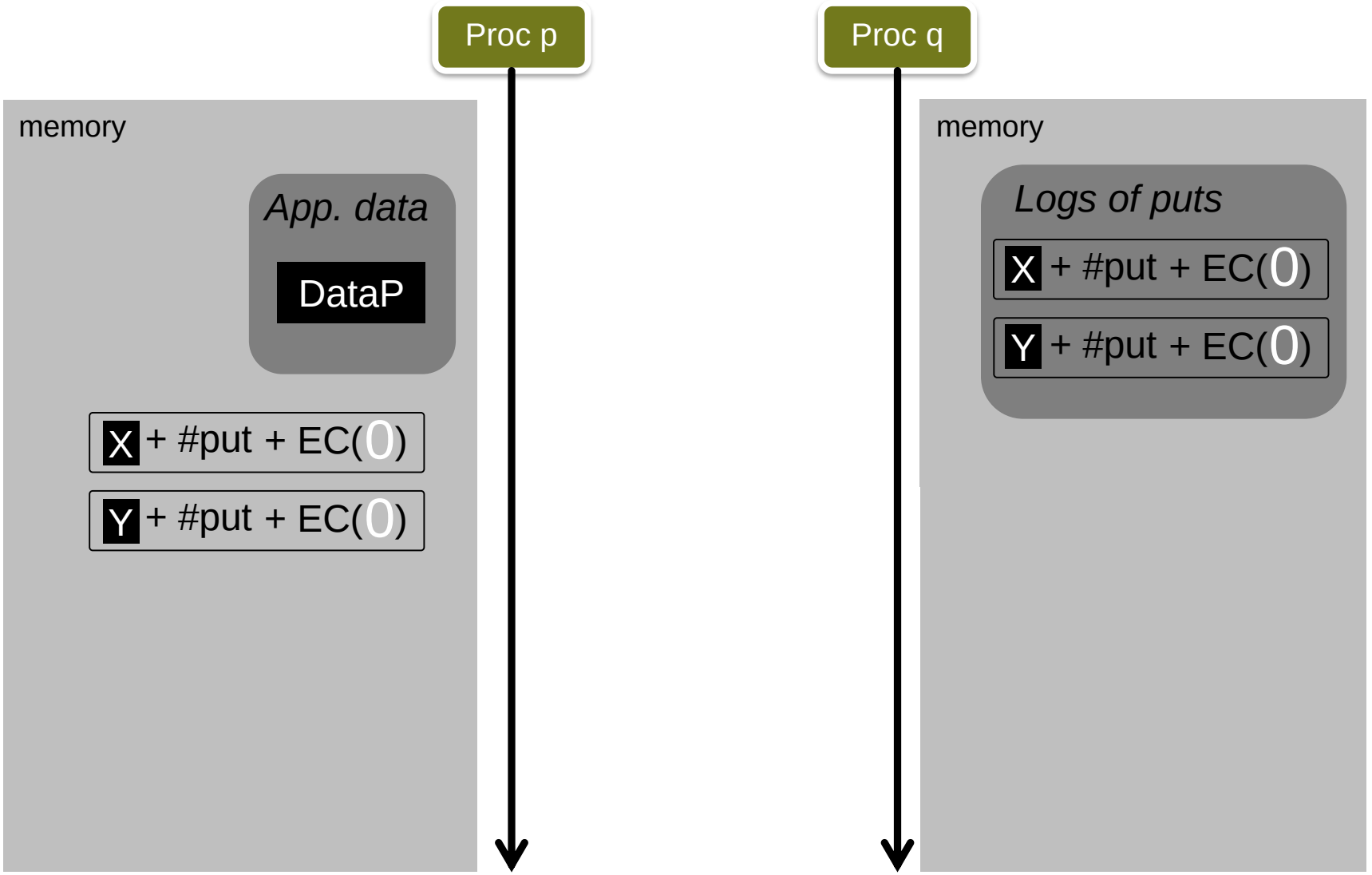

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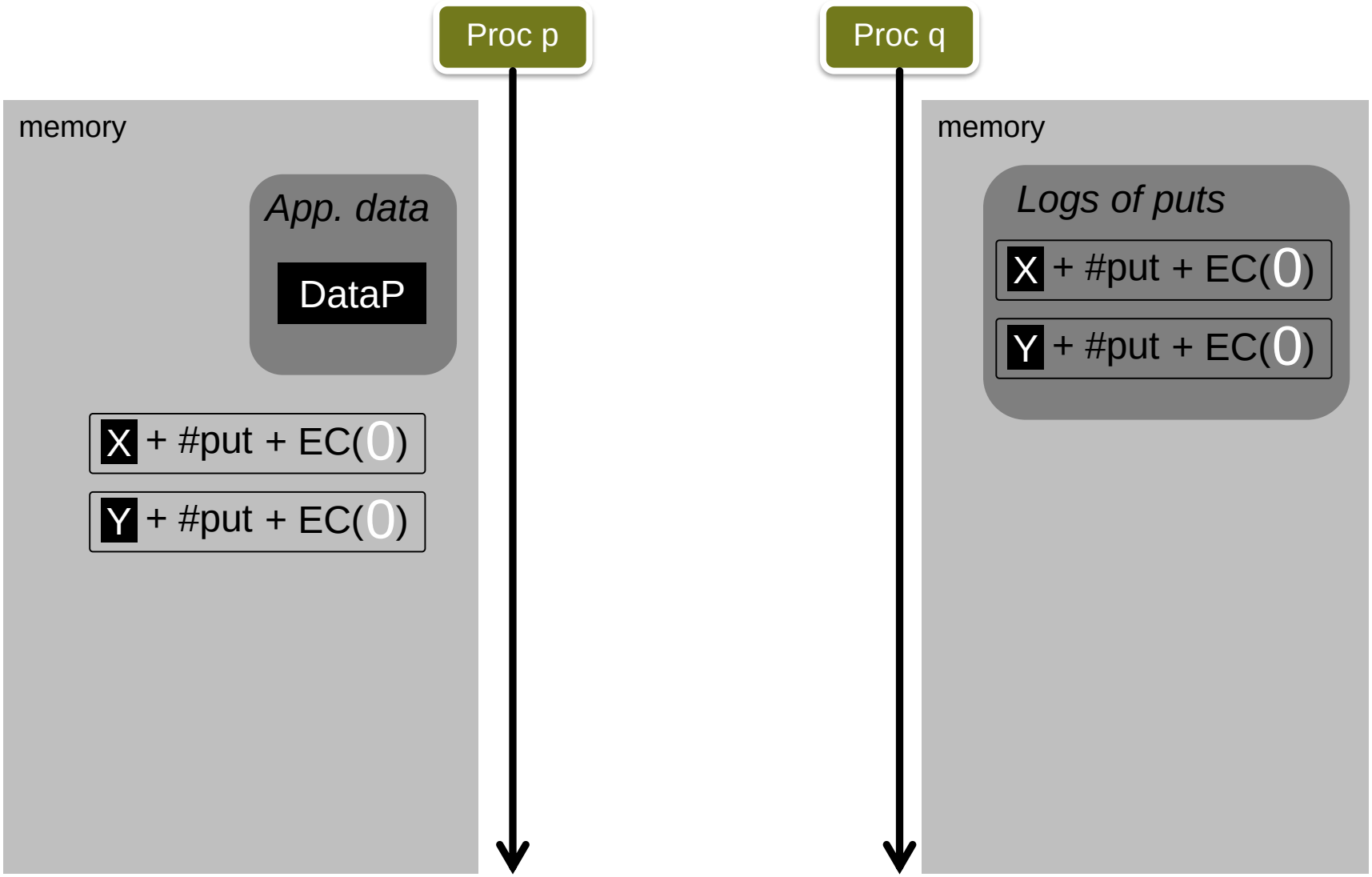

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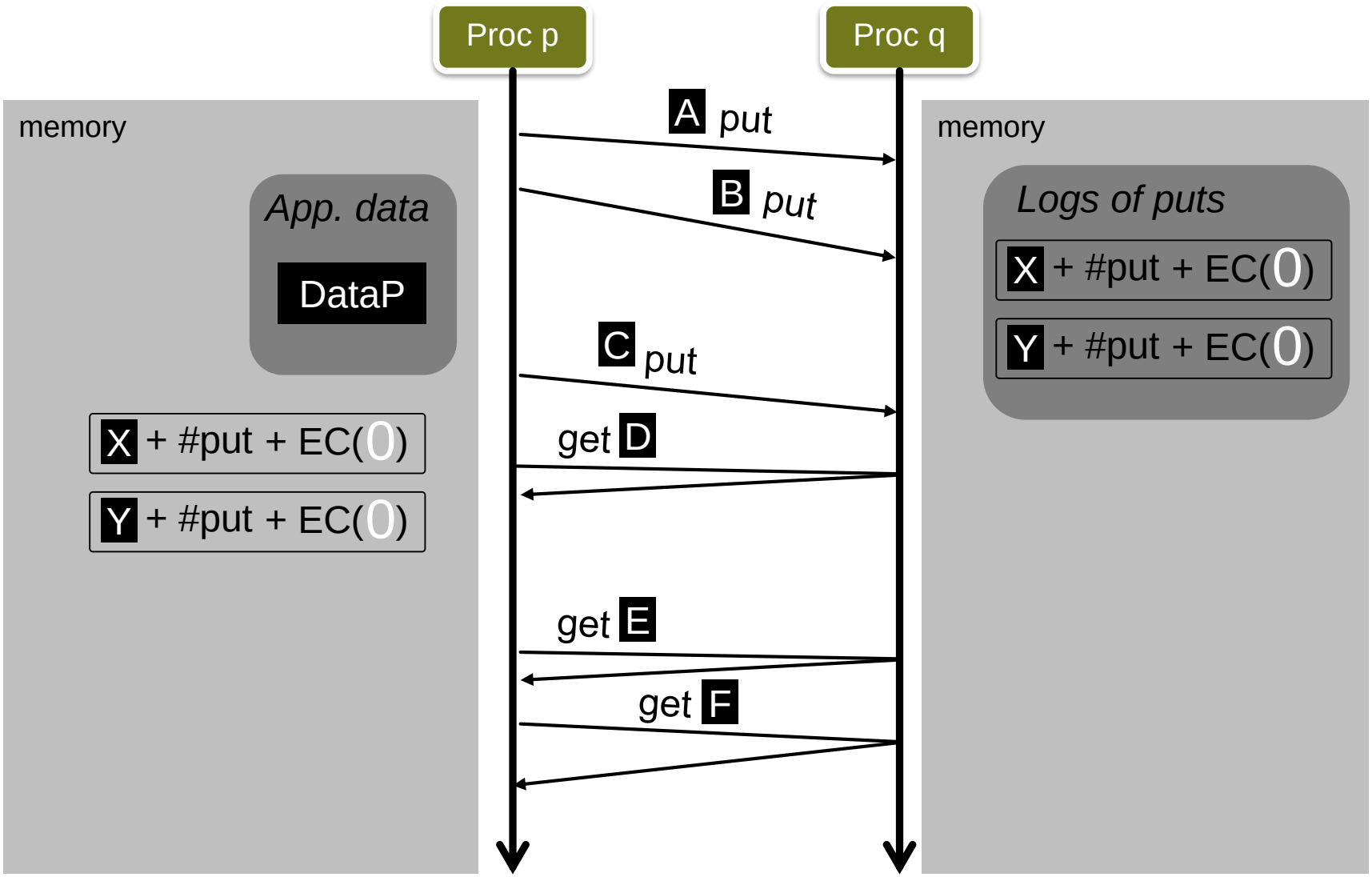

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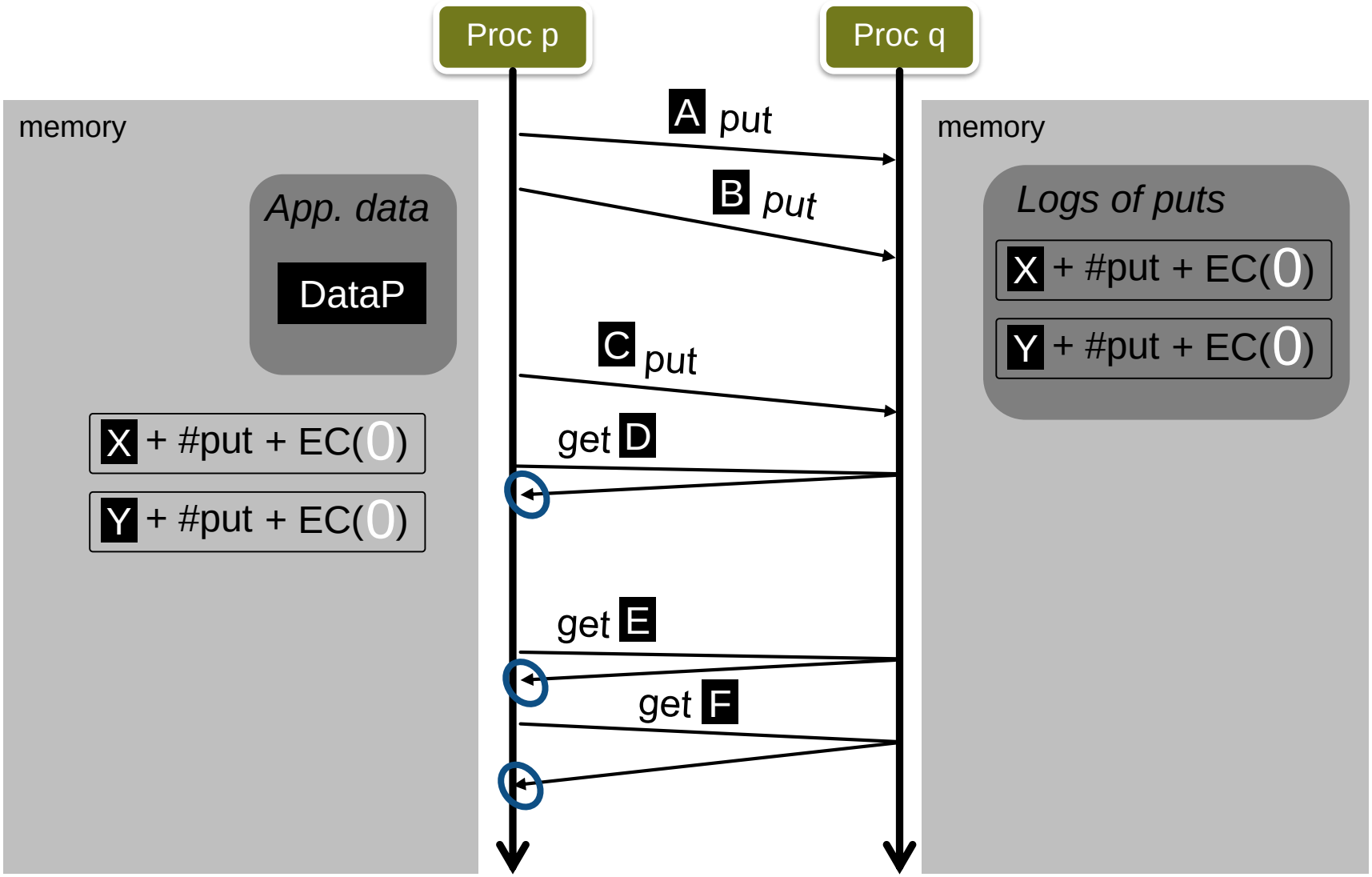

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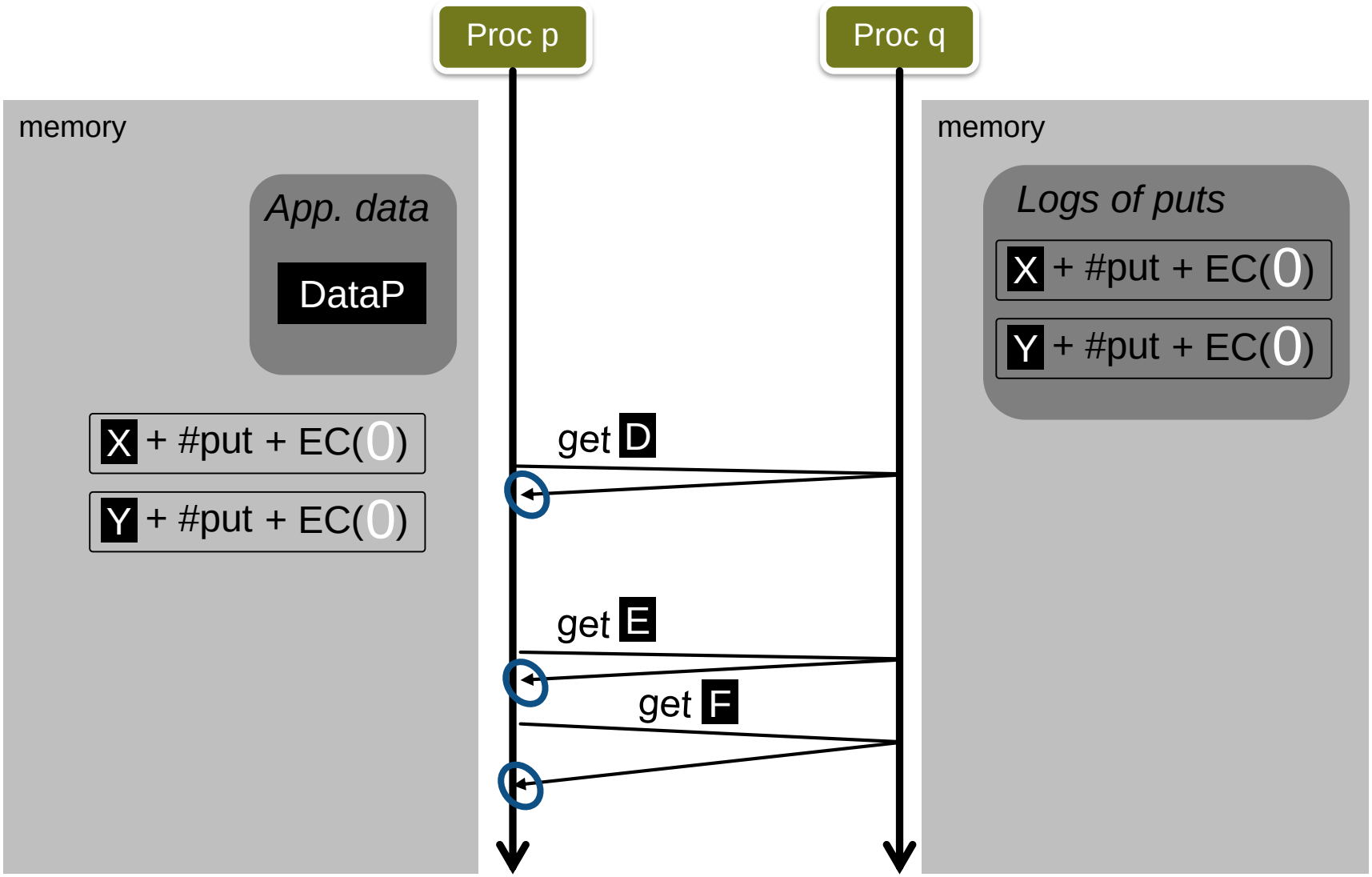

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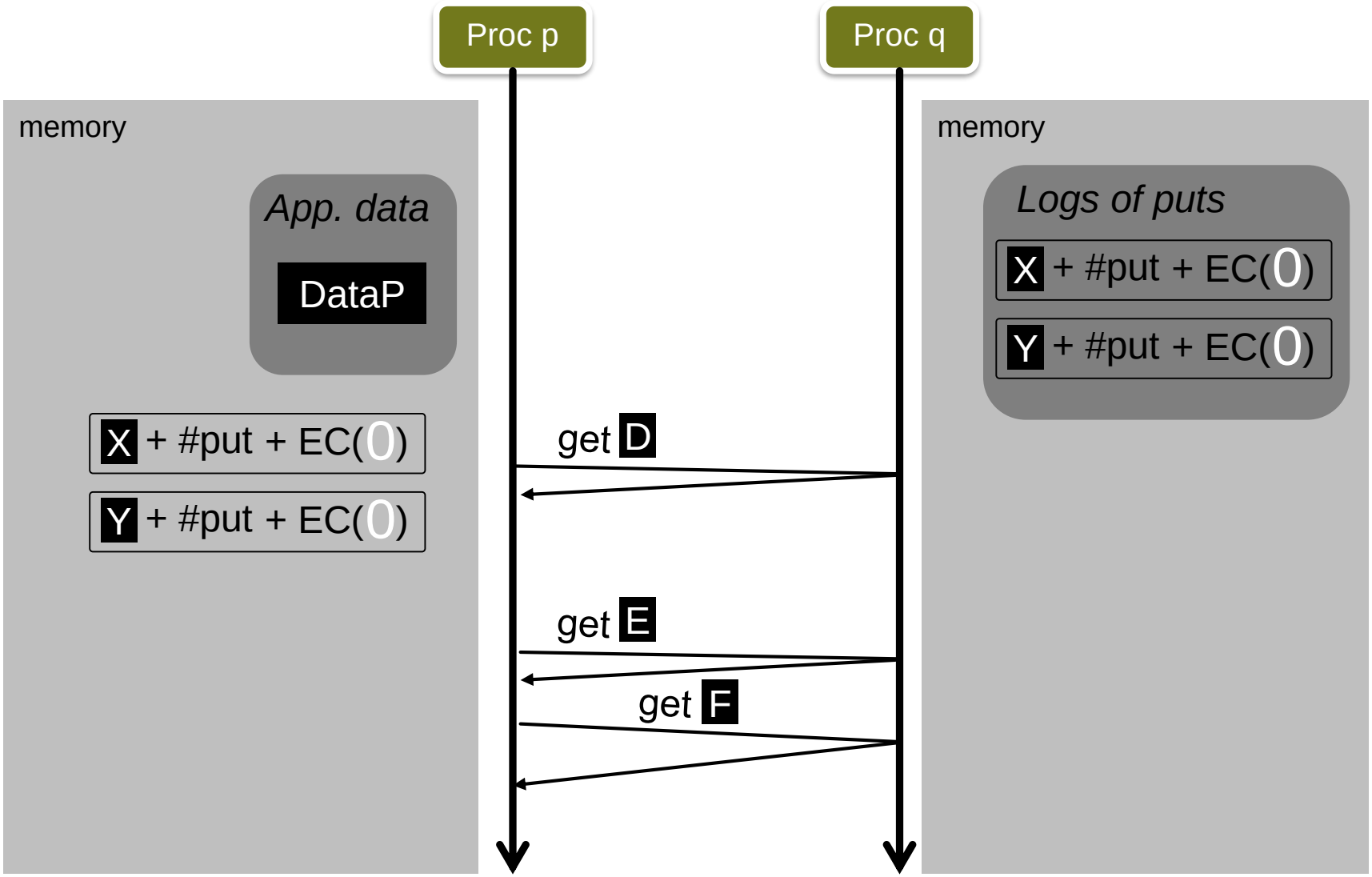

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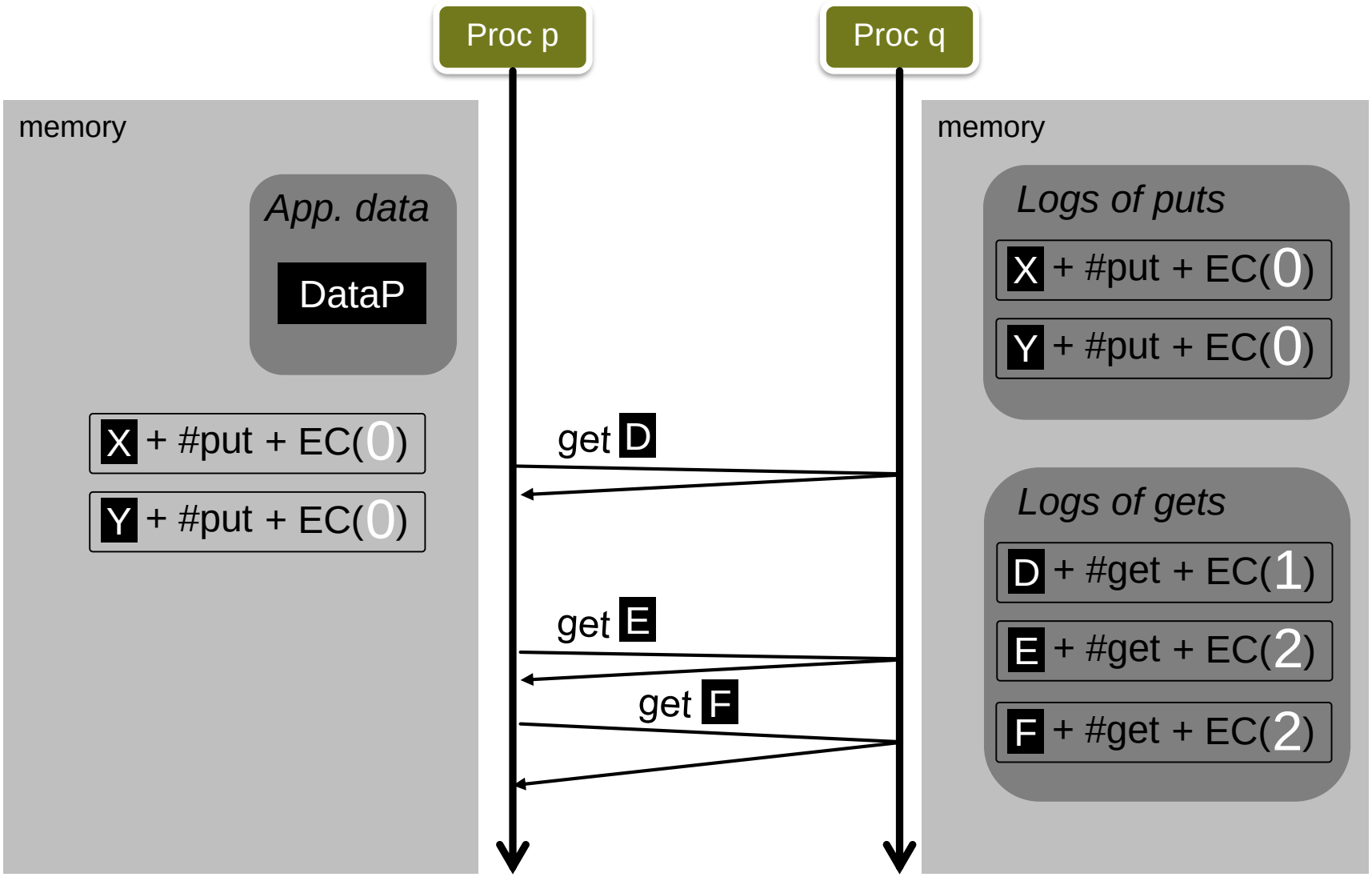

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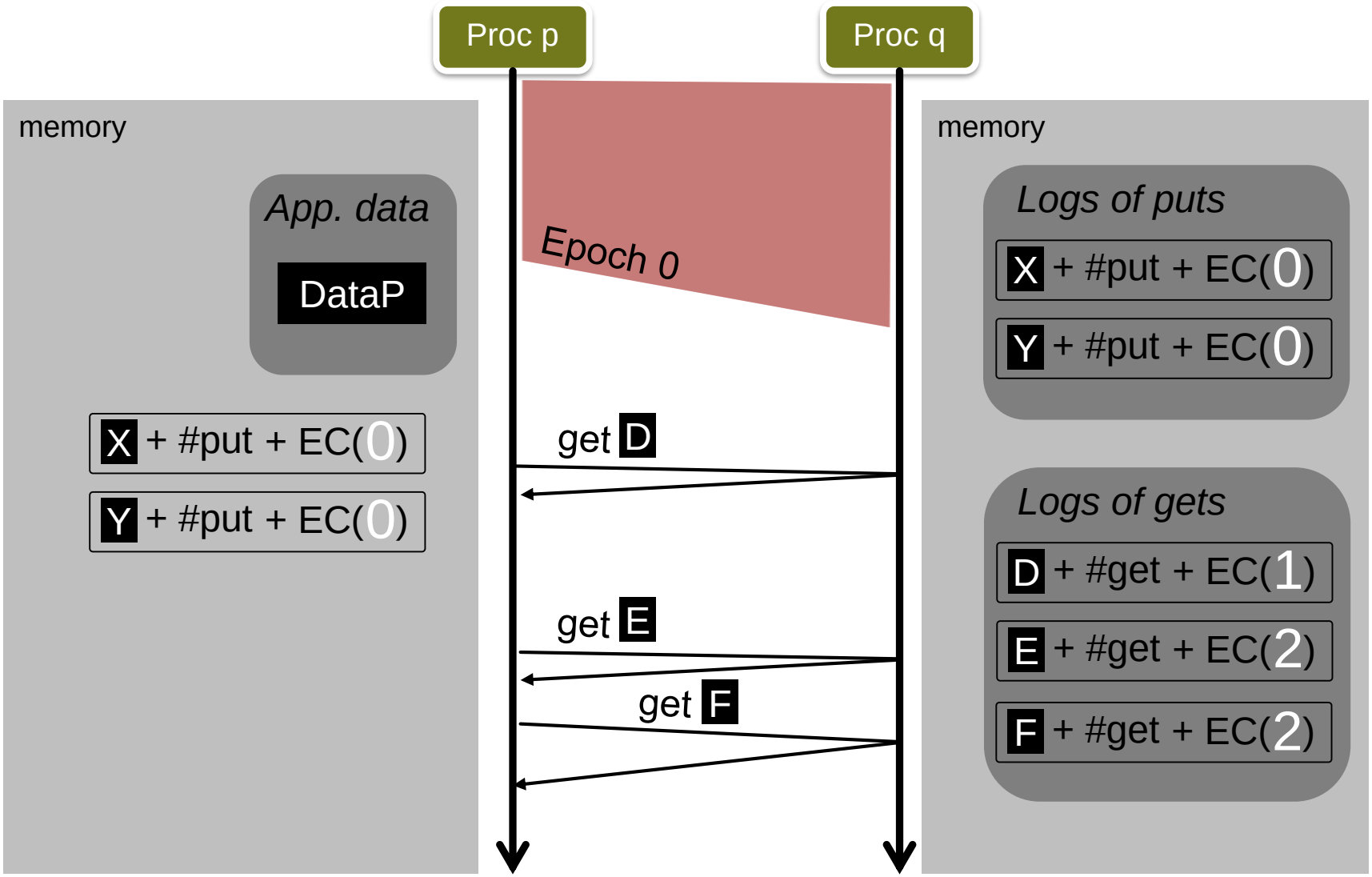

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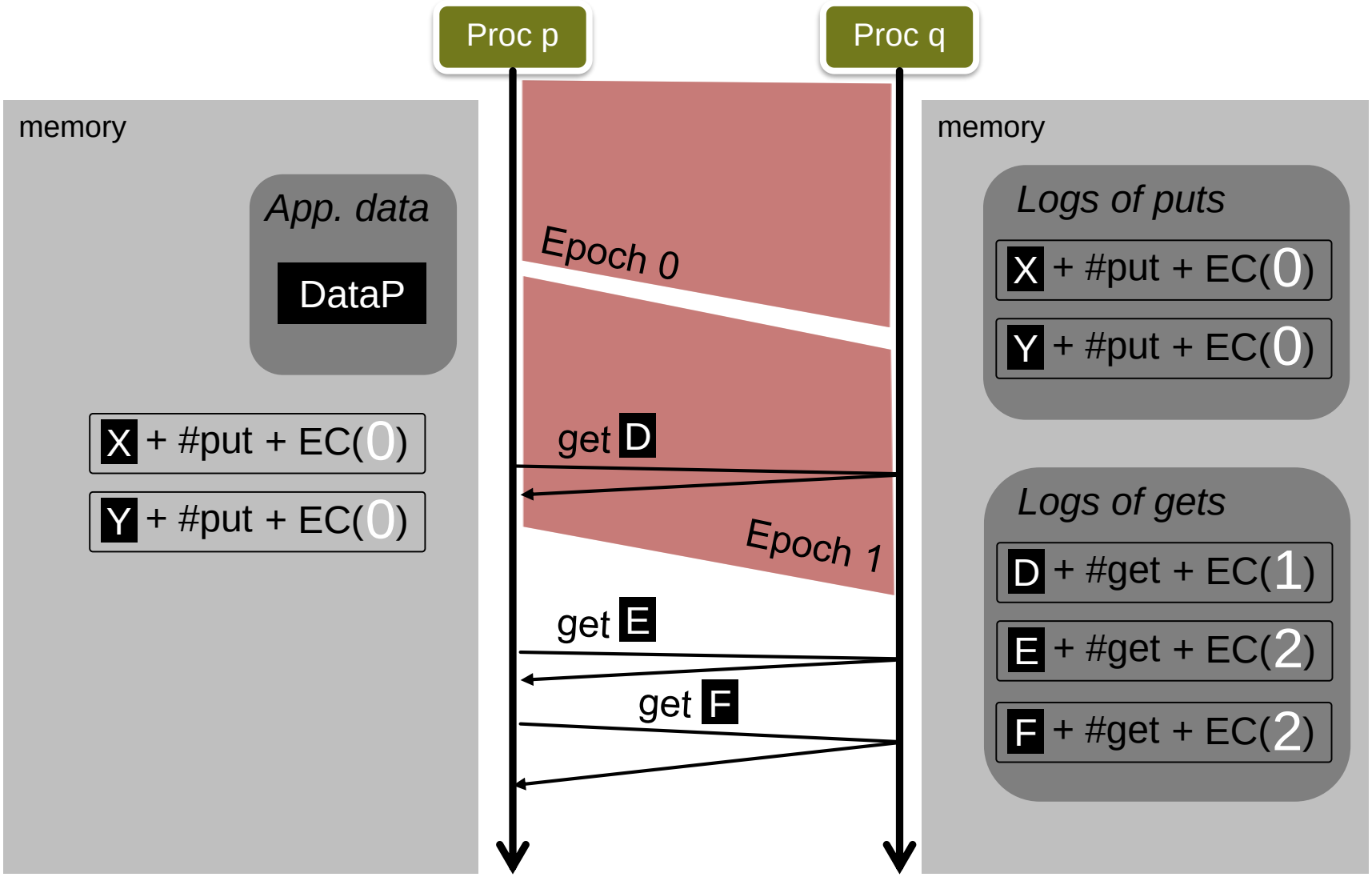

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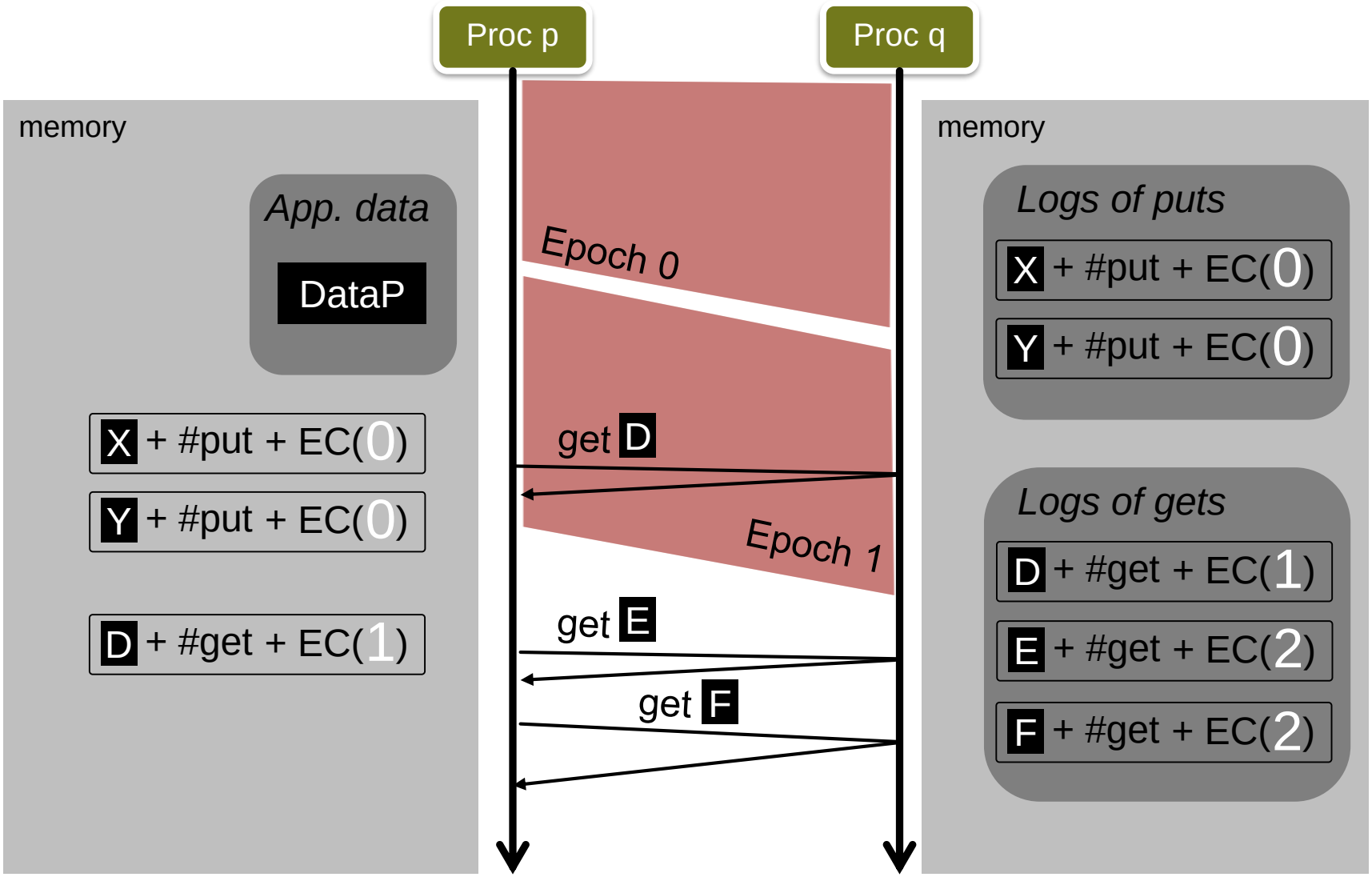

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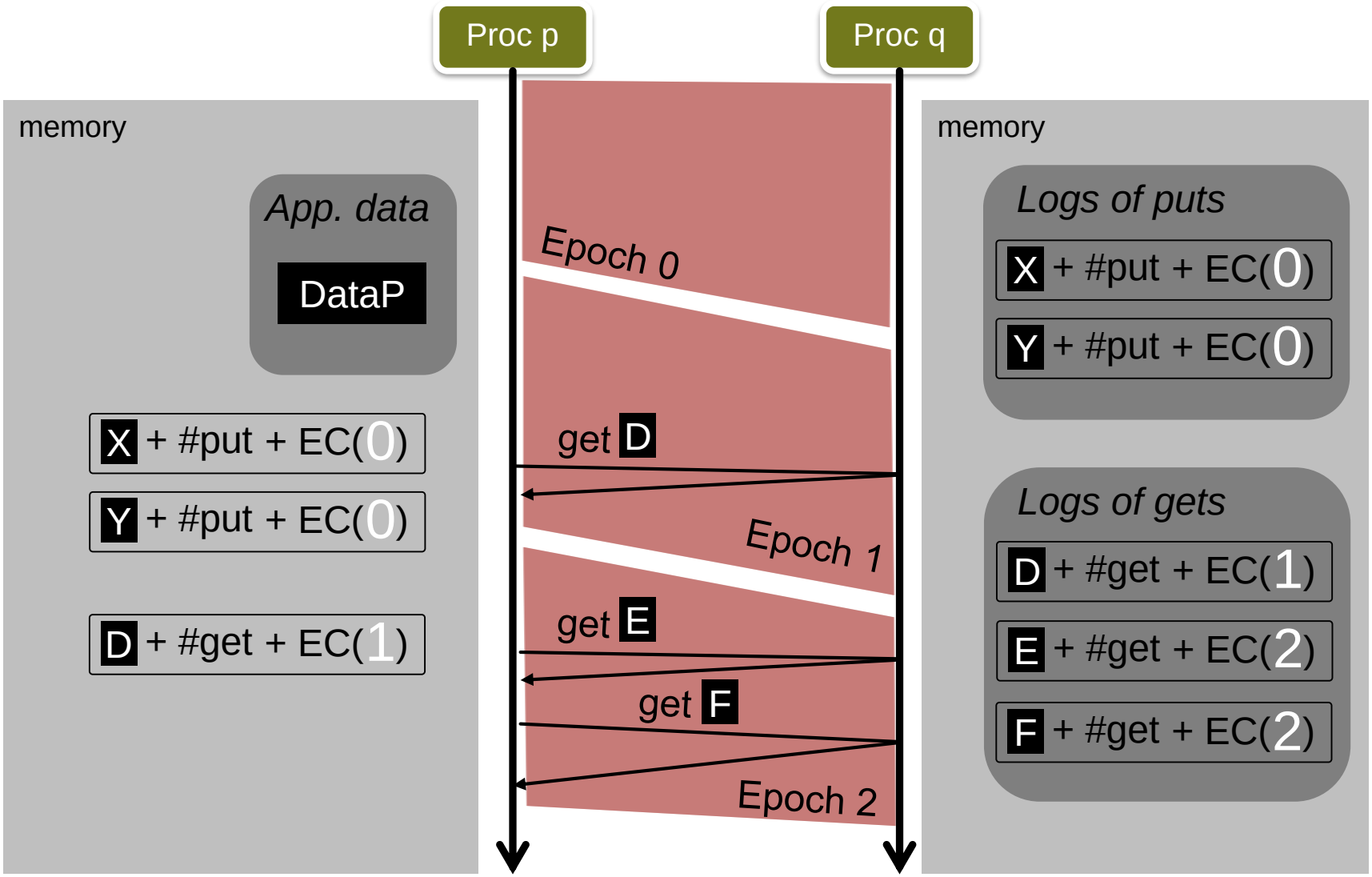

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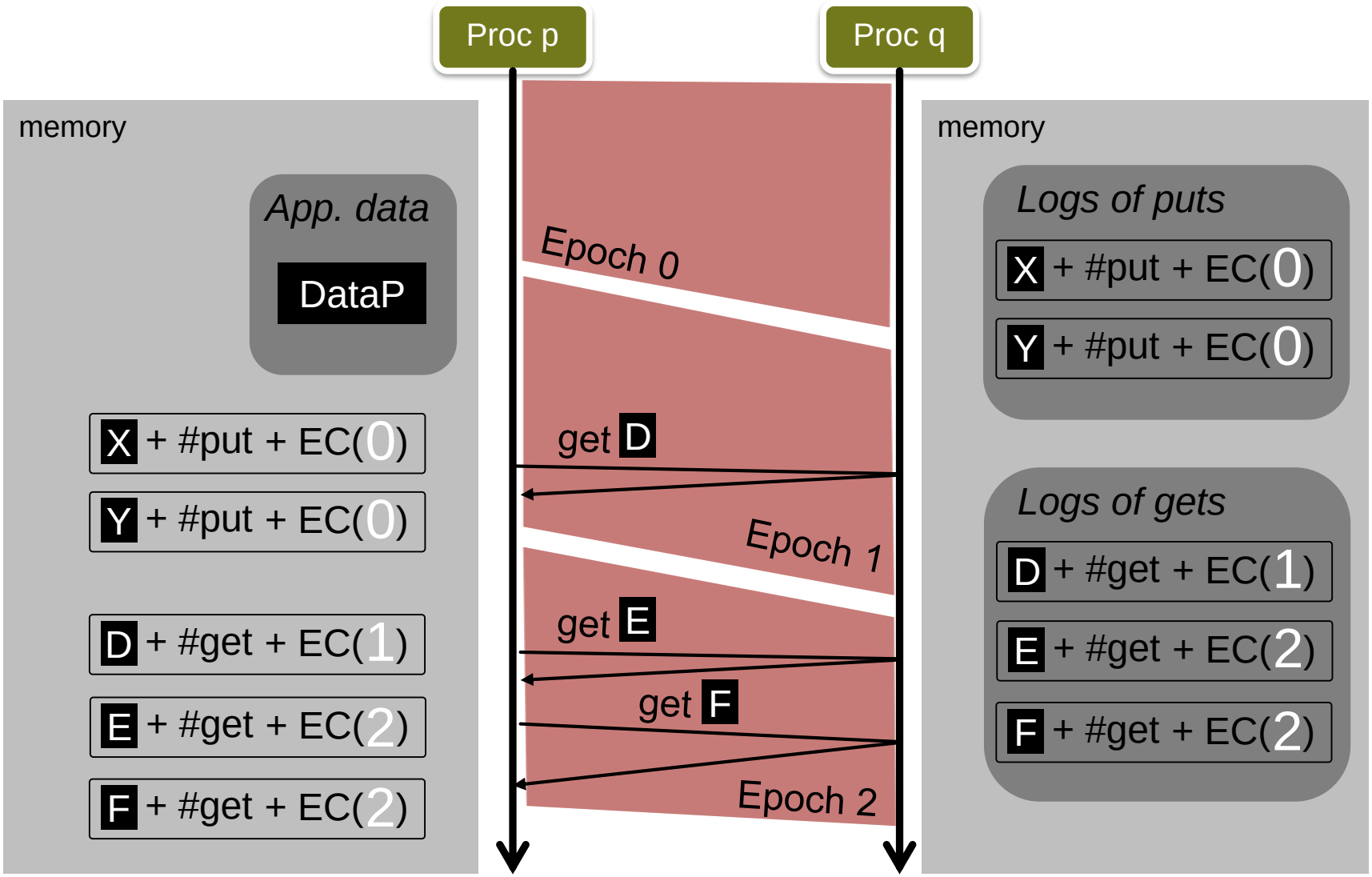

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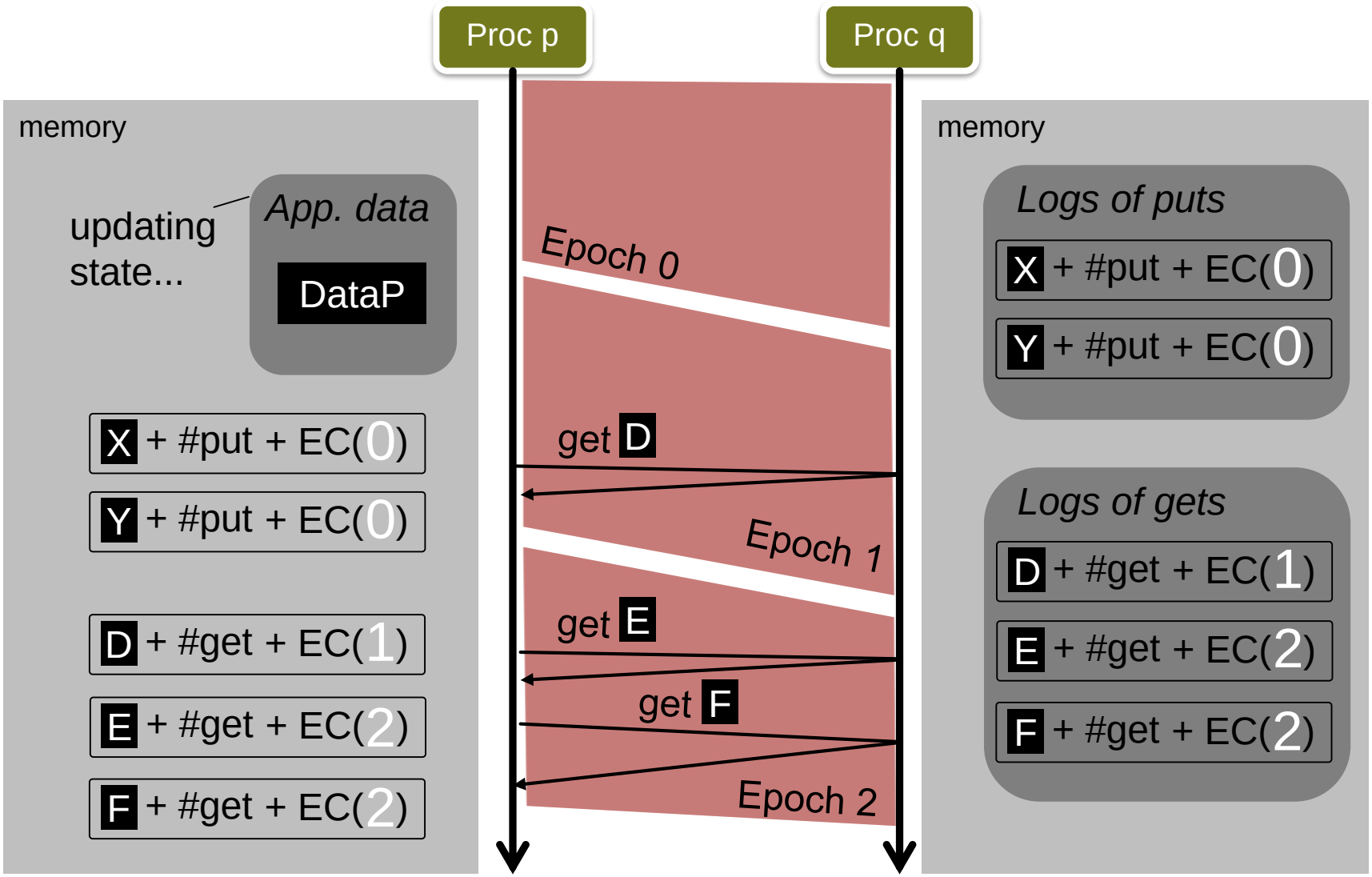

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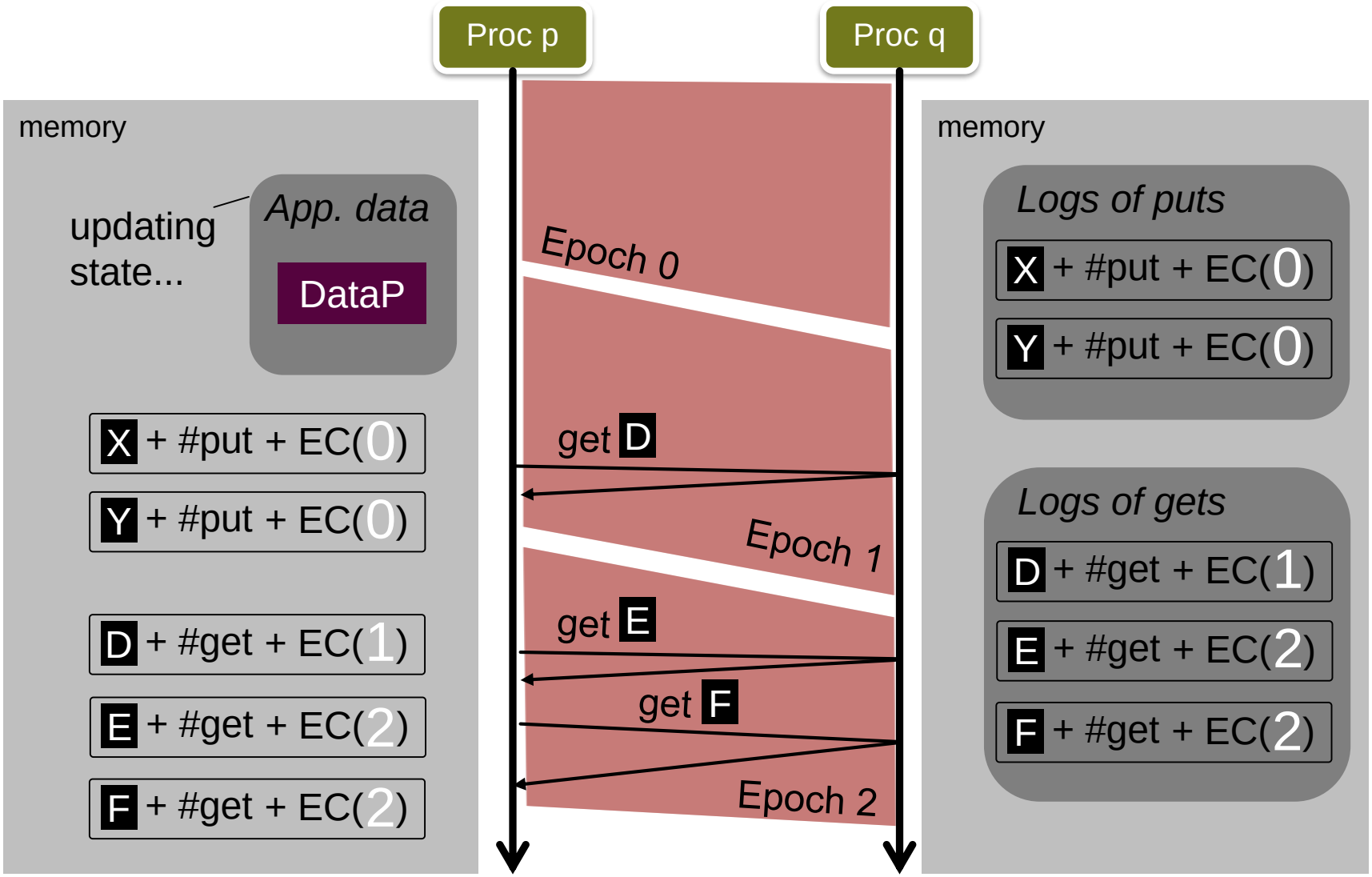

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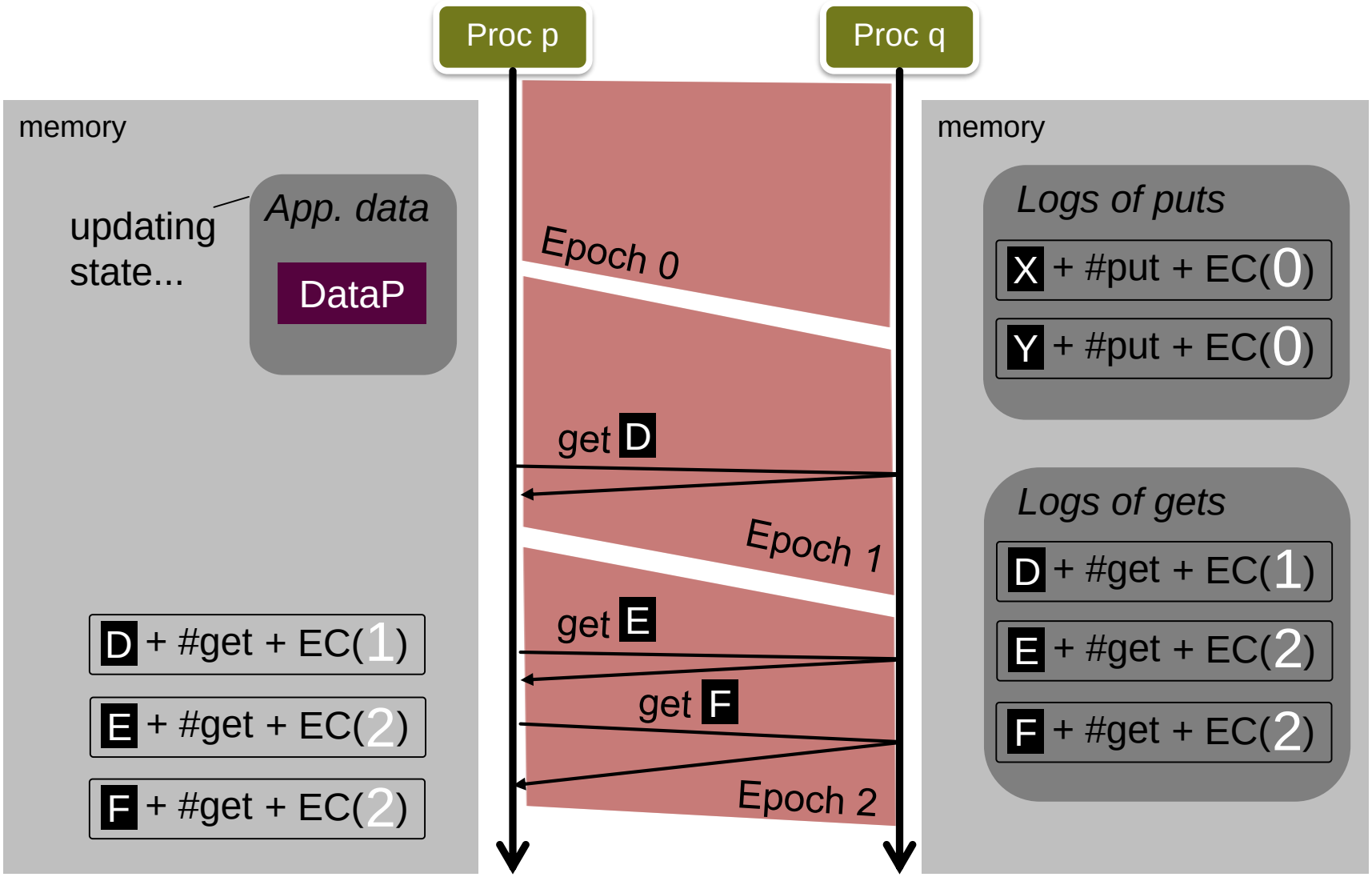

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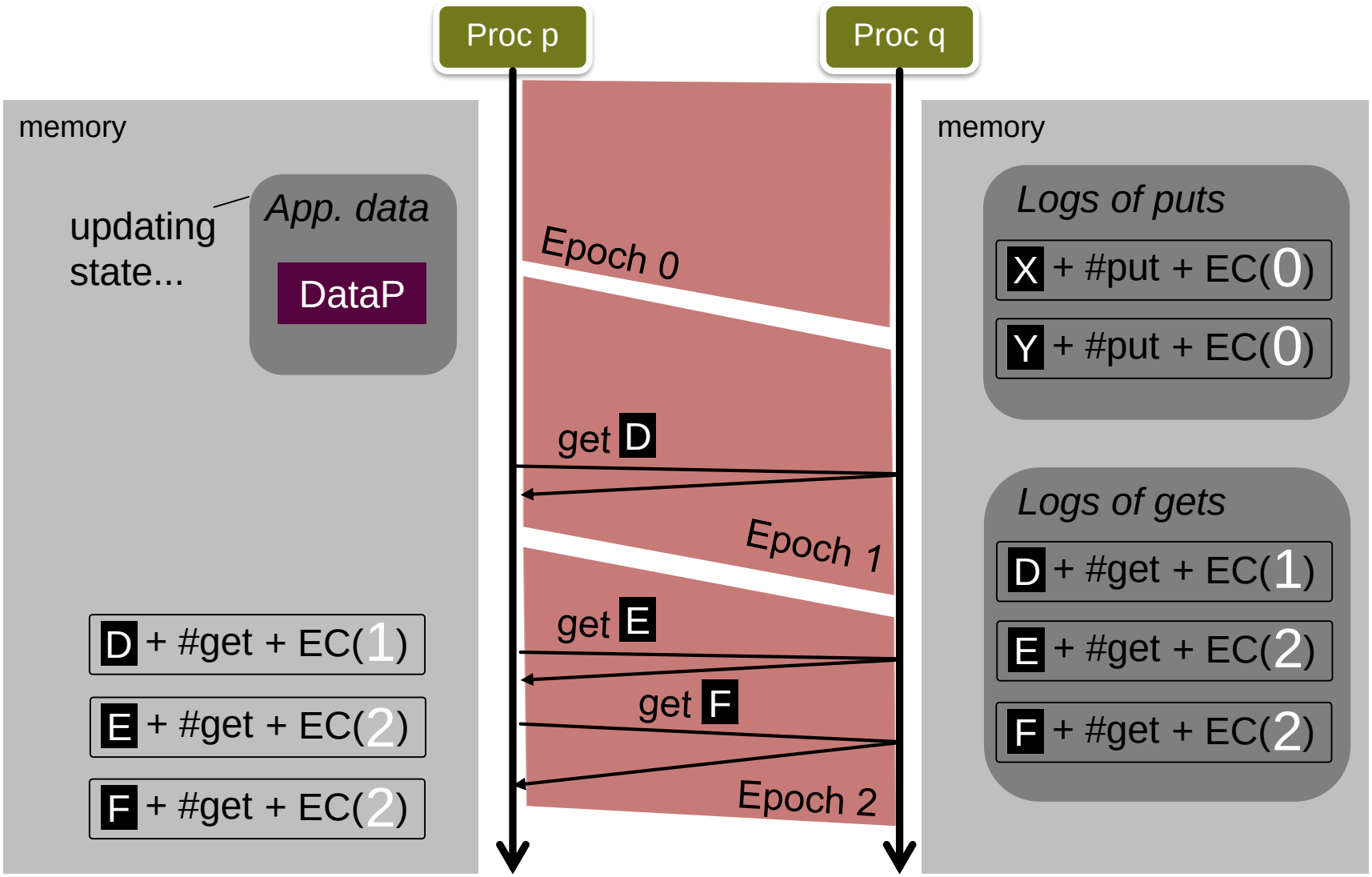

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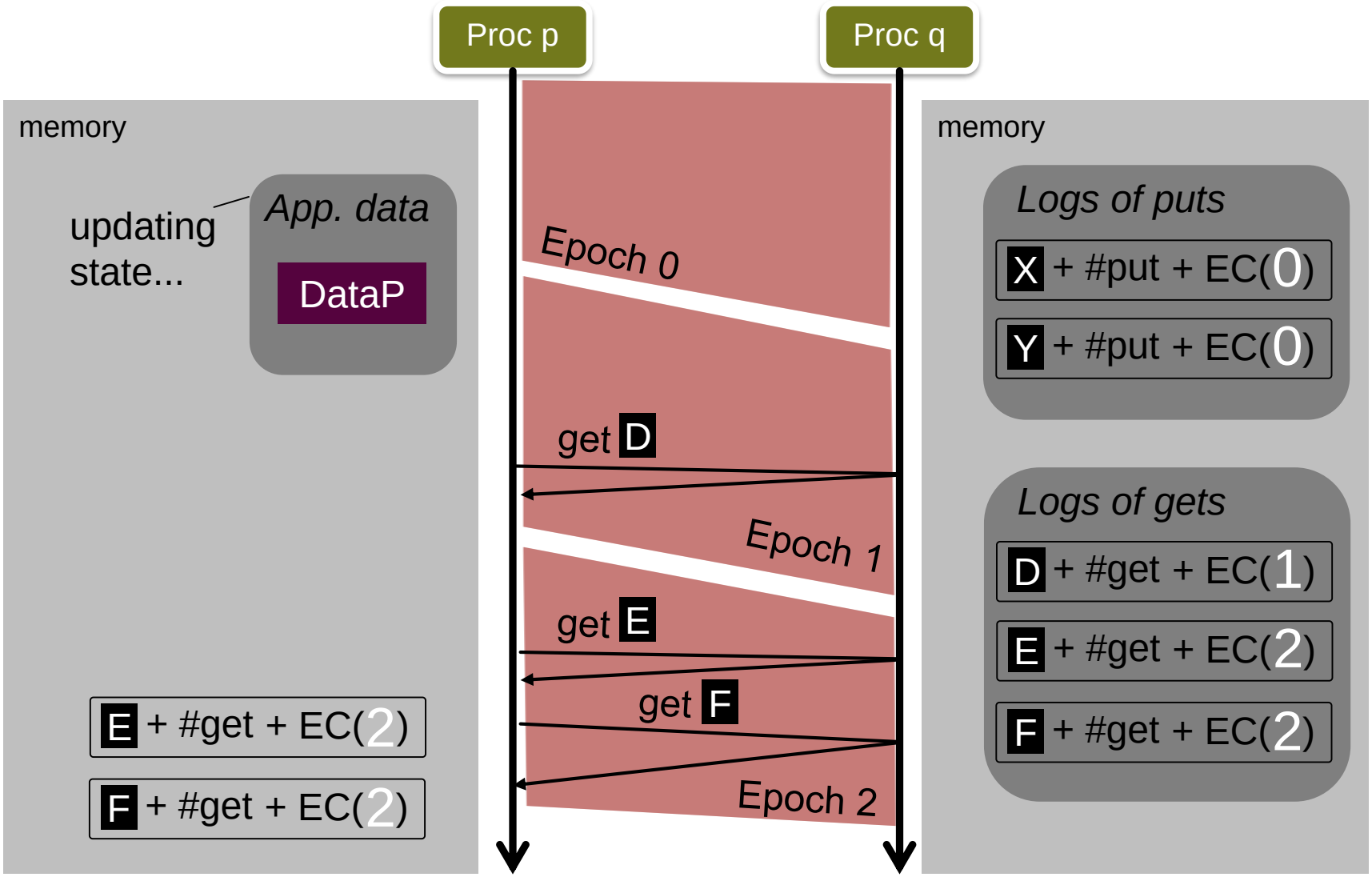

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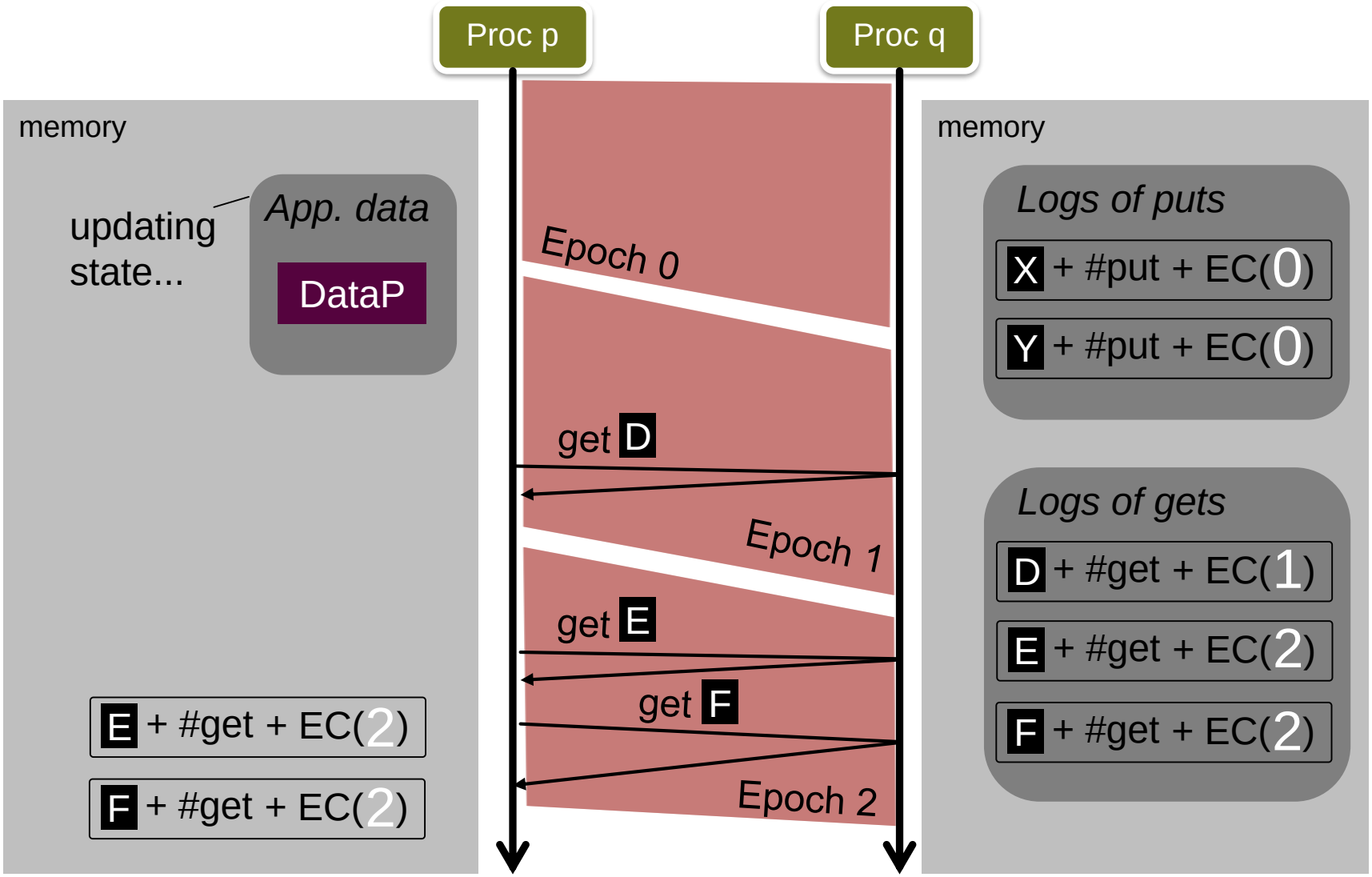

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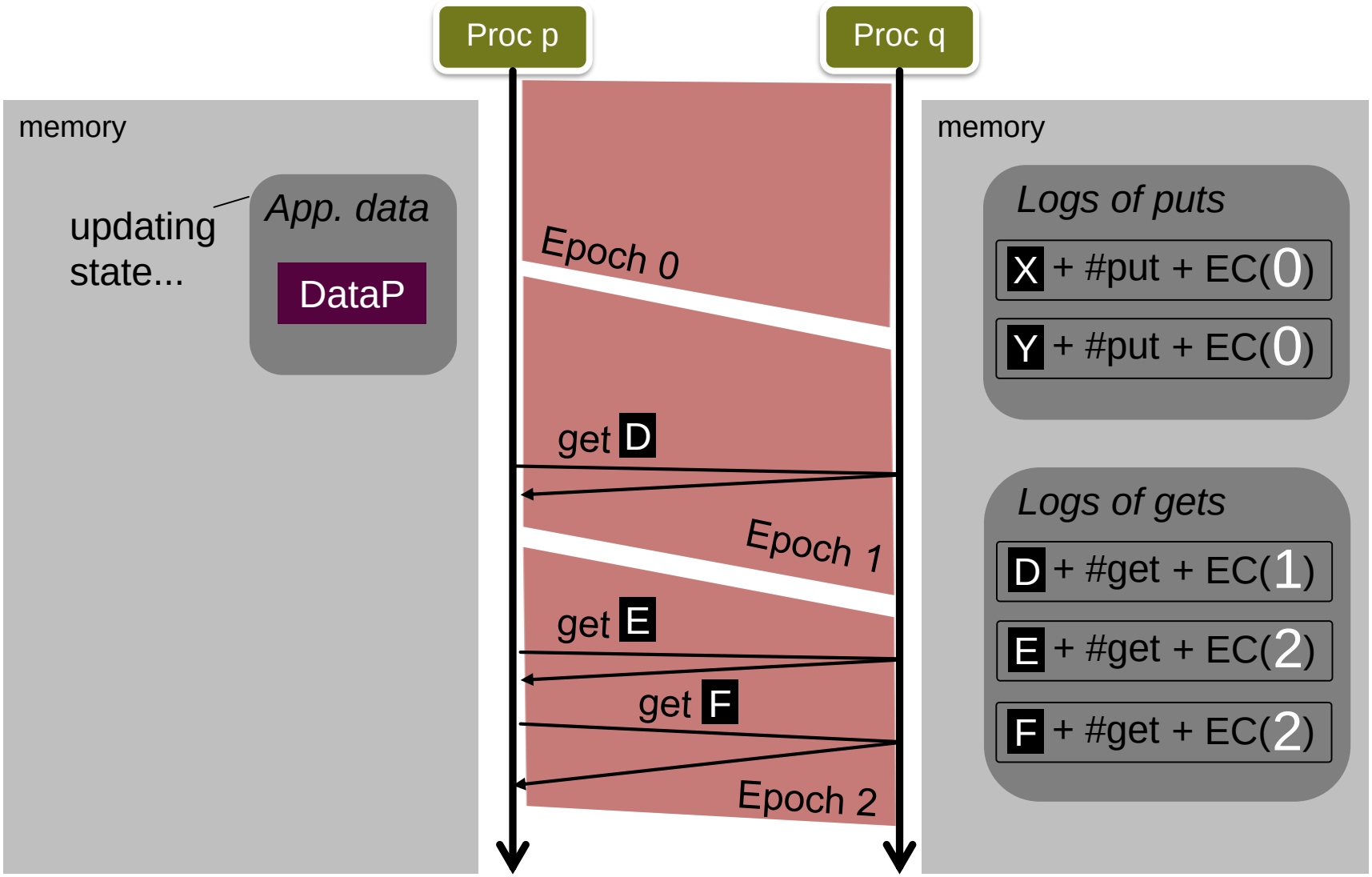

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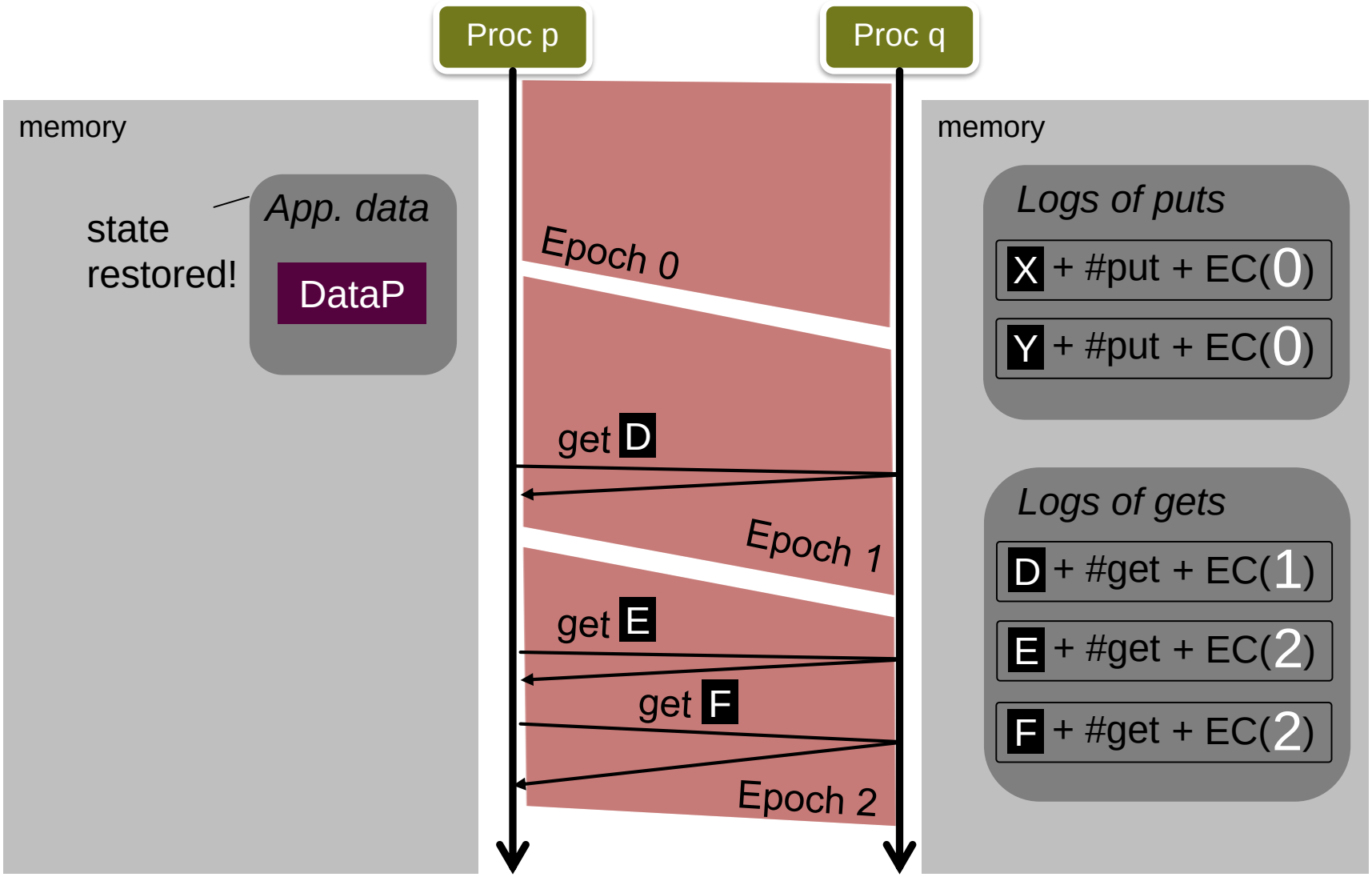

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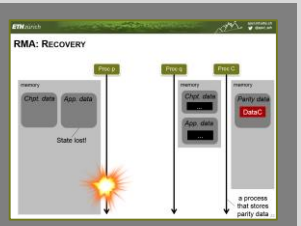

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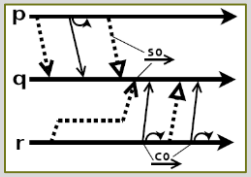

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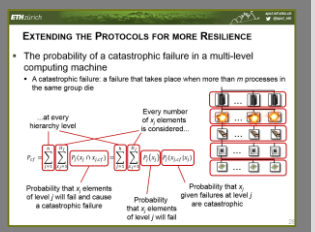

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A Cray XE/XT supercomputer

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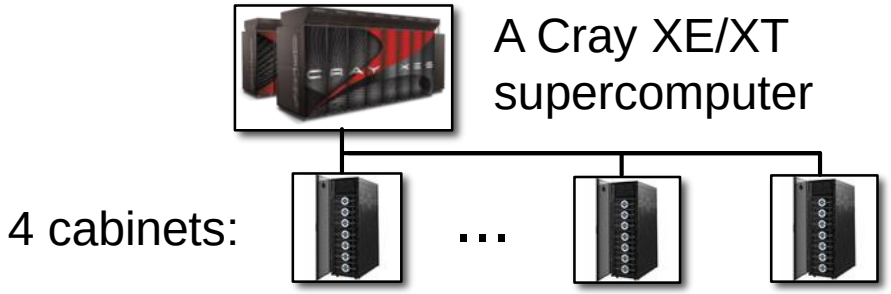

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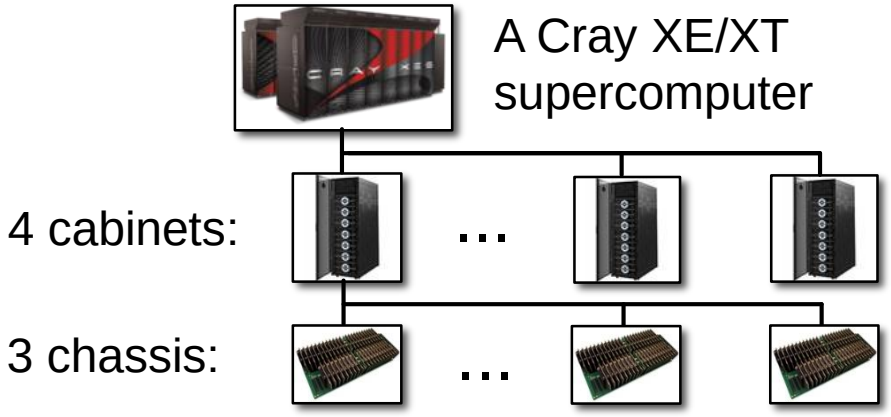

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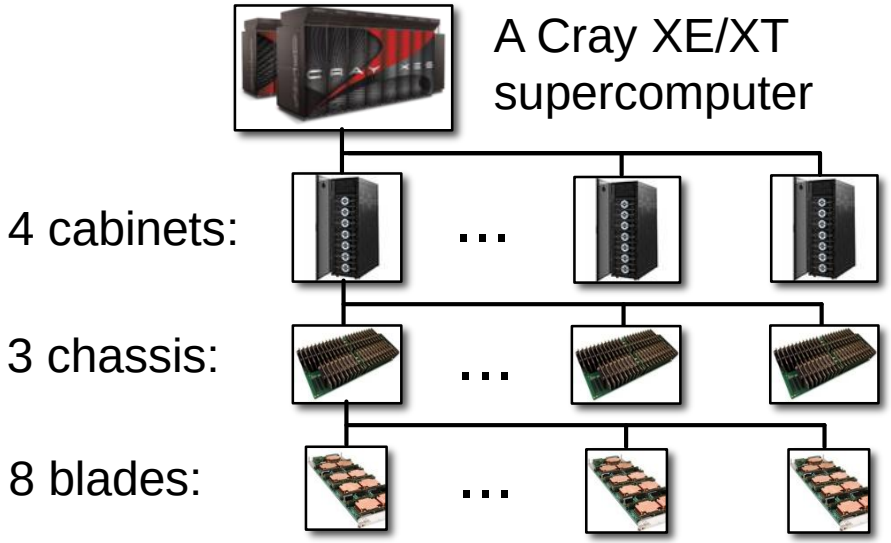

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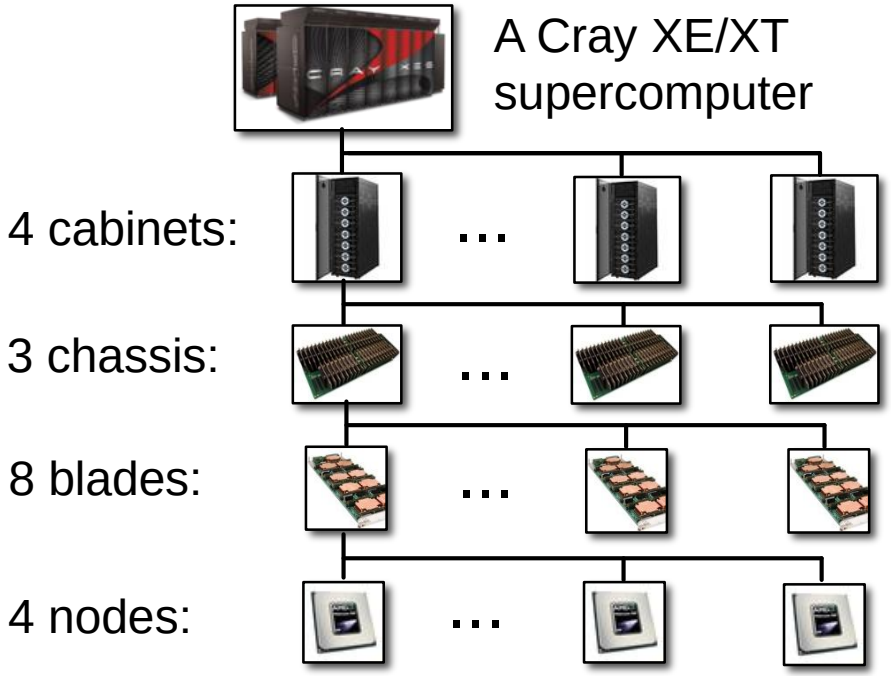

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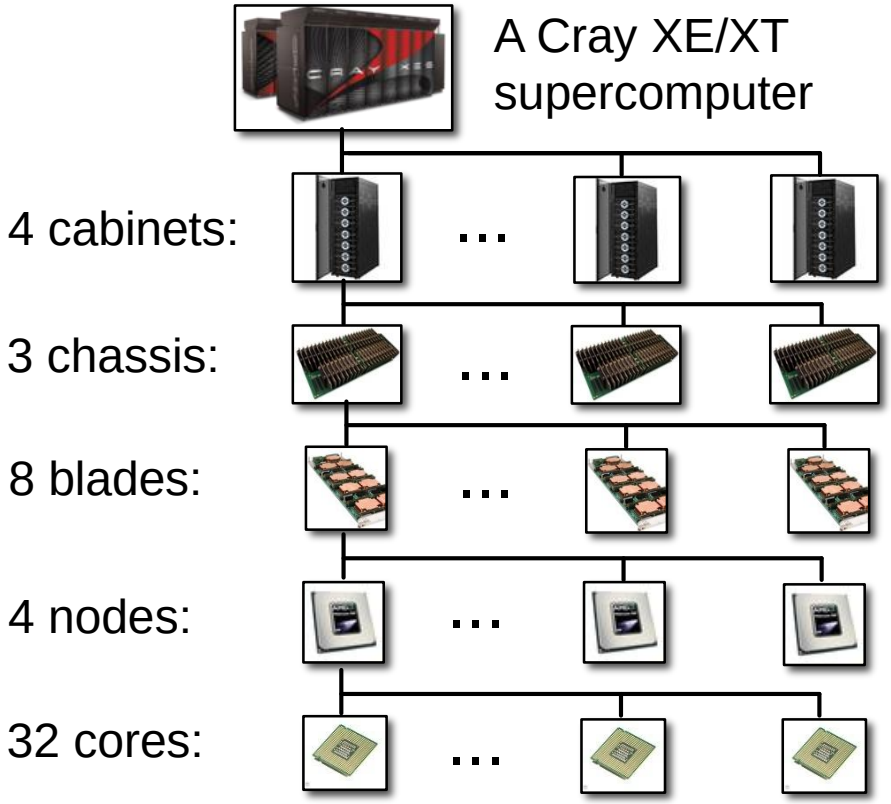

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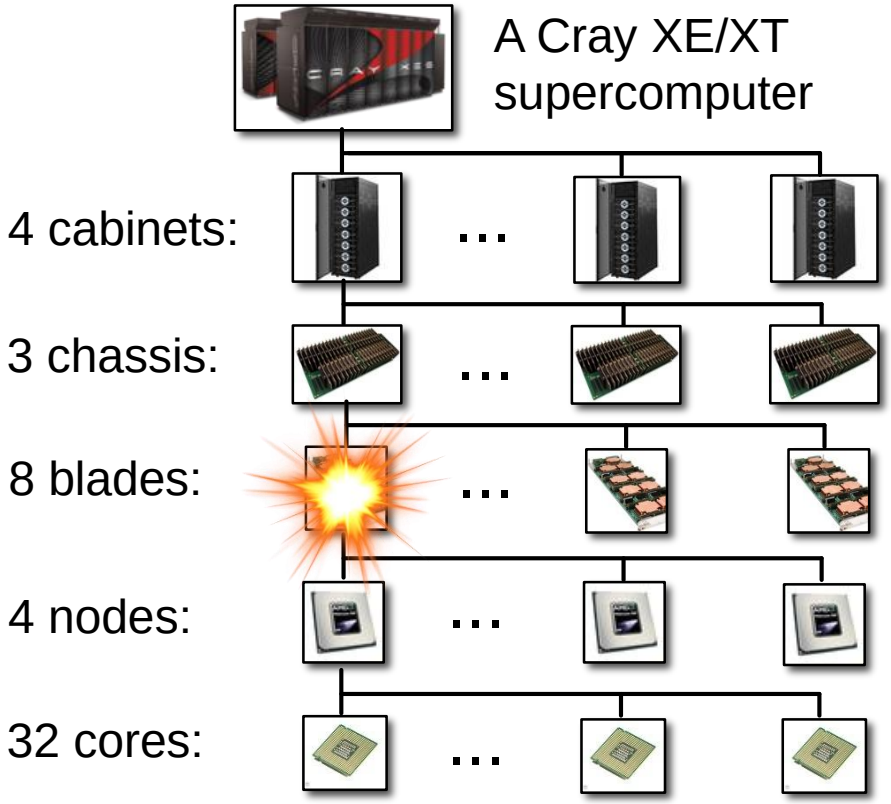

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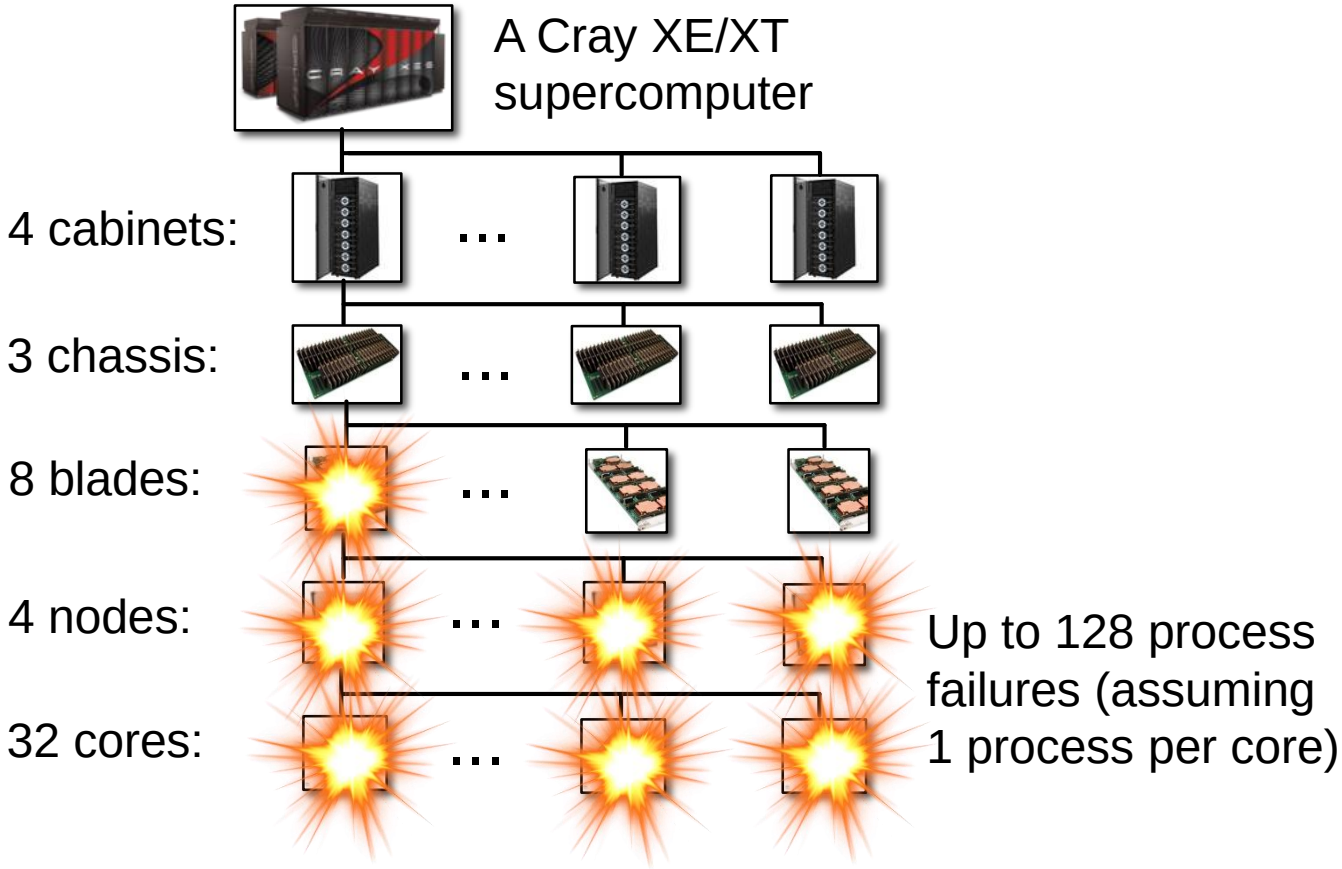

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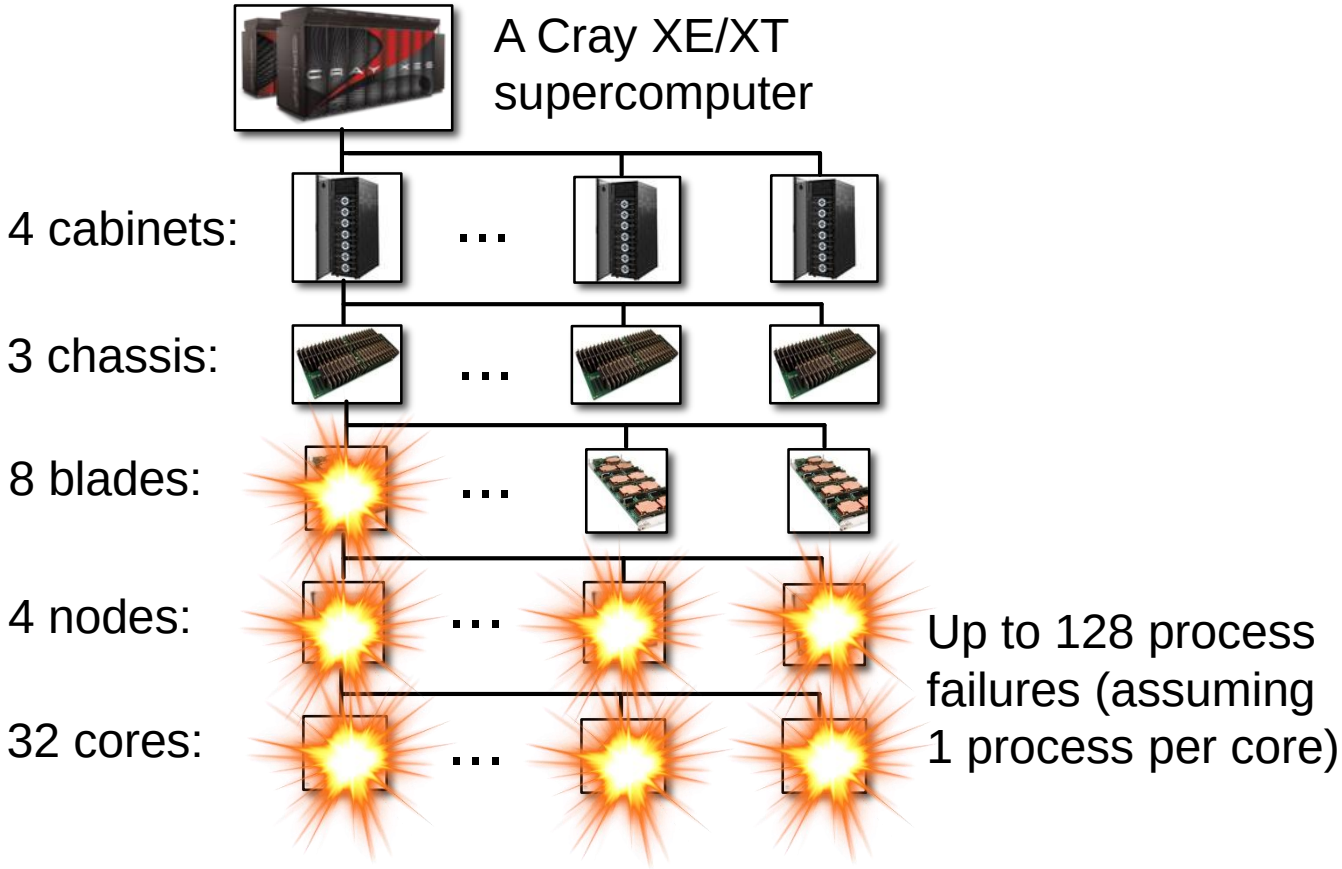

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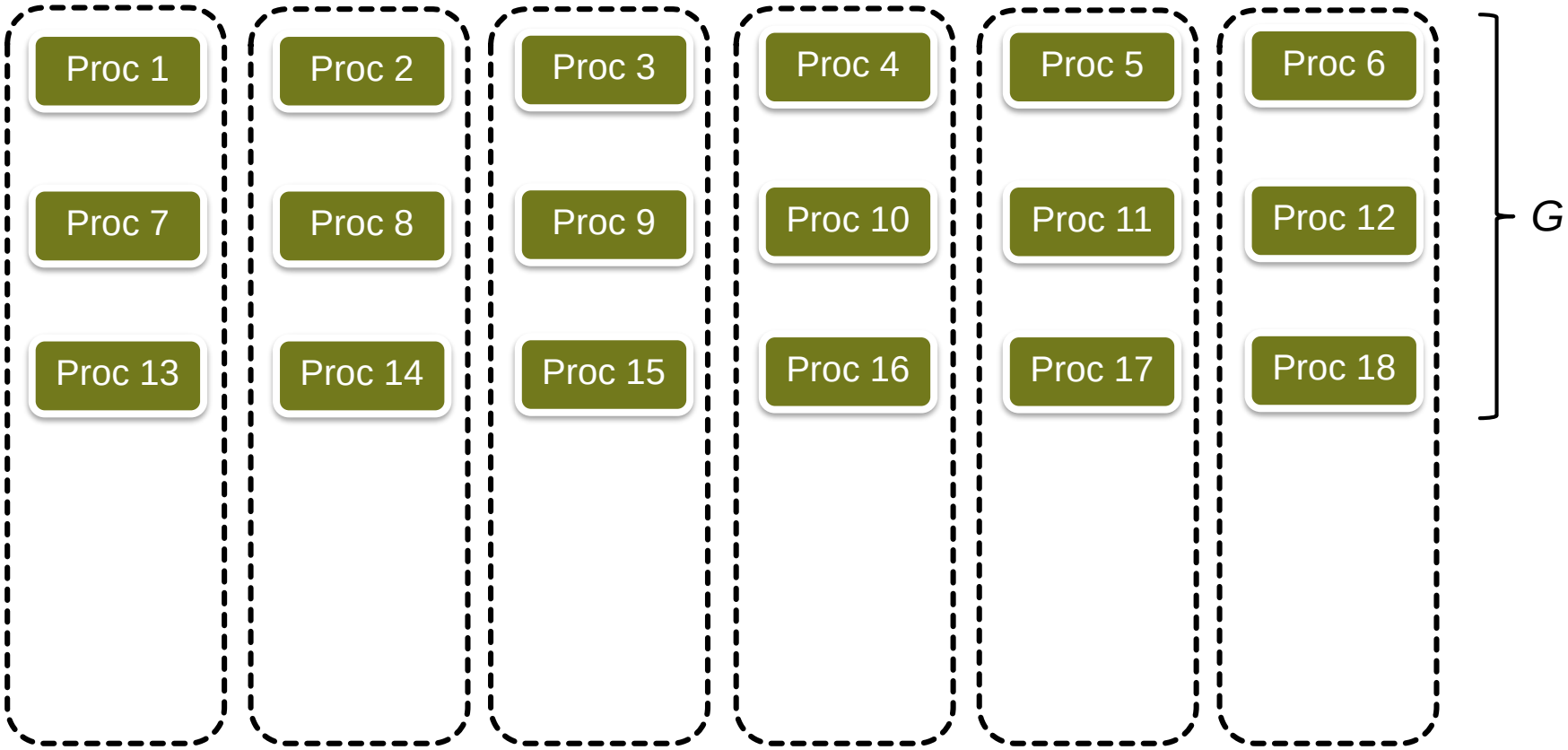

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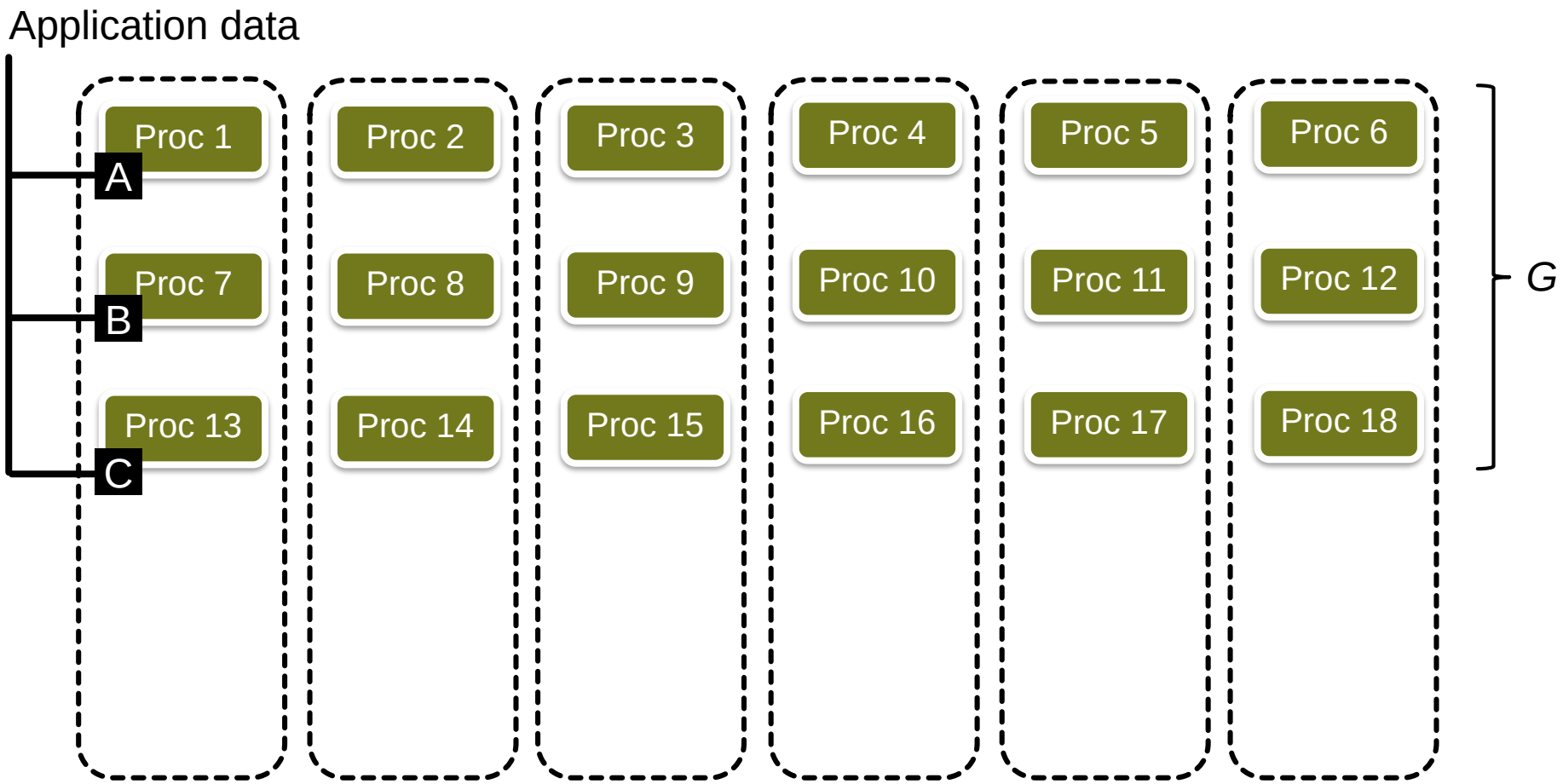

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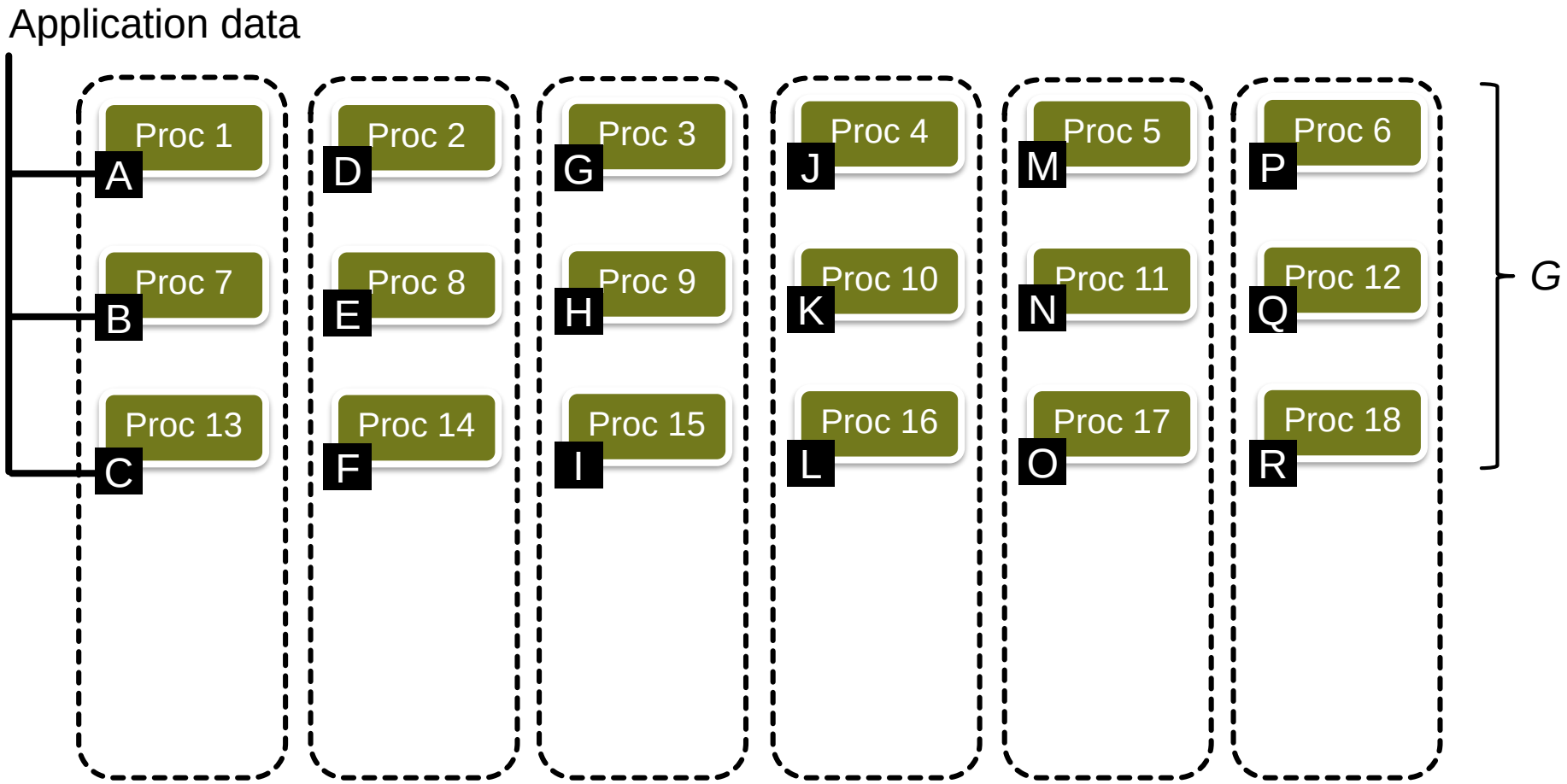

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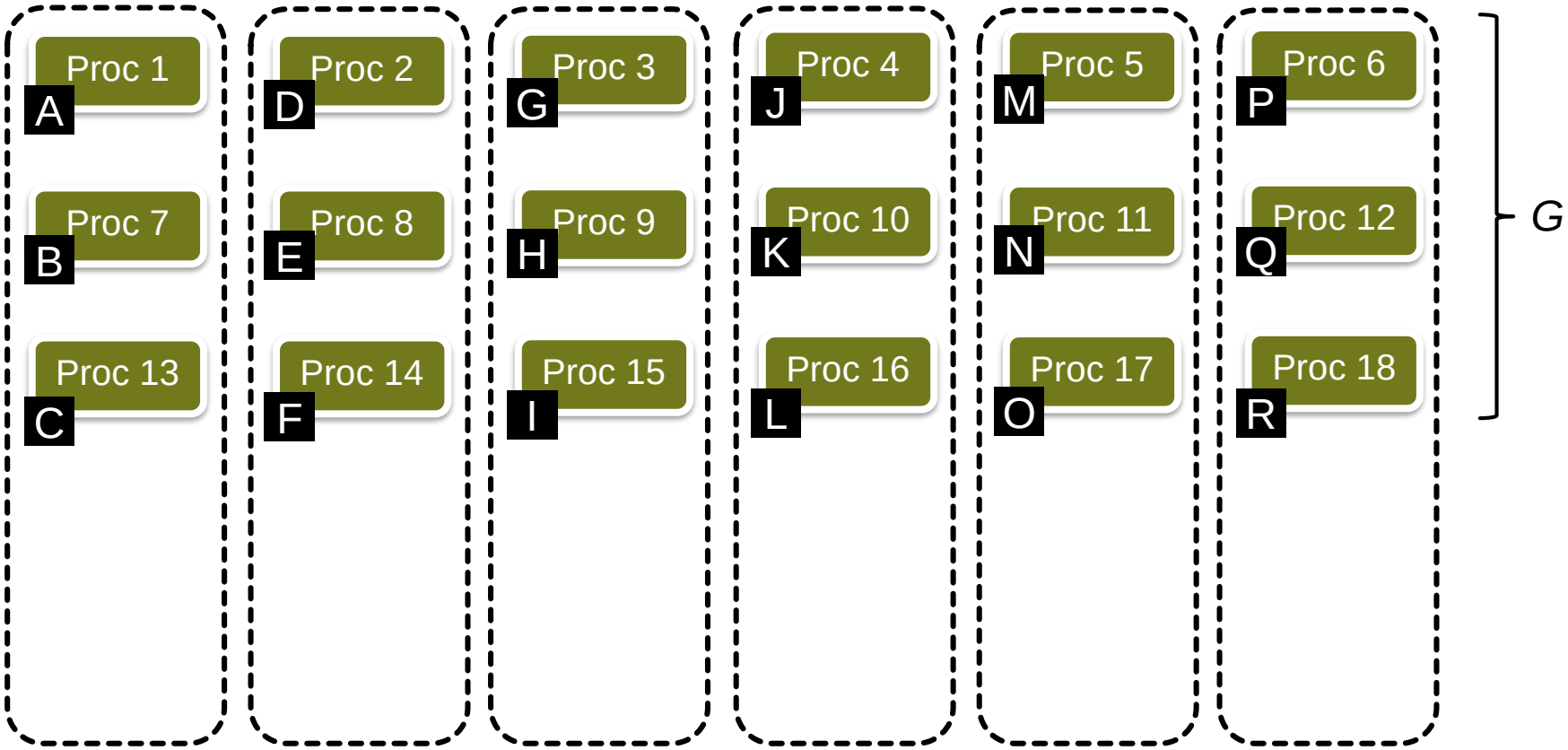

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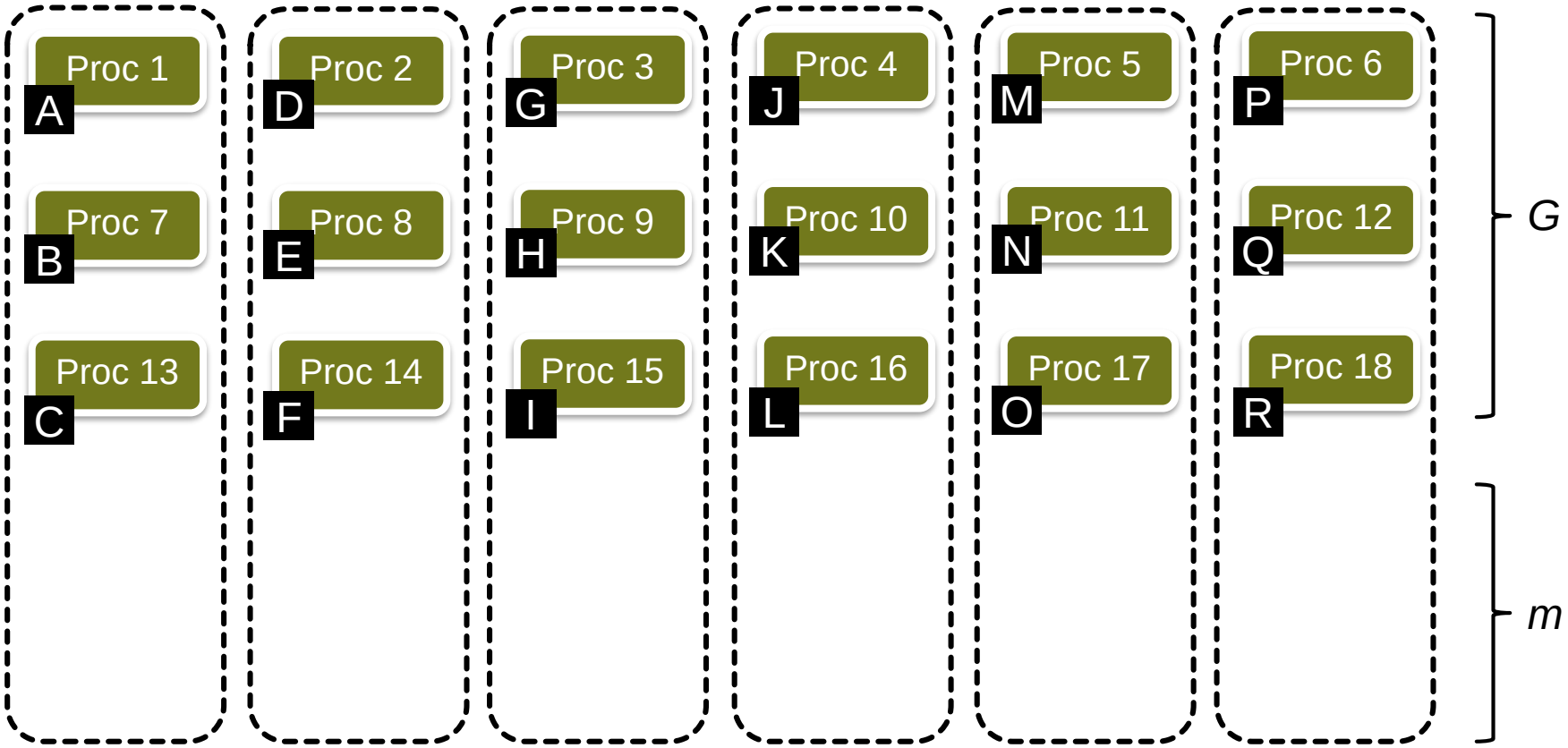

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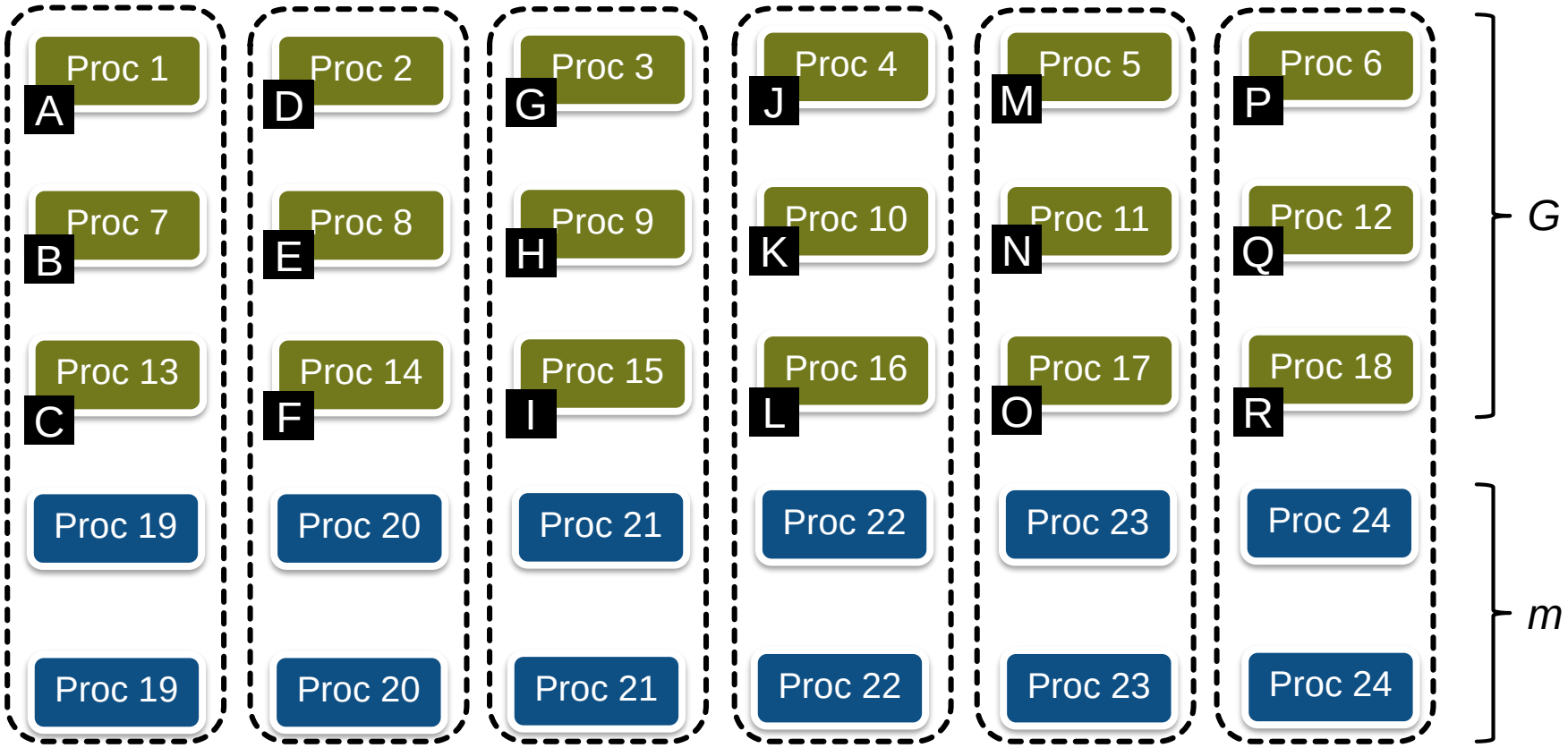

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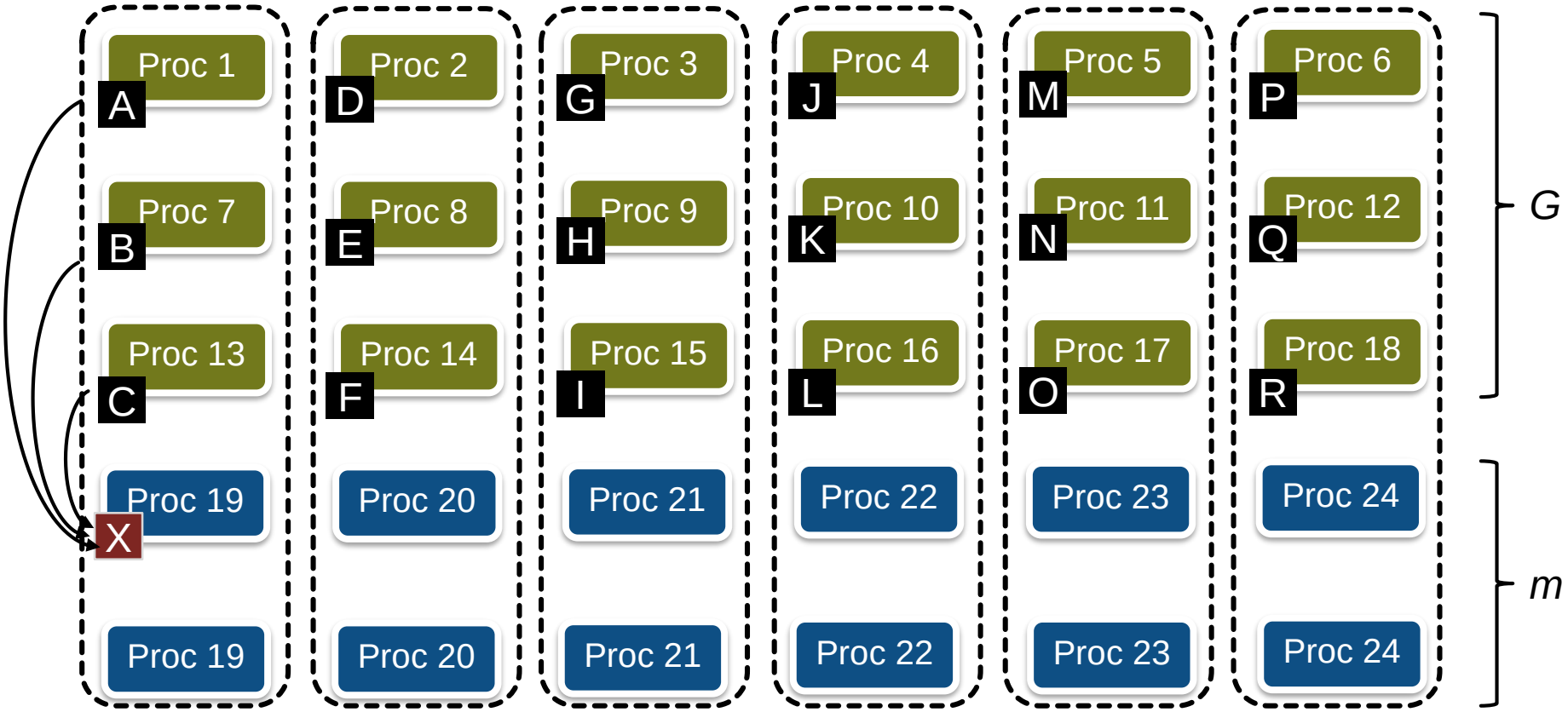

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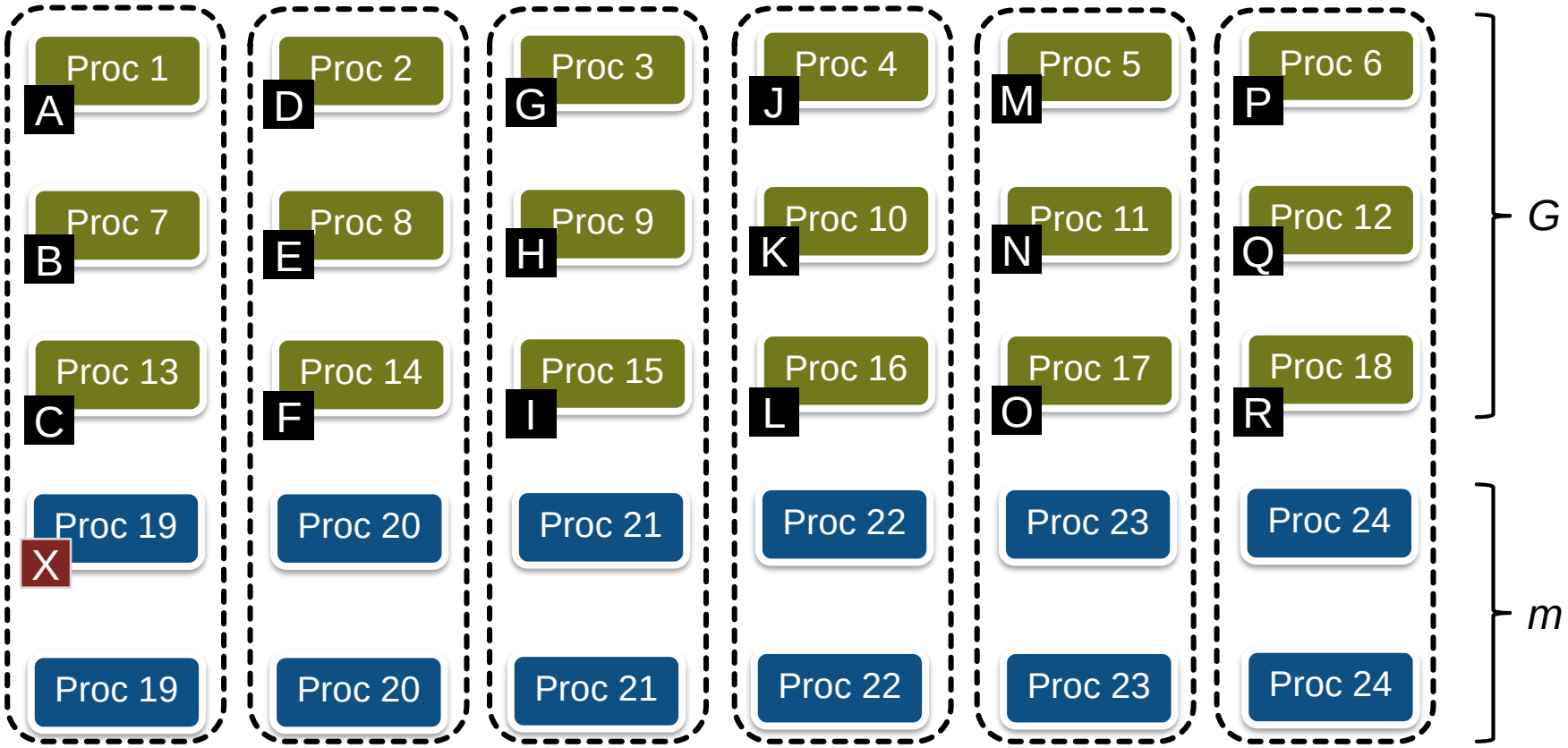

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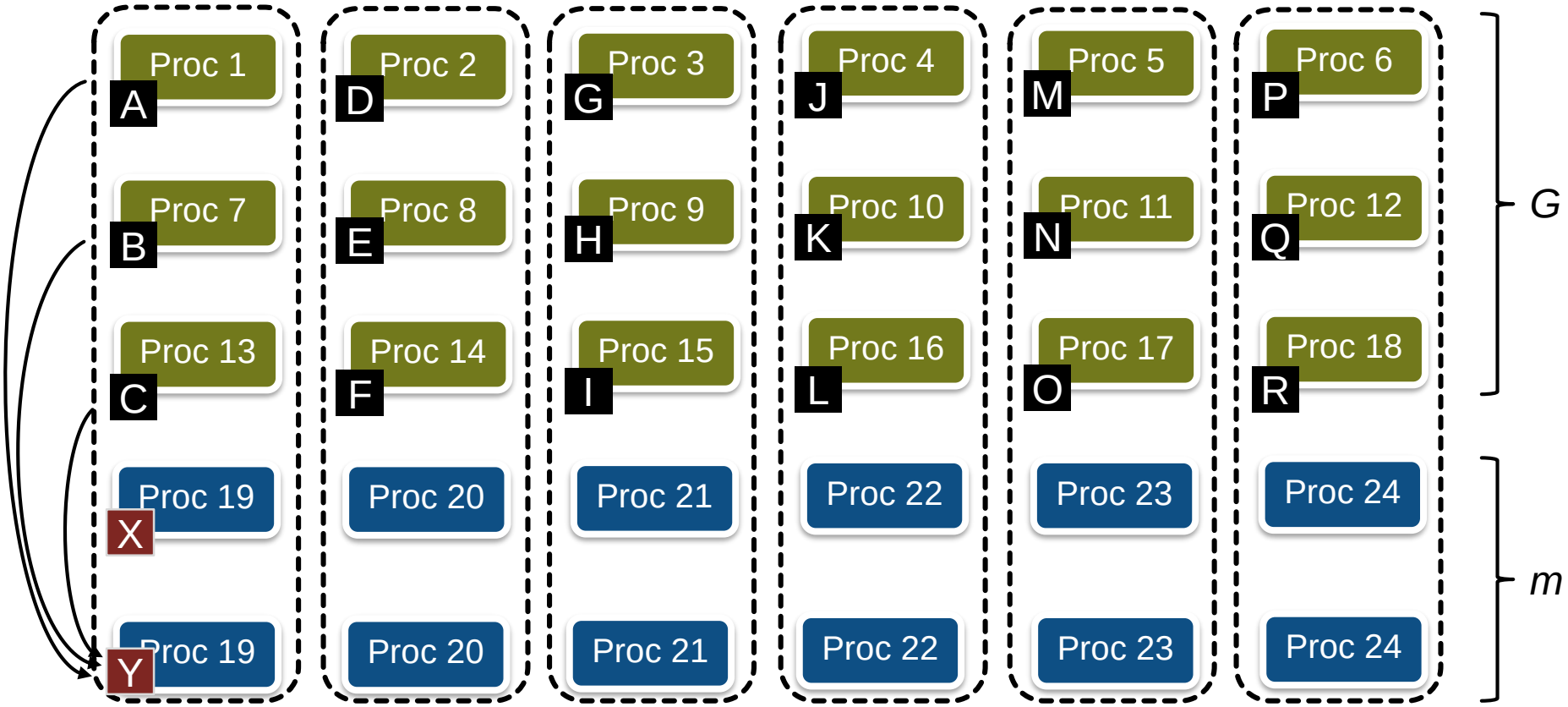

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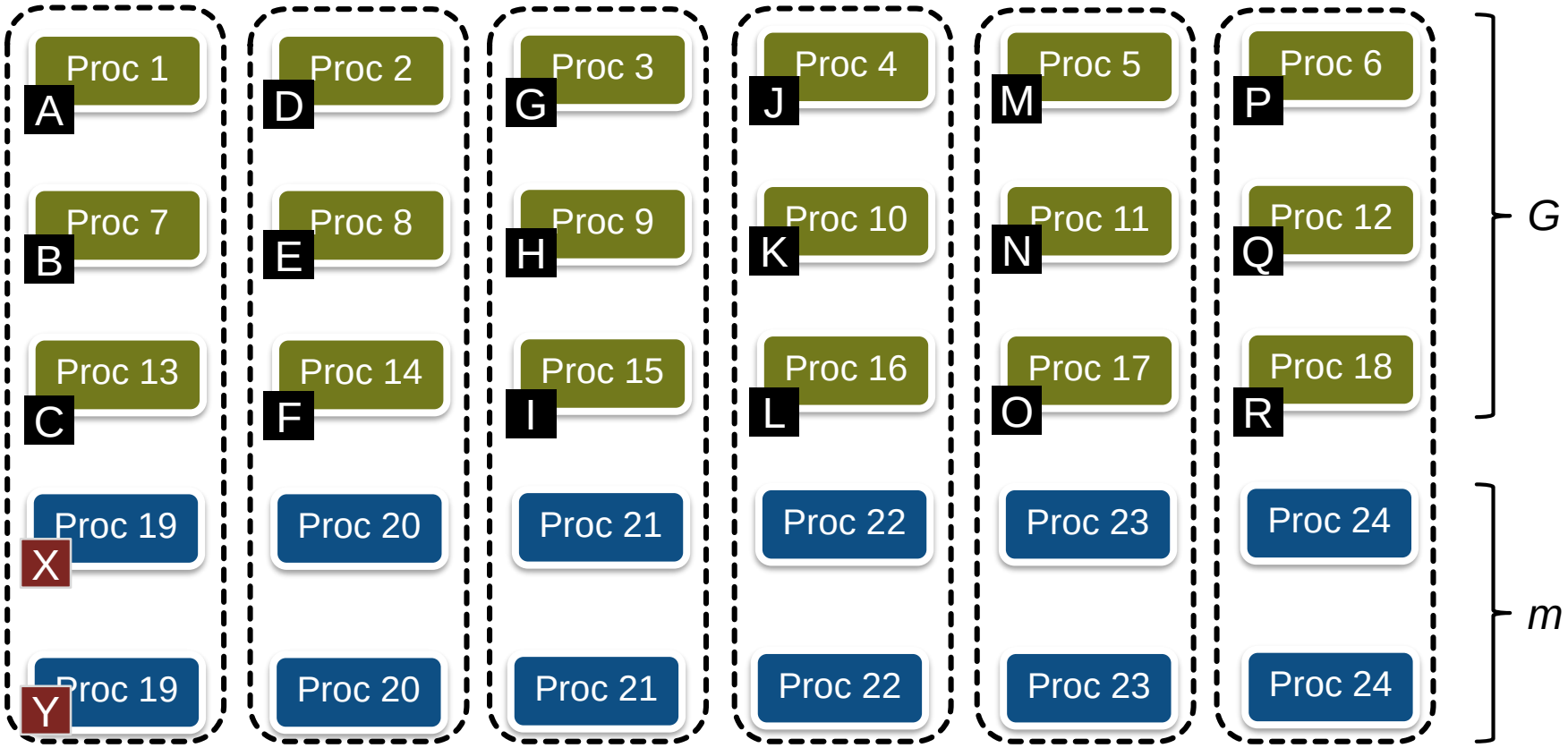

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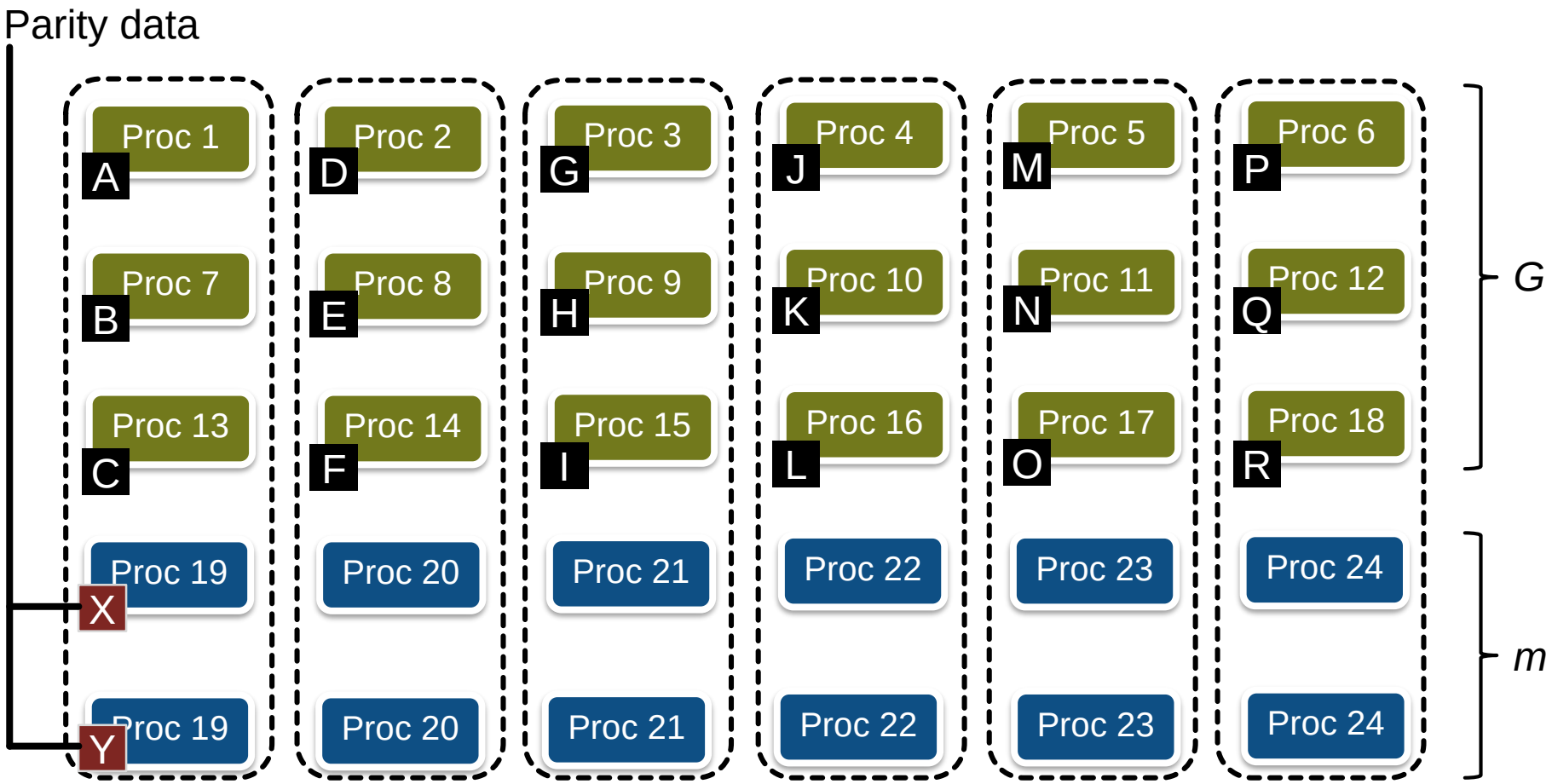

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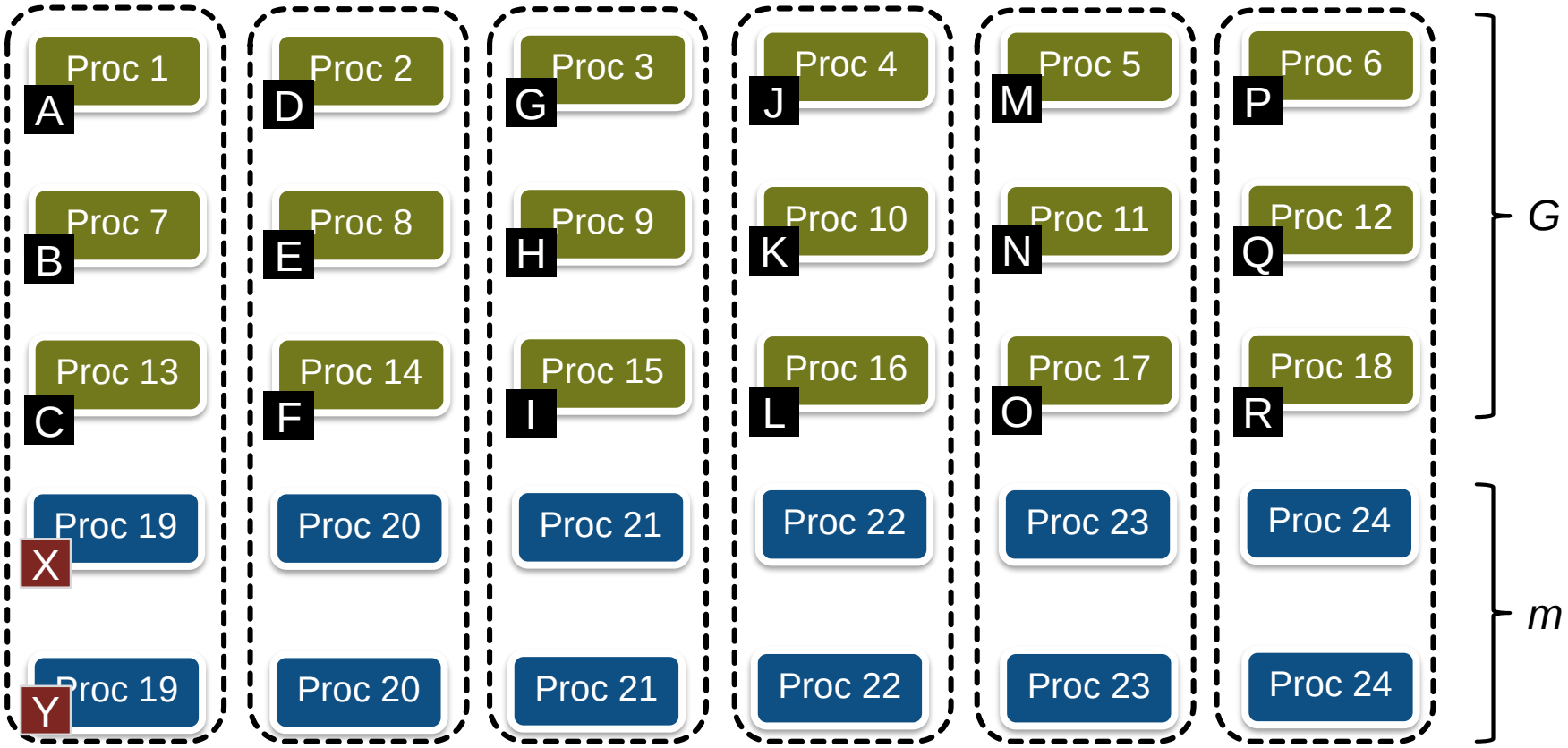

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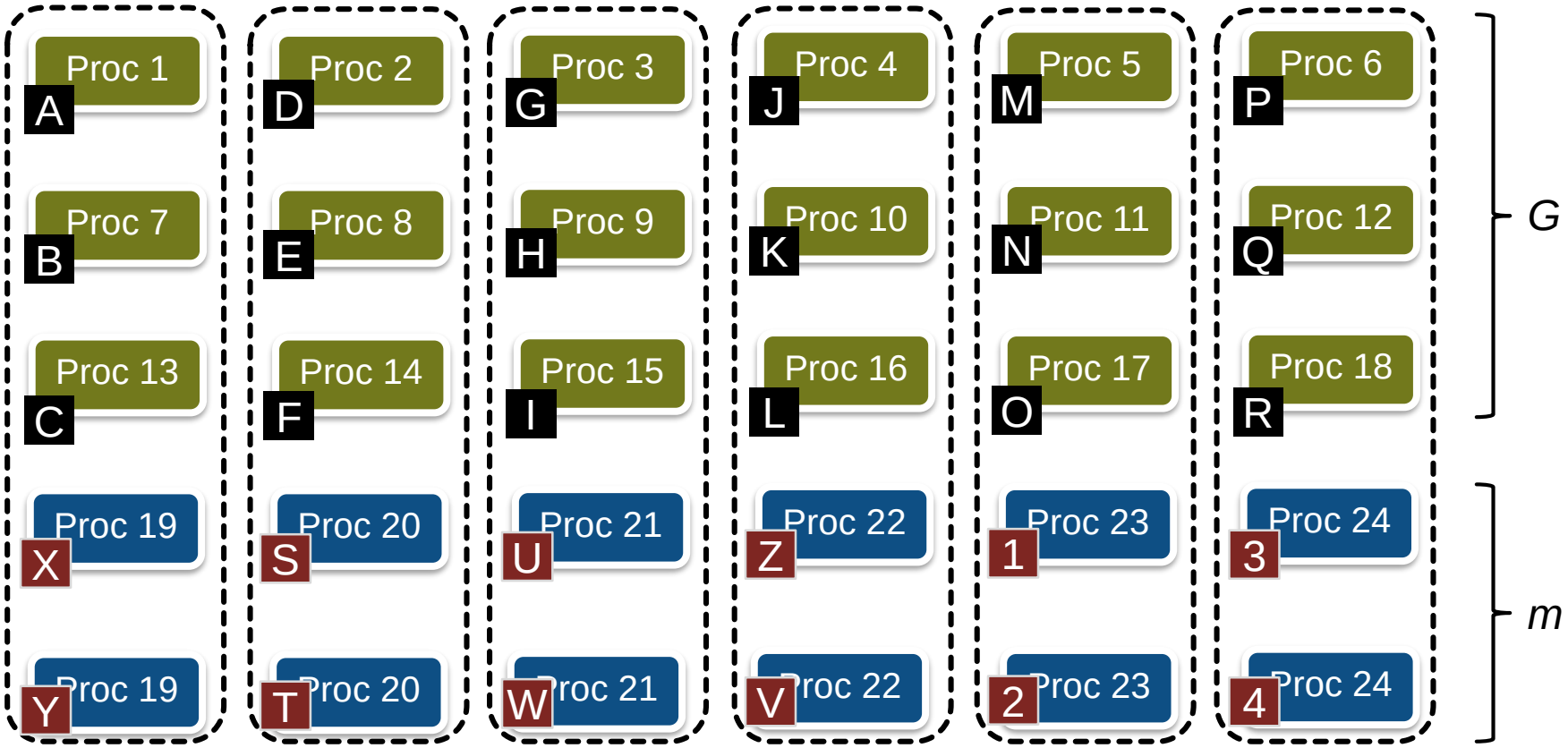

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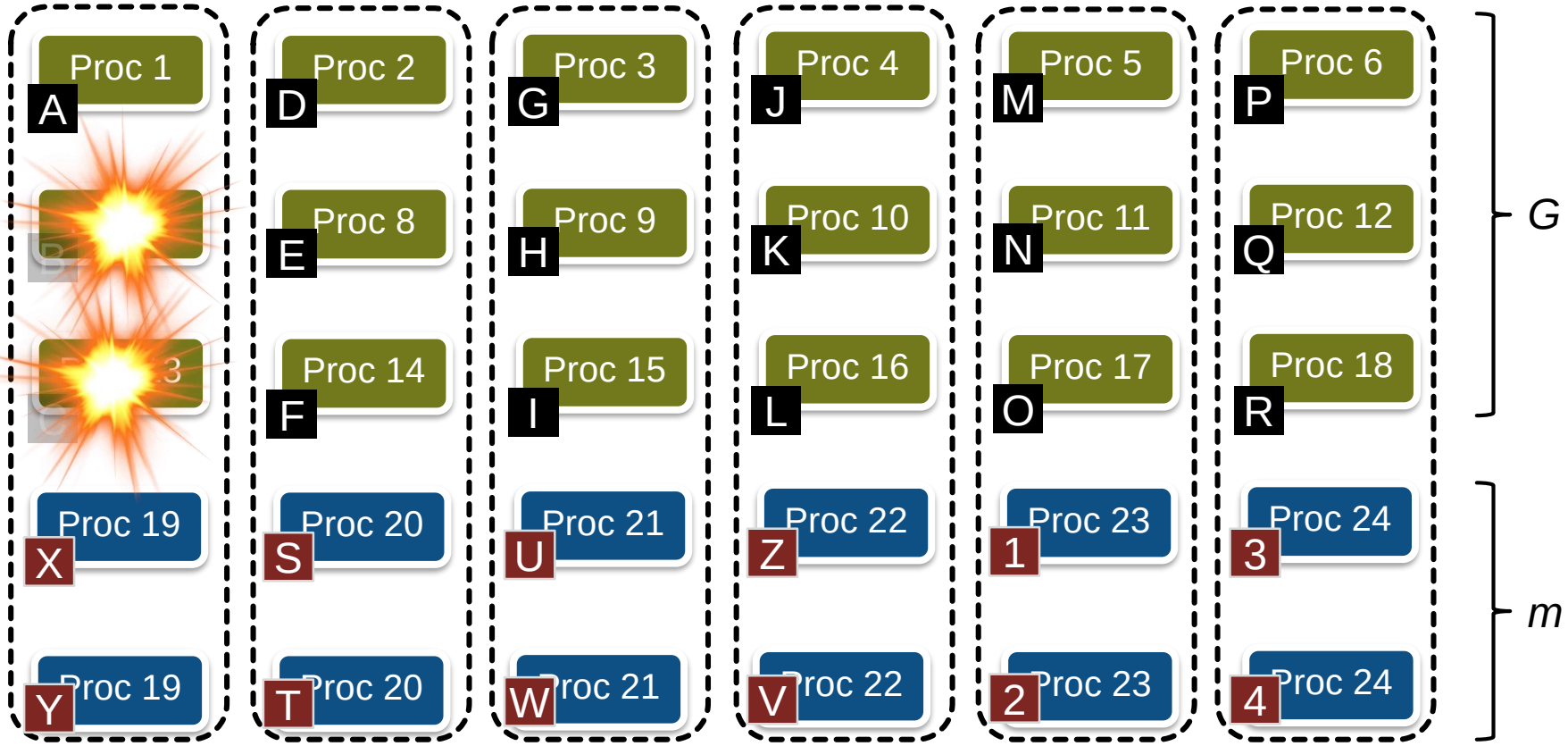

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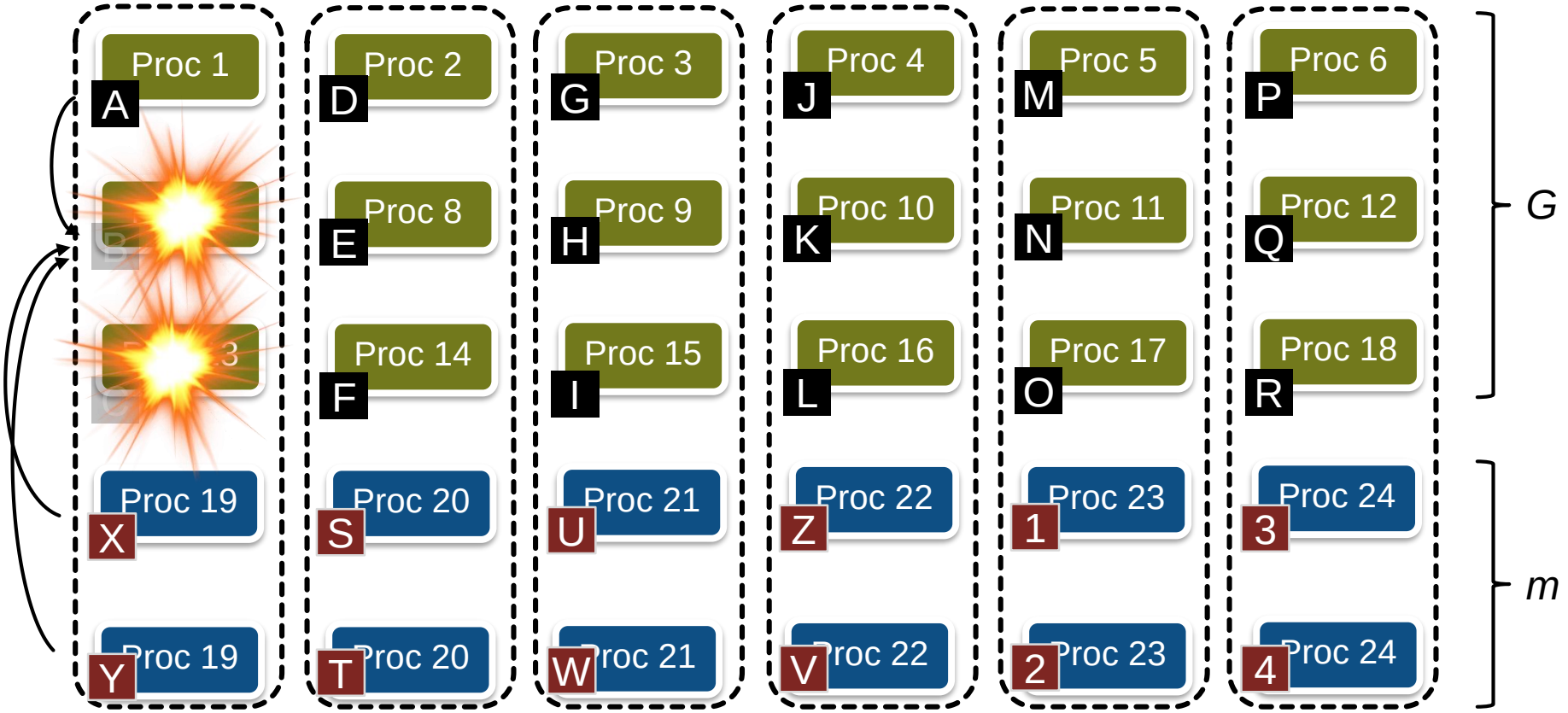

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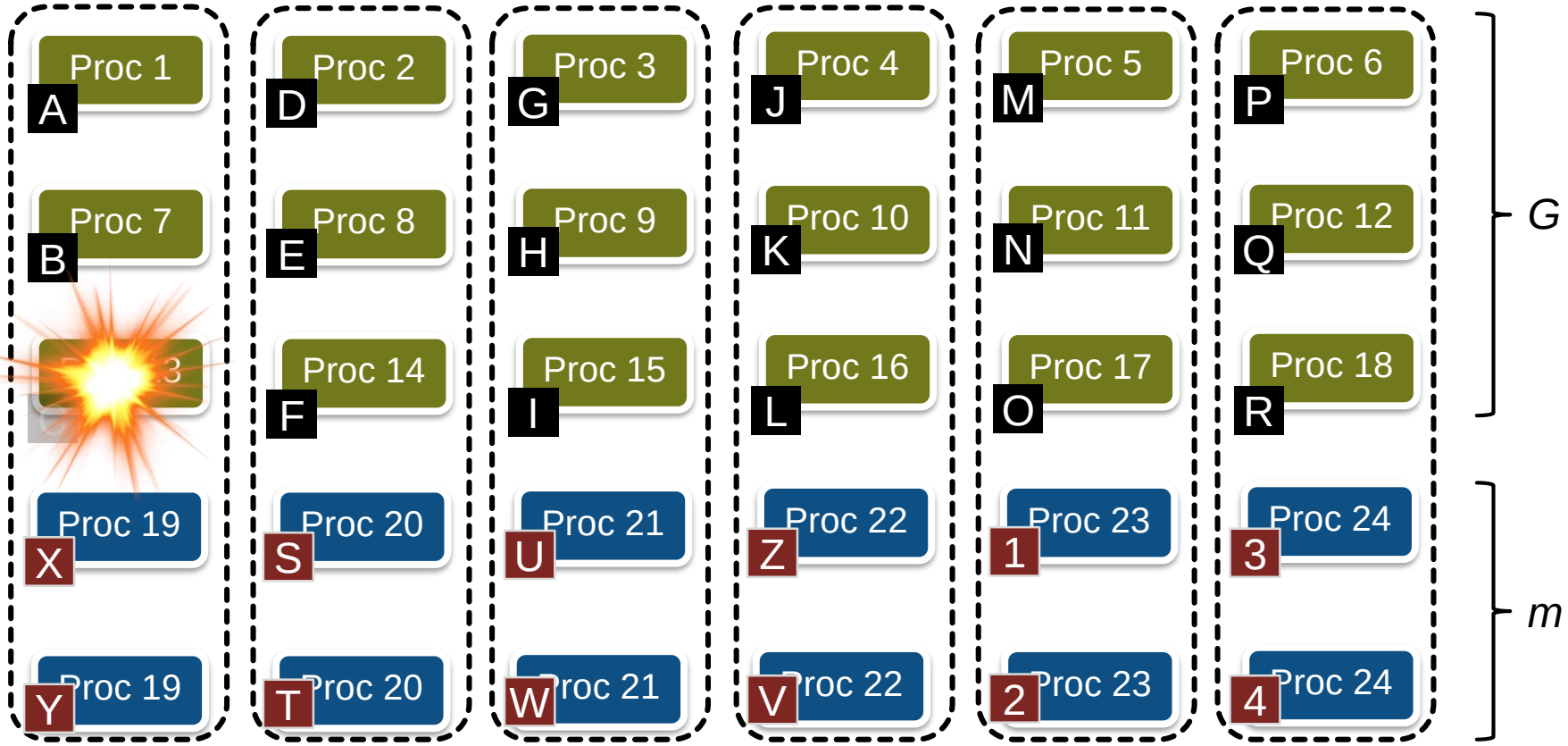

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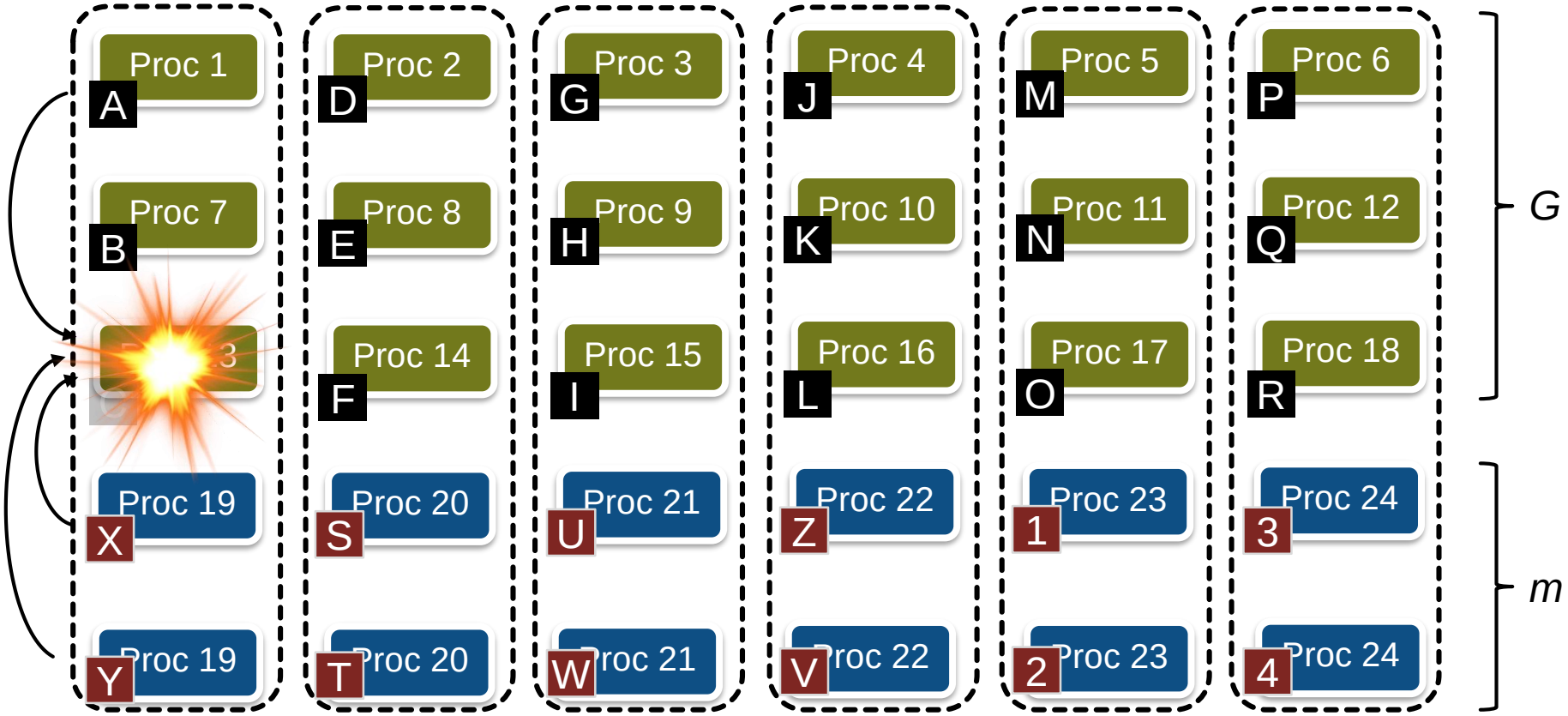

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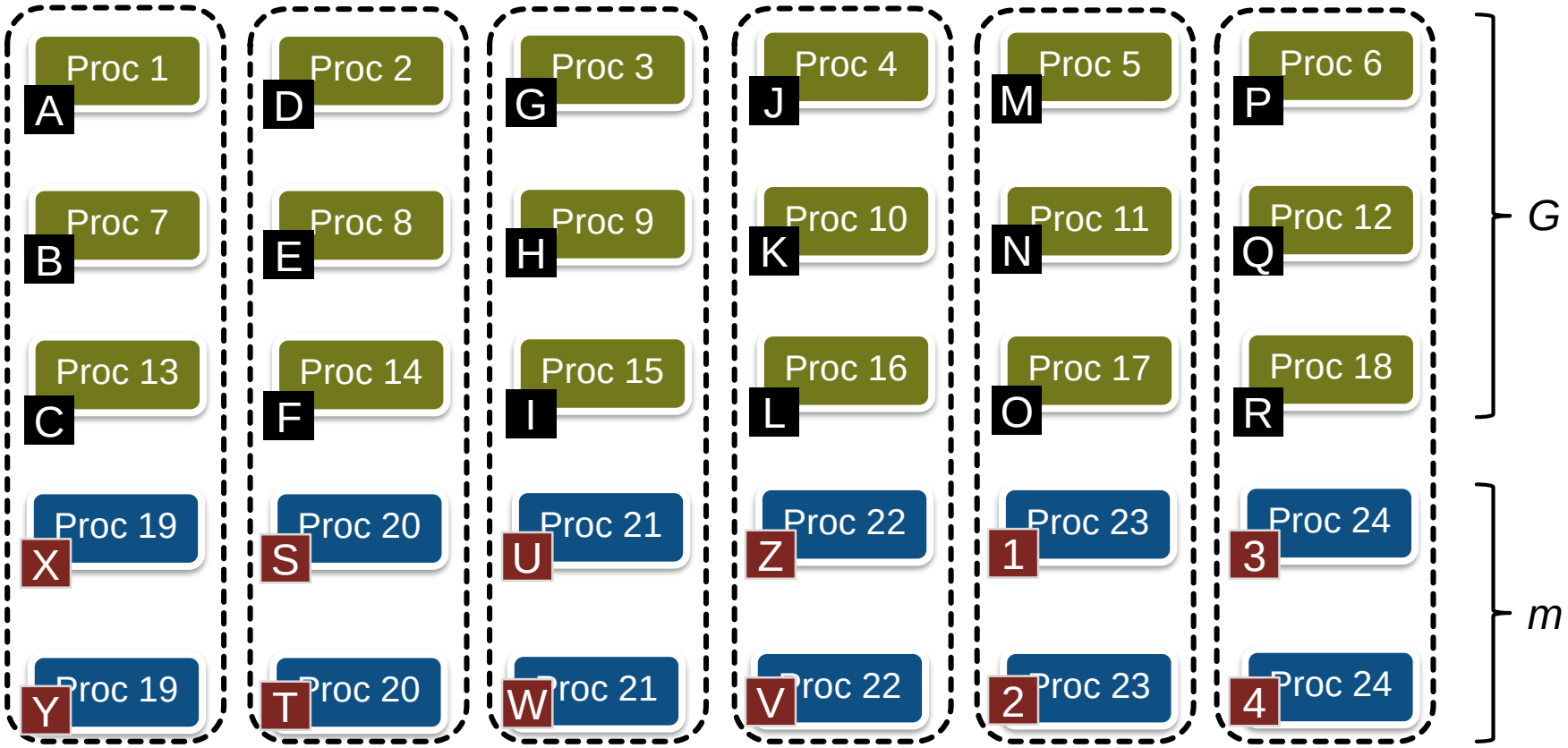

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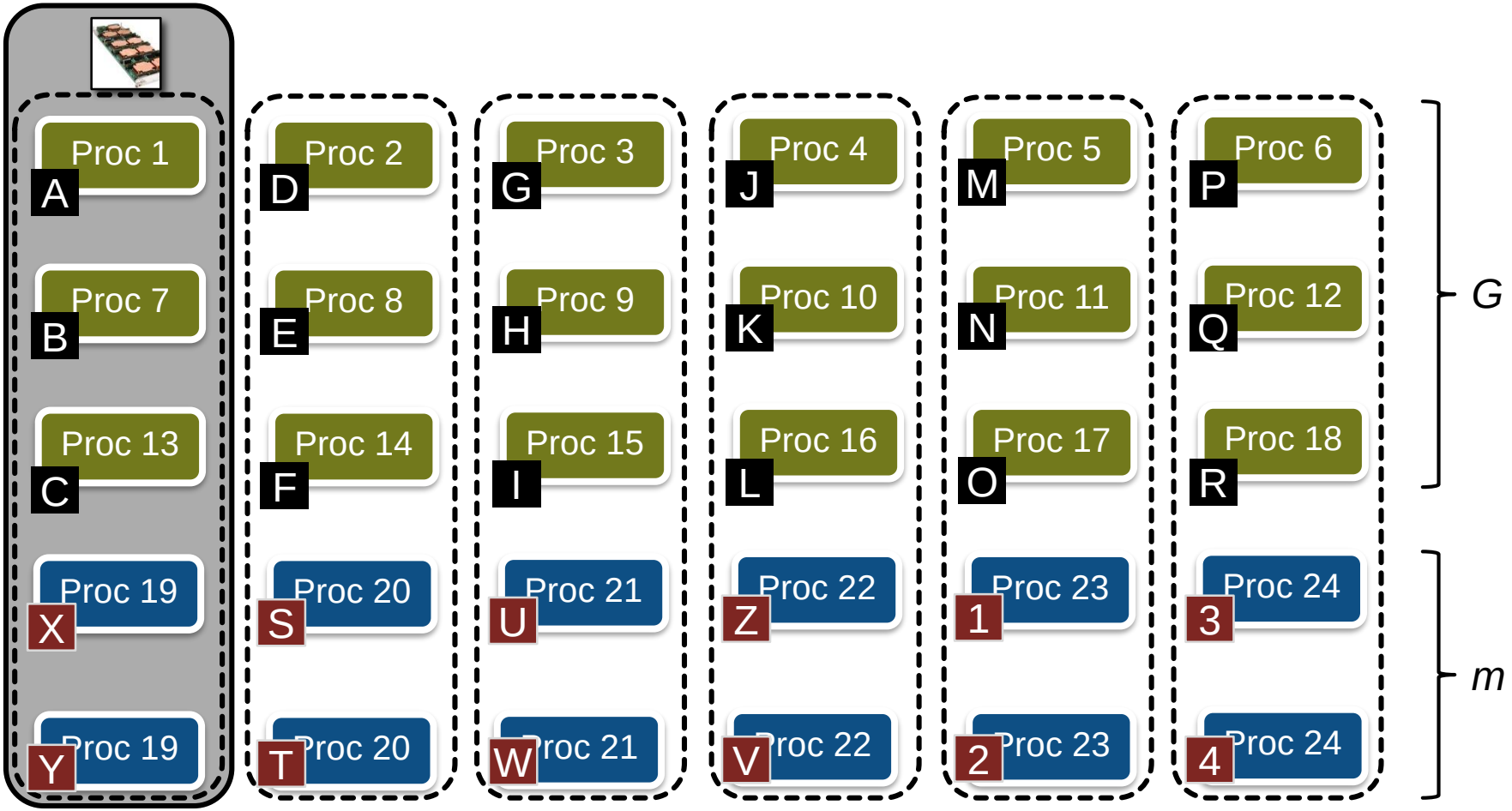

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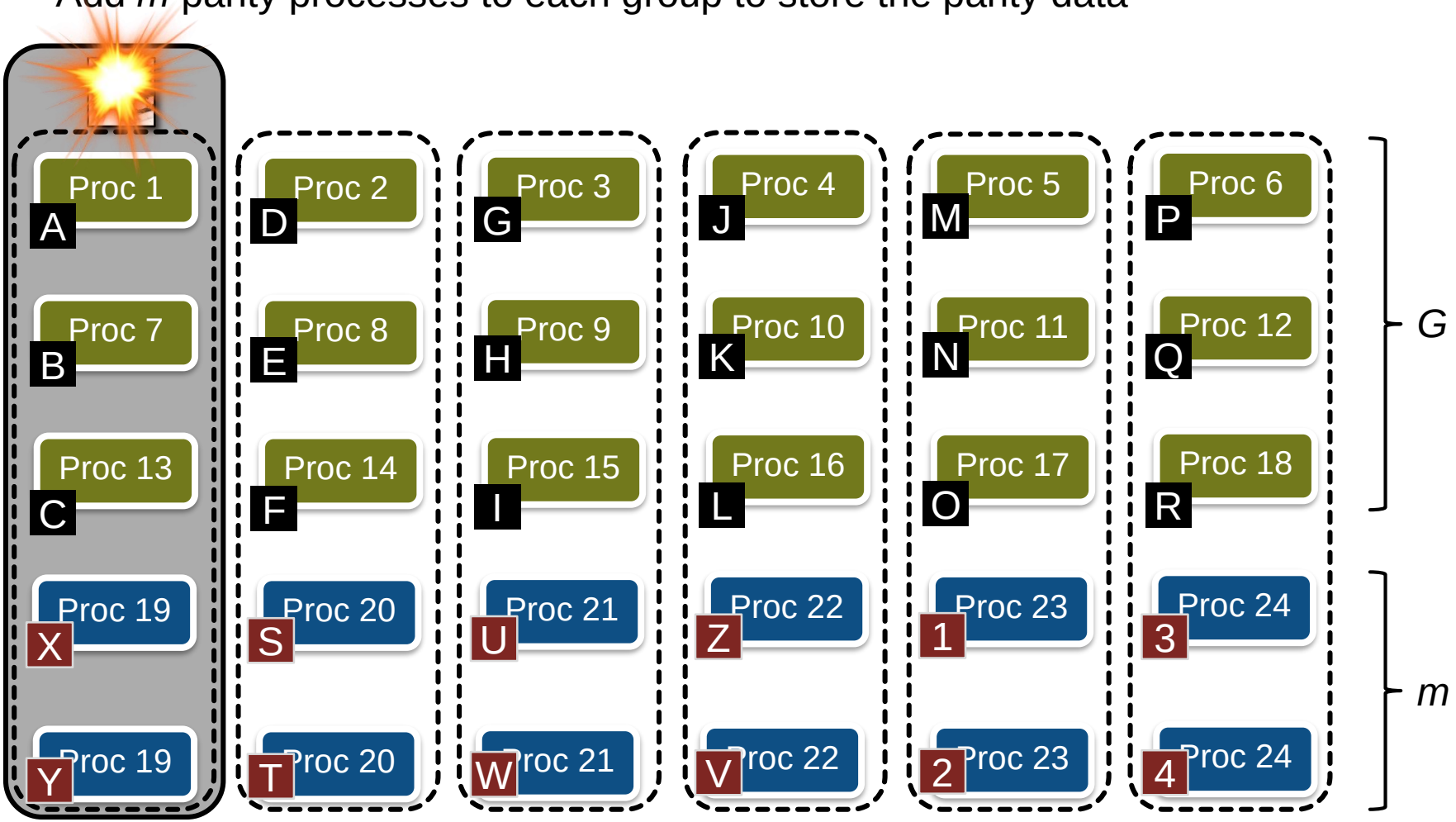

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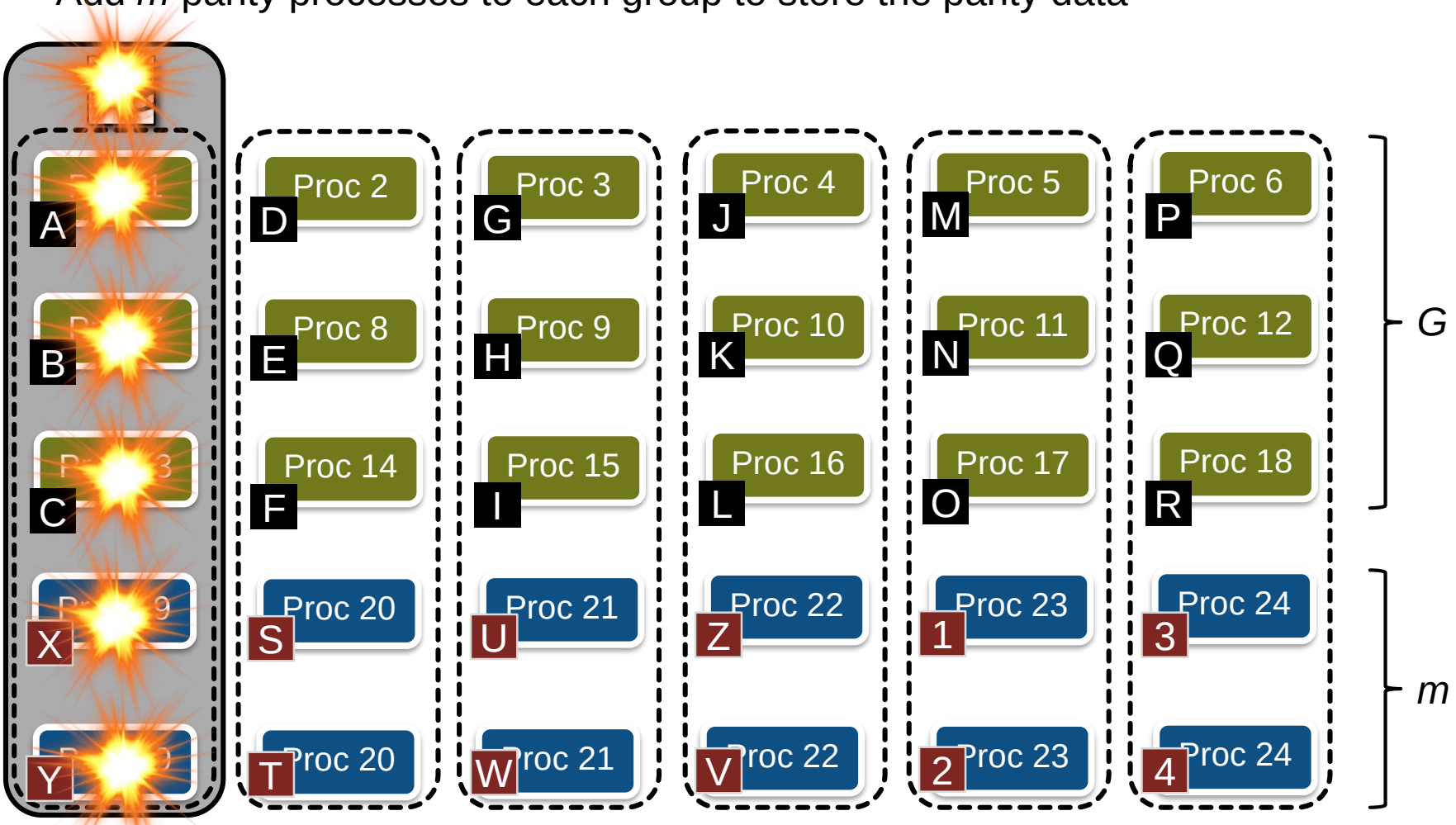

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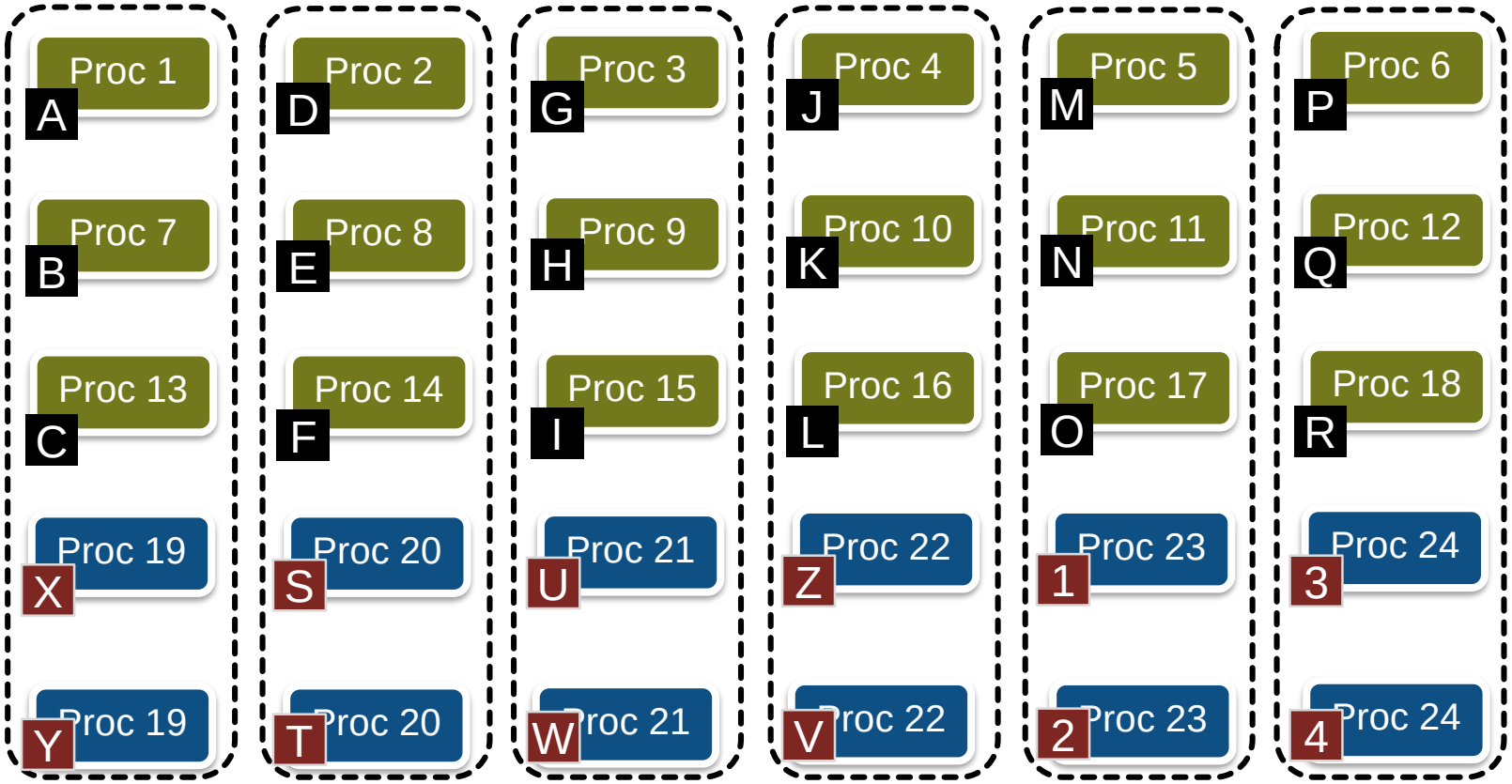

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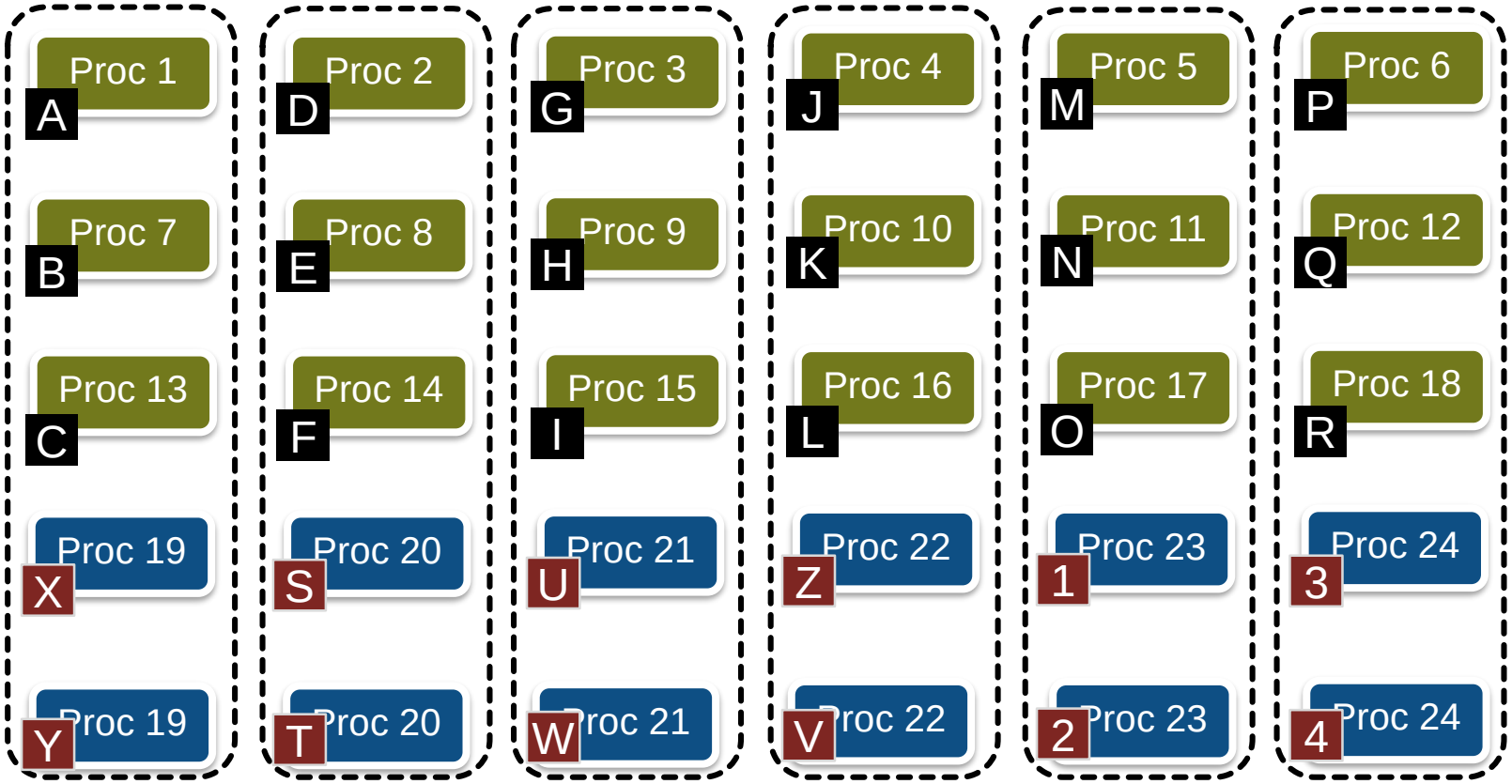

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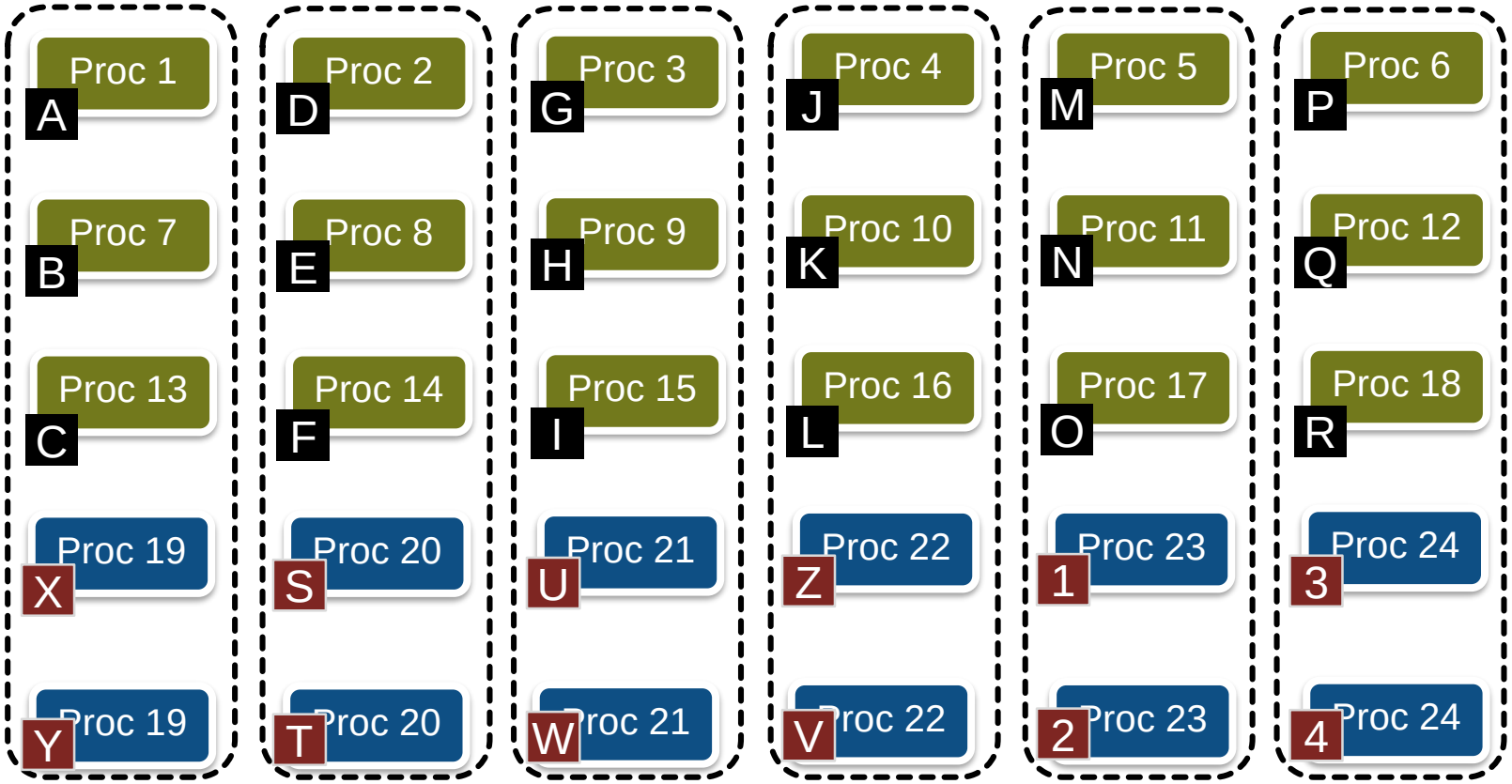

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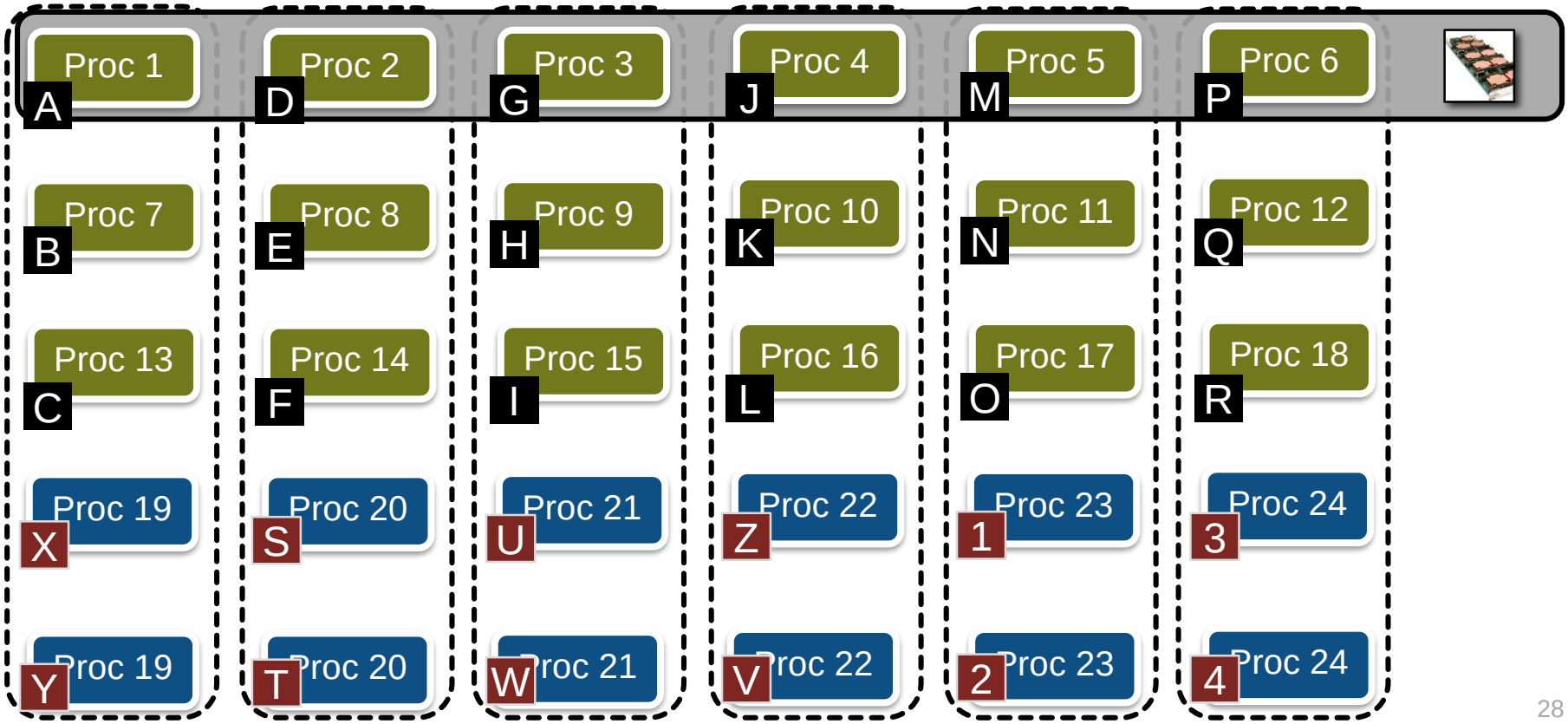

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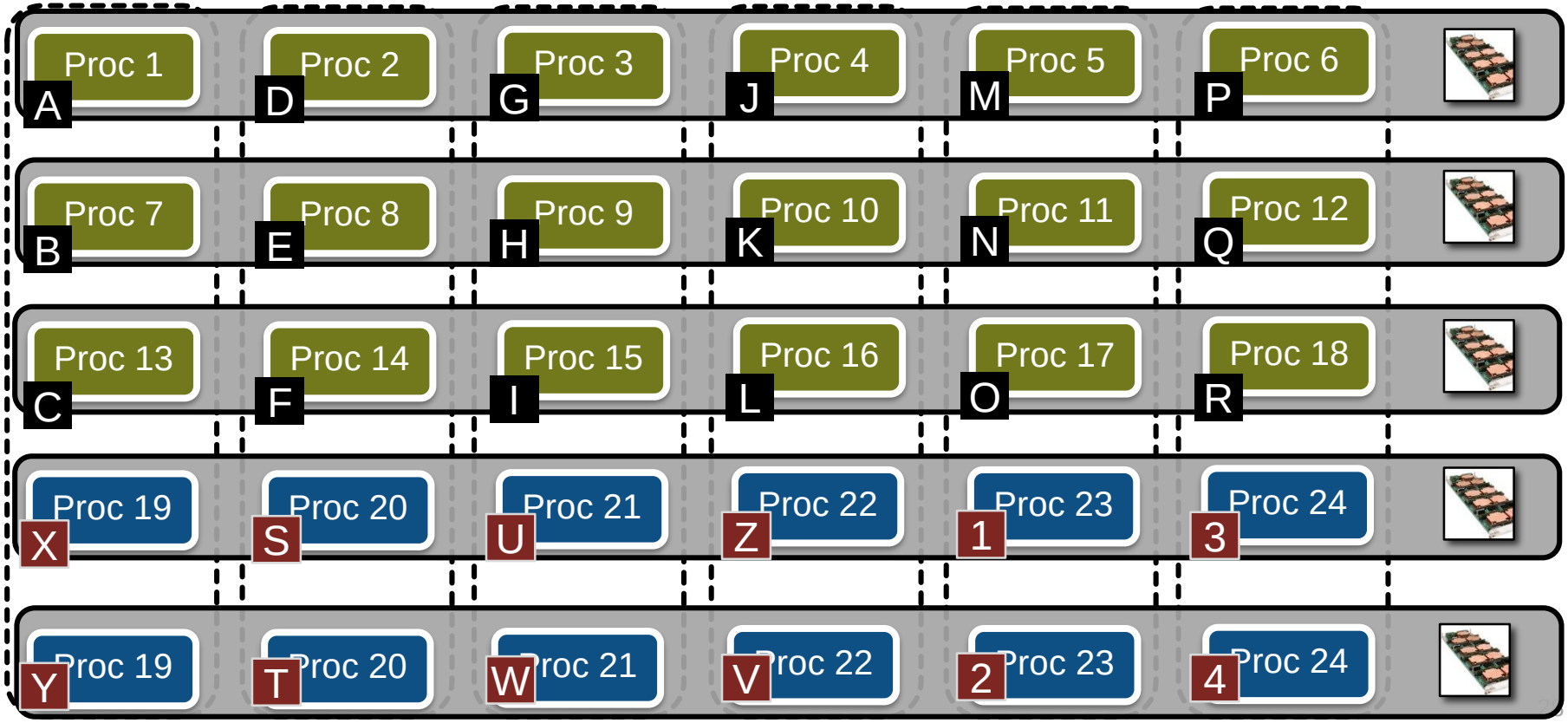

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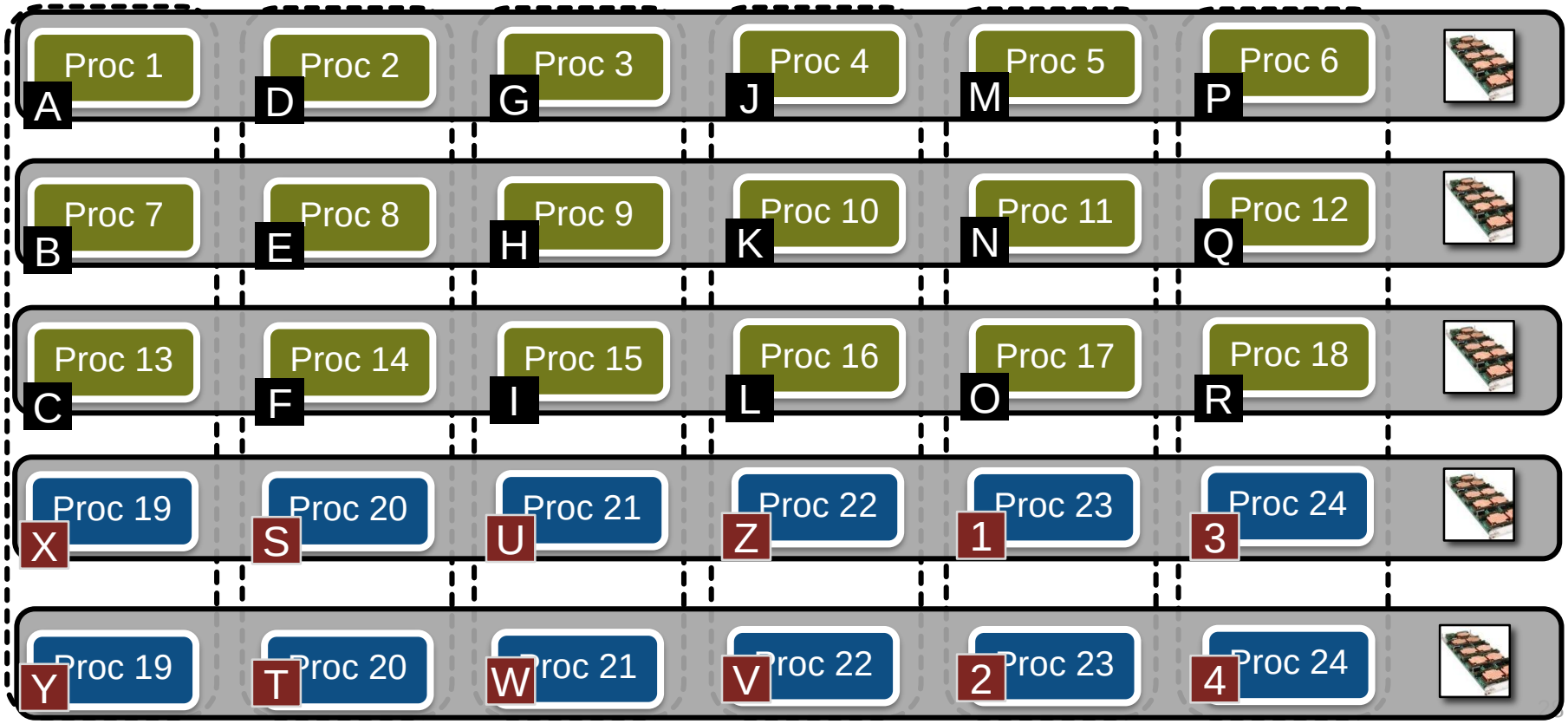

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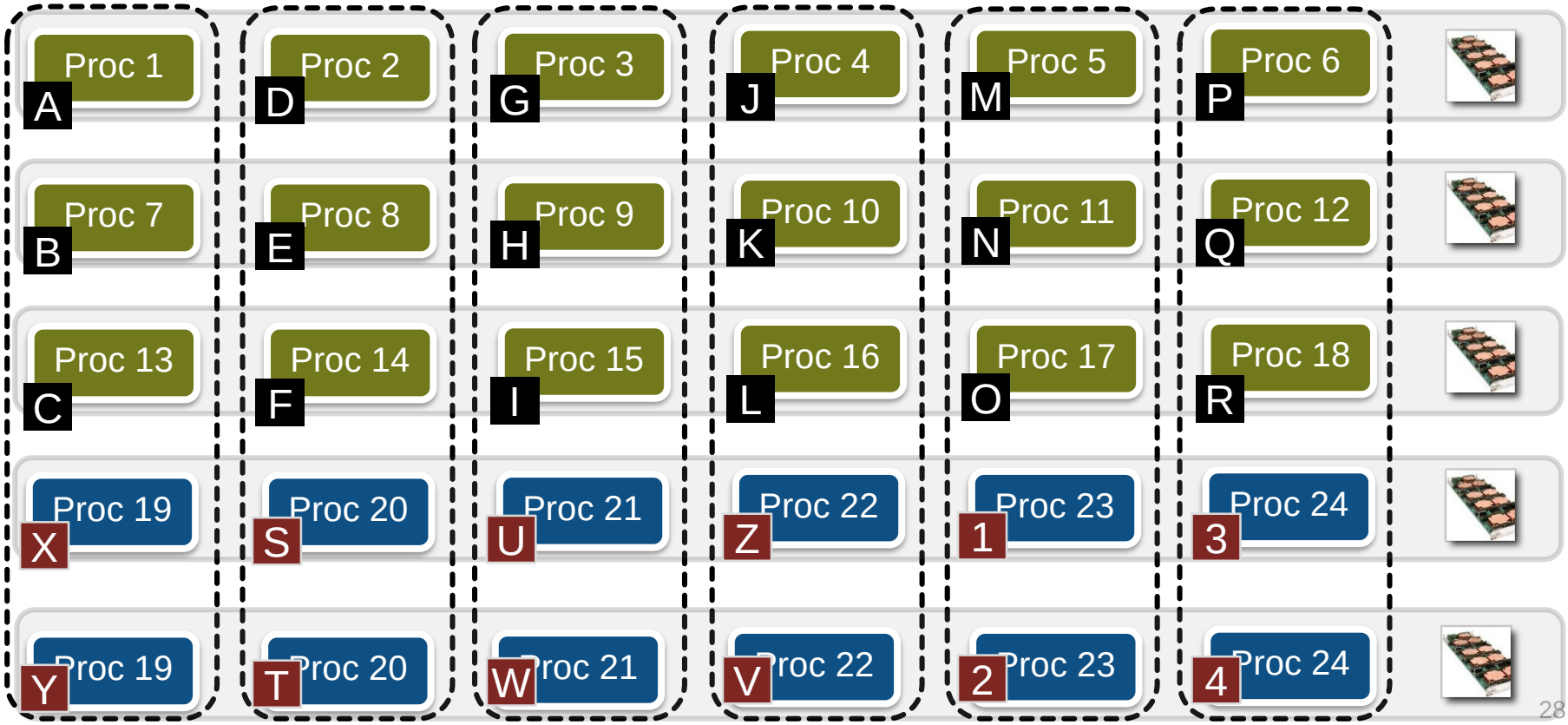

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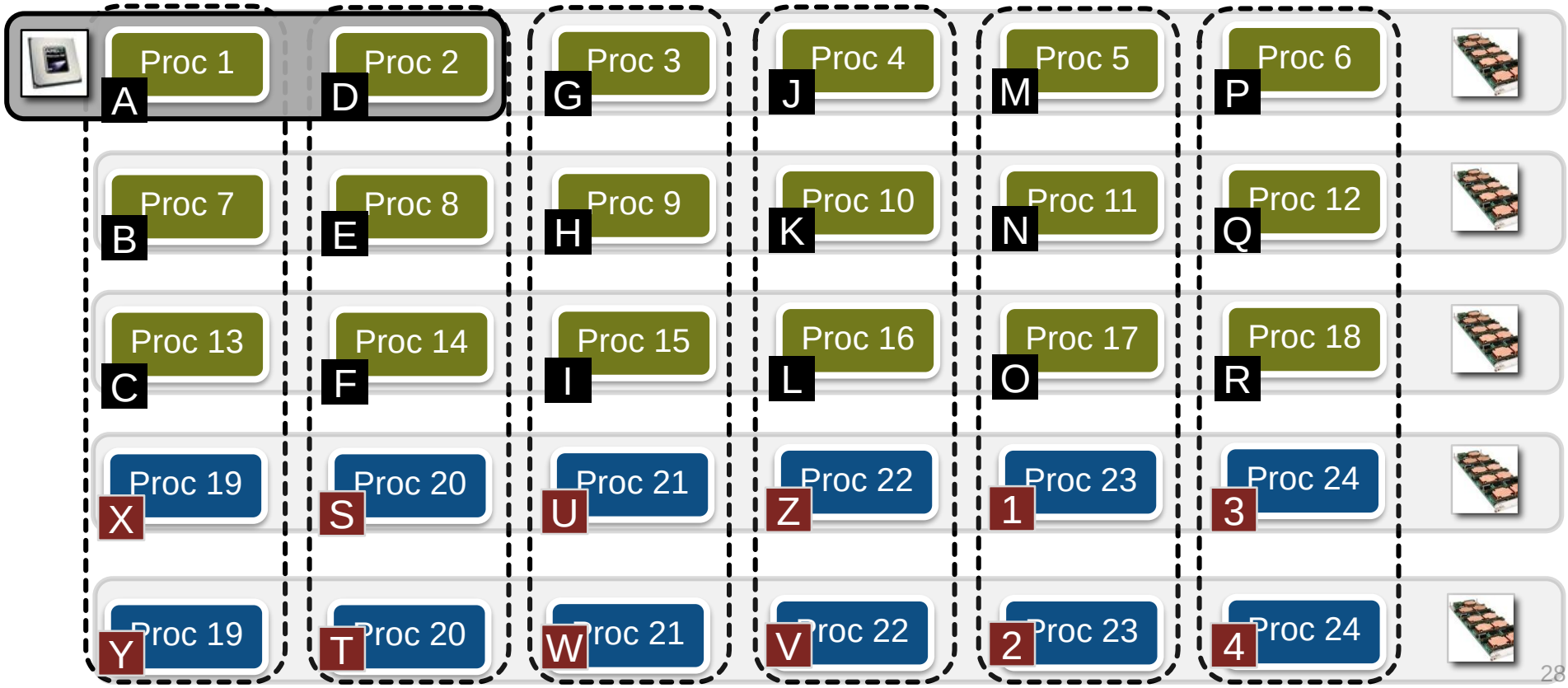

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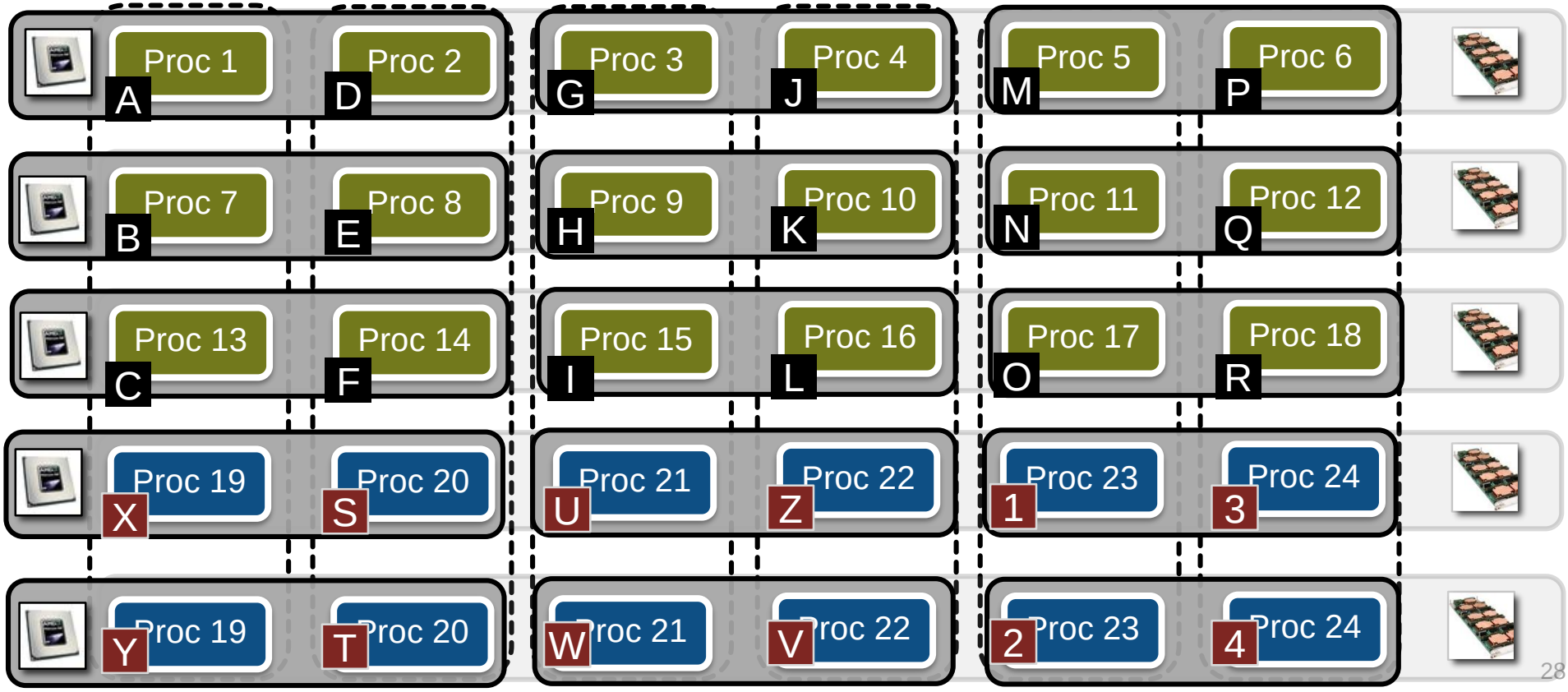

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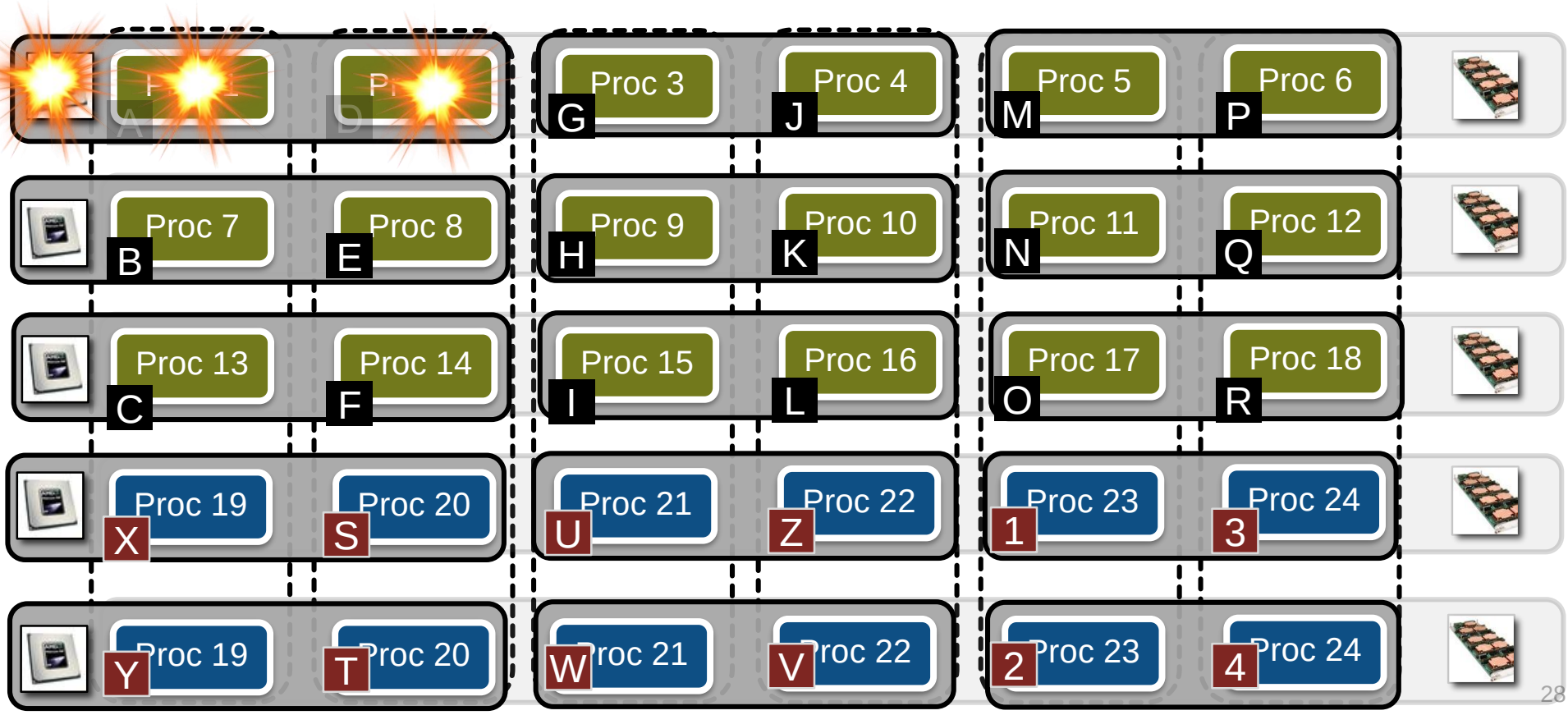

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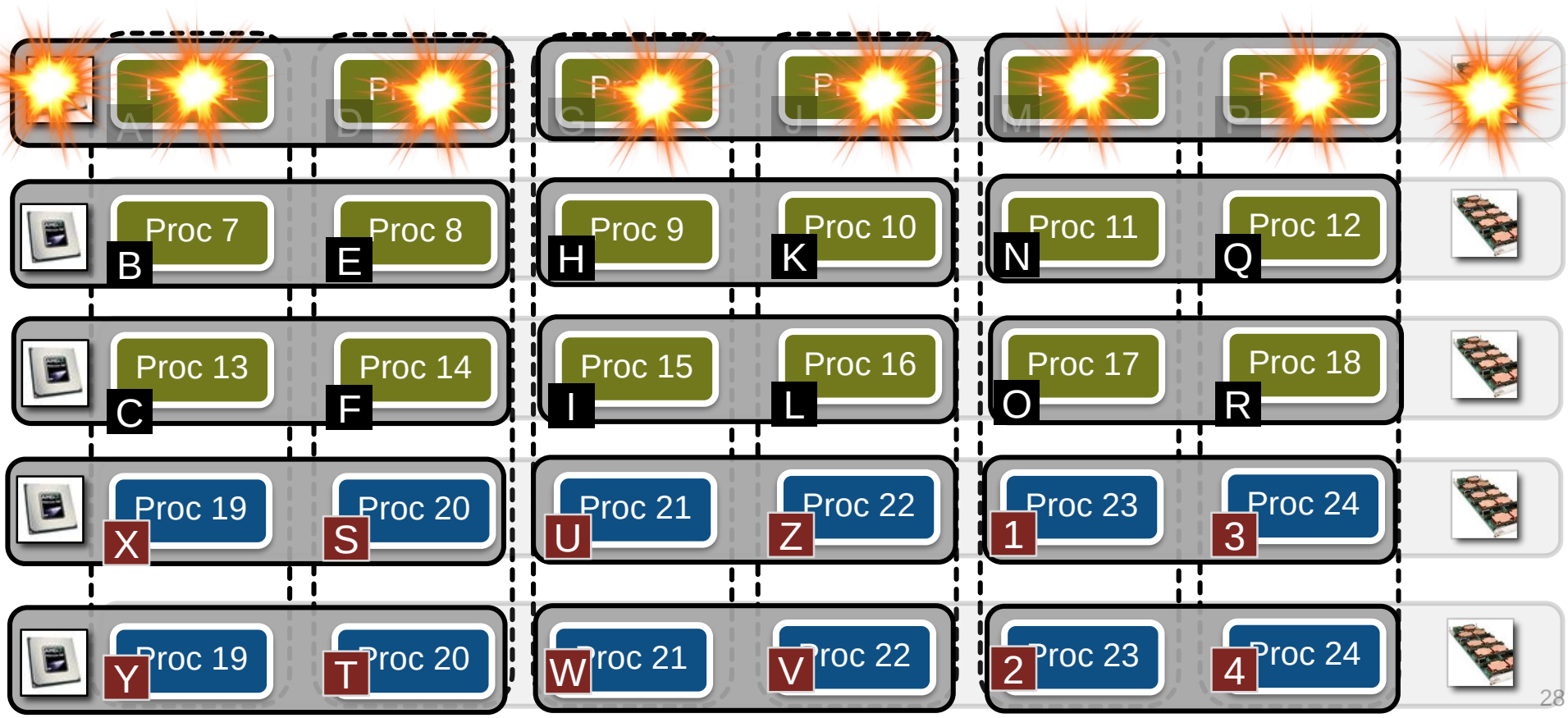

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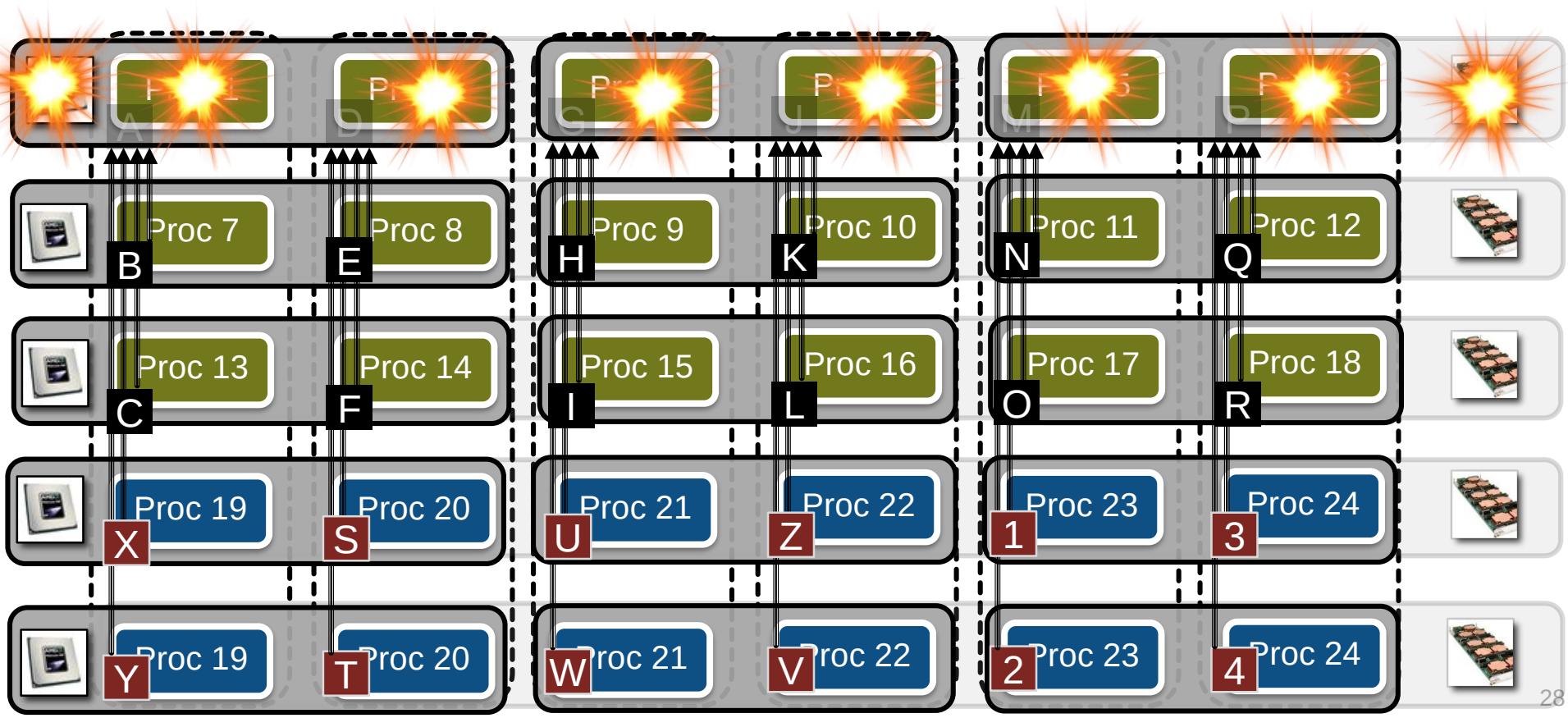

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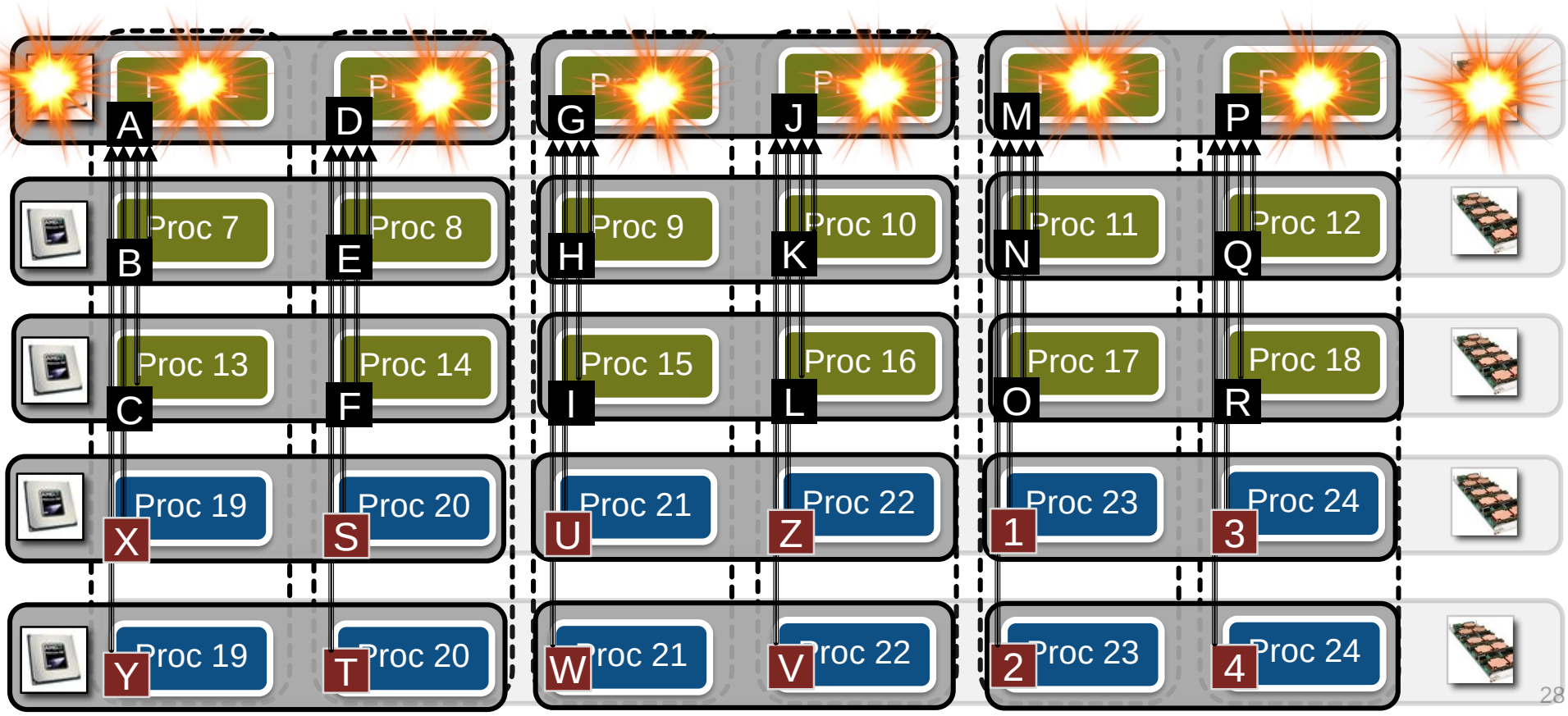

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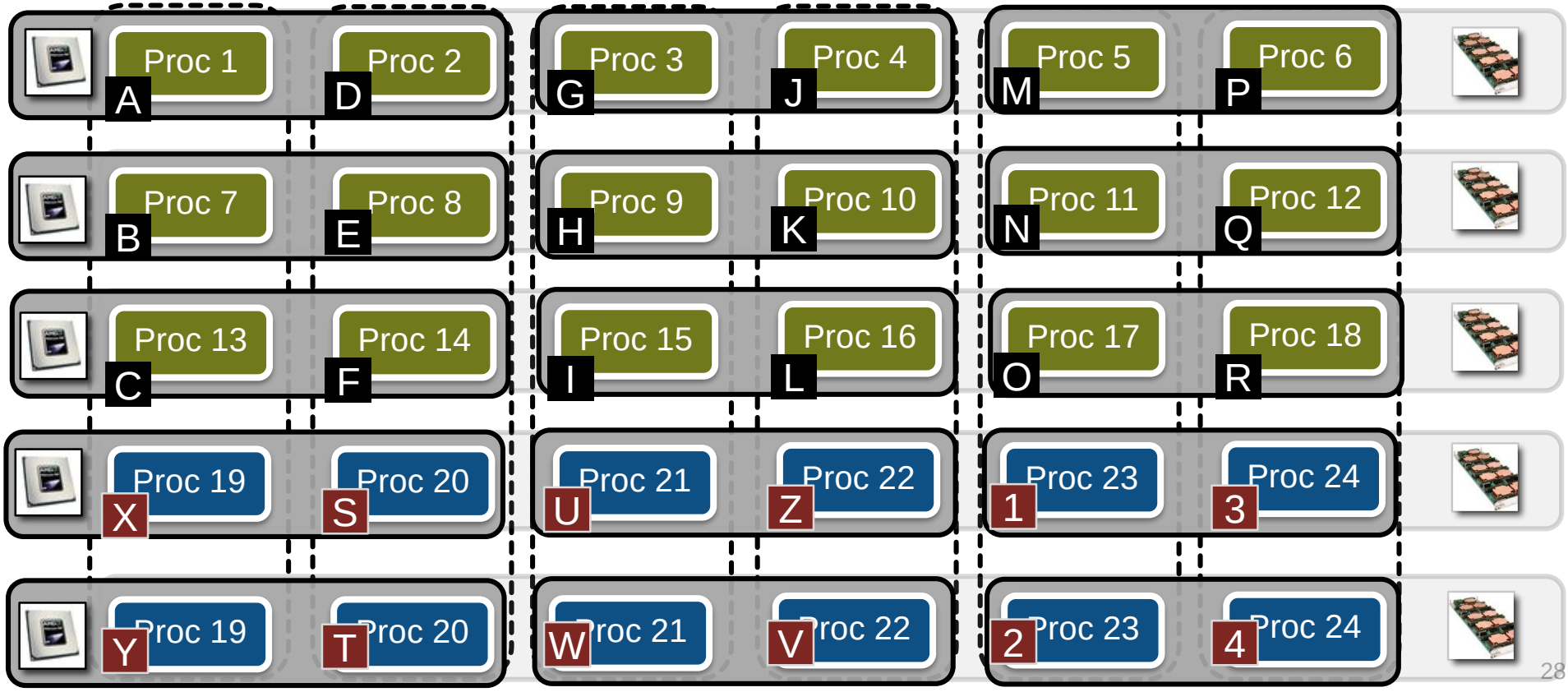

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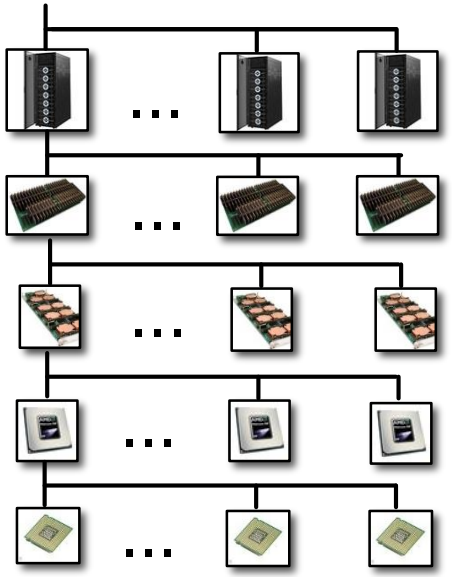

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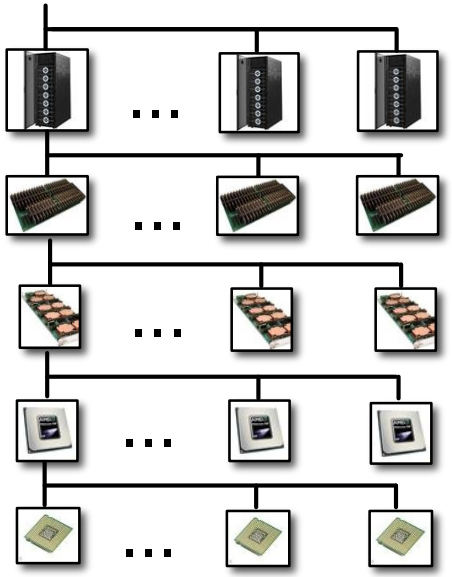

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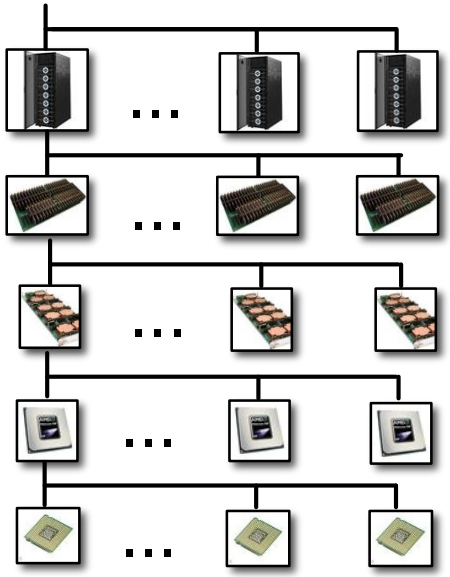

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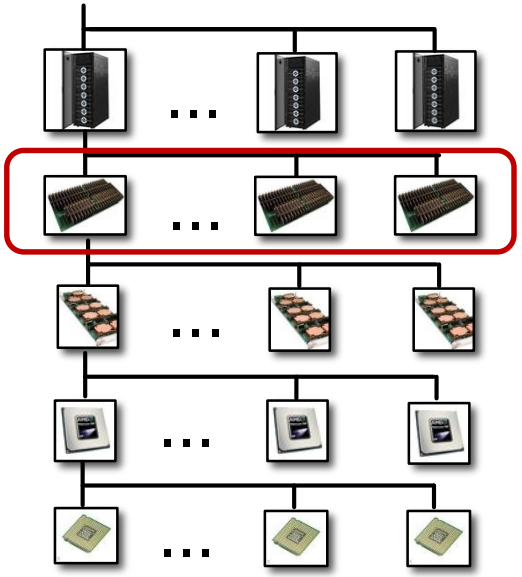

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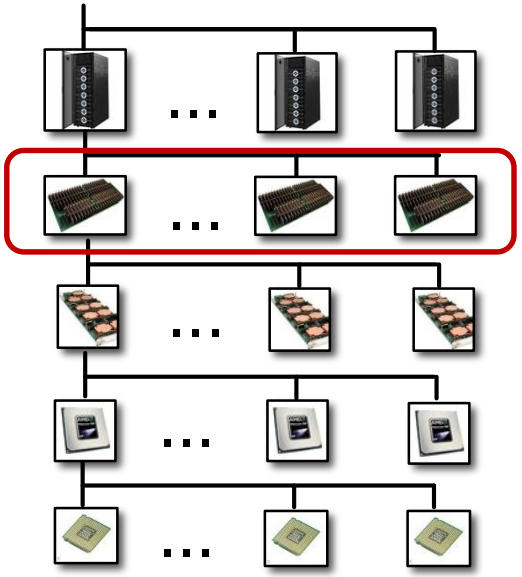

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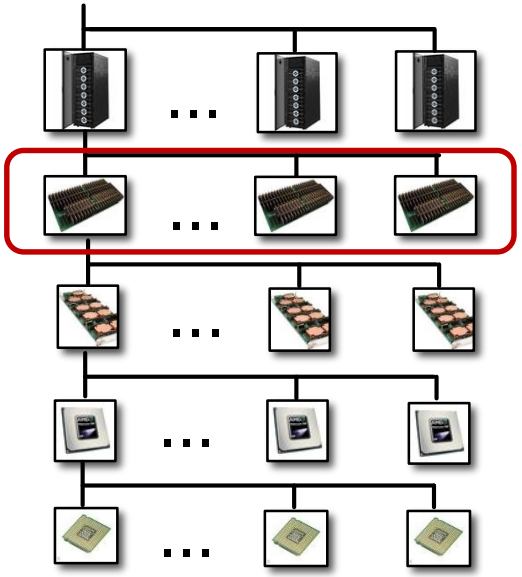

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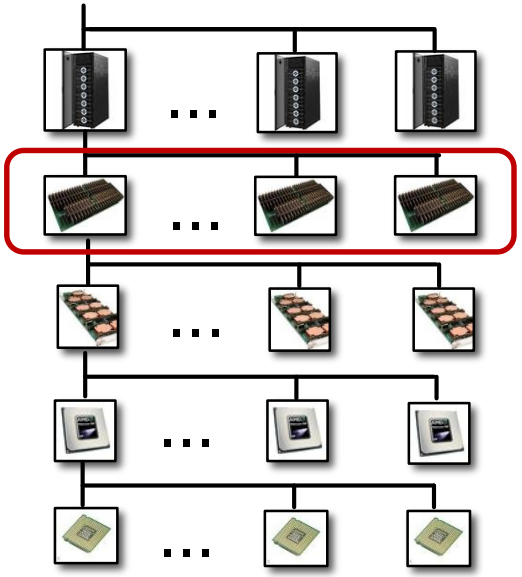

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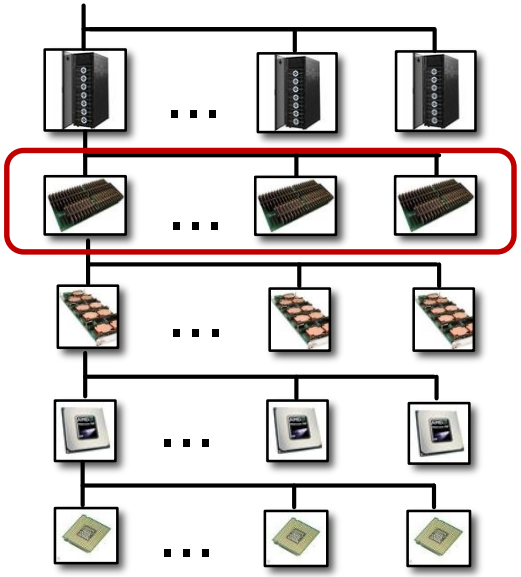

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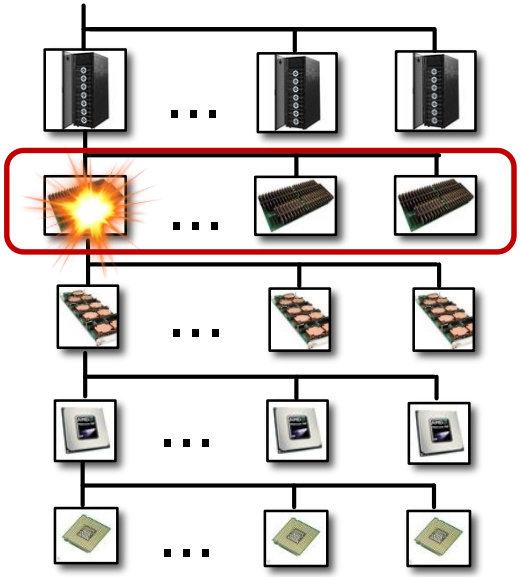

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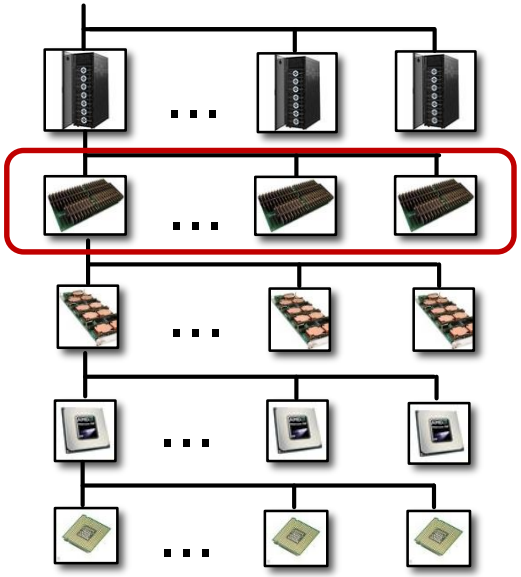

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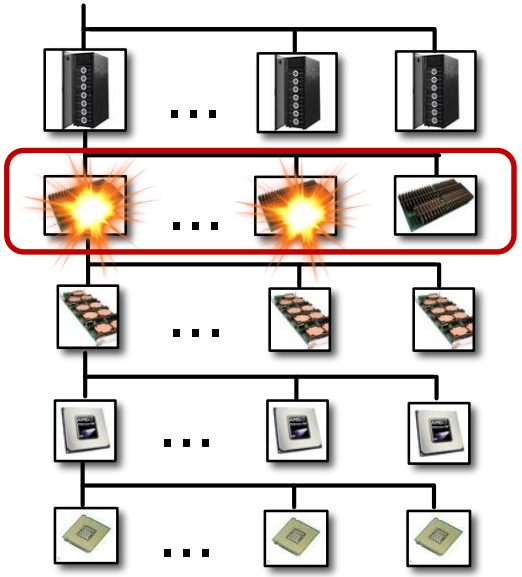

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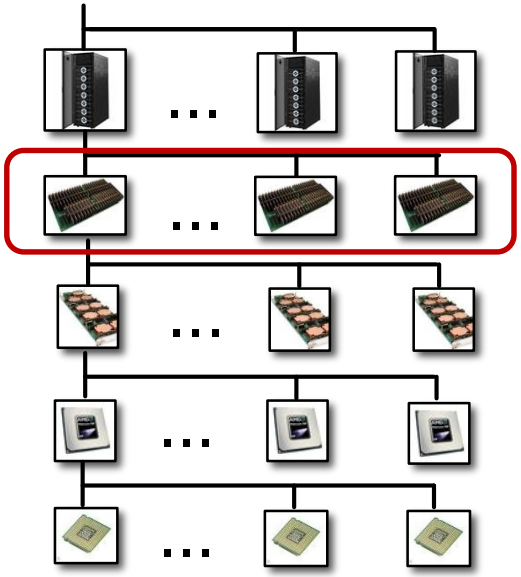

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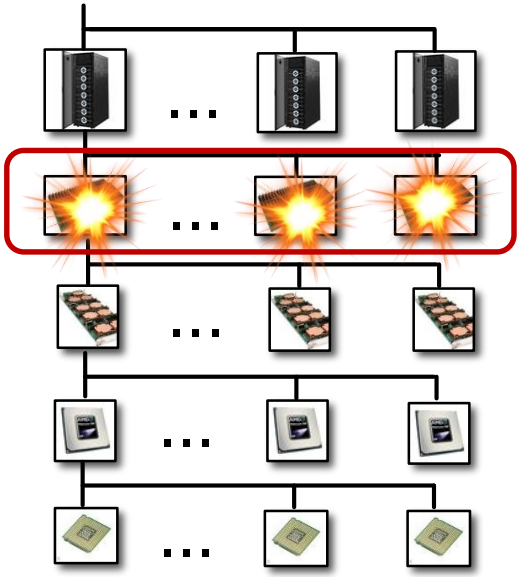

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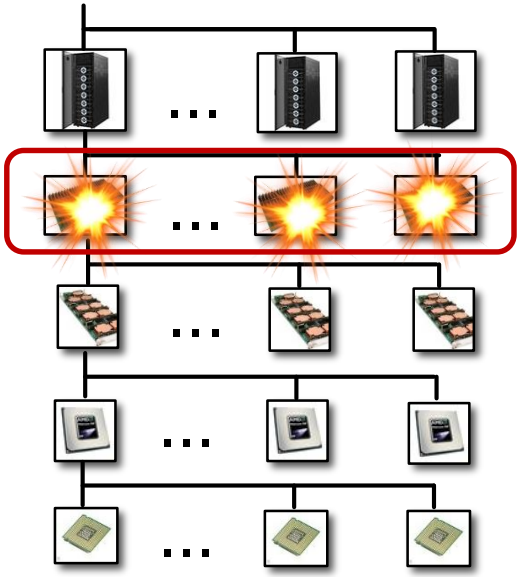

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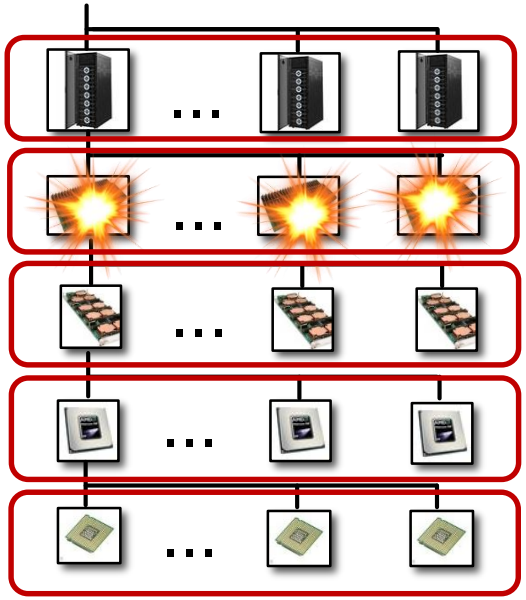

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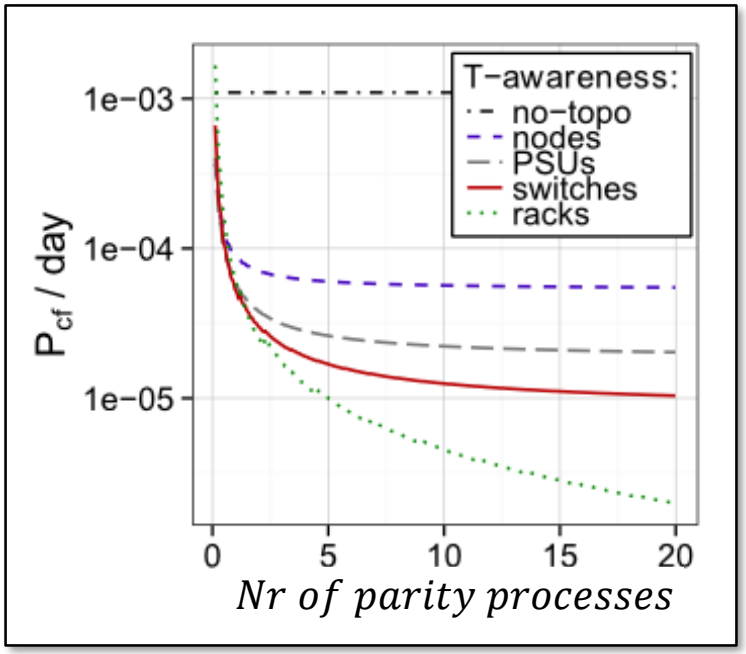

Overview of our Research

Generic model

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MPI-2 PGAS

CC in RMA

MP vs. RMA

Schemes

UC in RMA

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Holistic fault-tolerance library

Design

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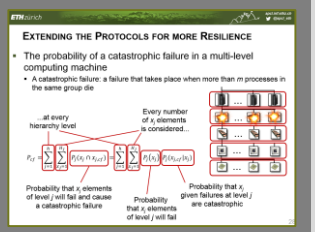

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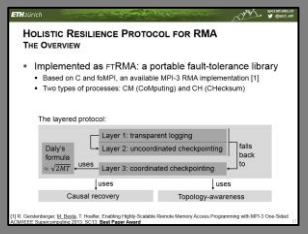

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Holistic Resilience Protocol for RMA

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- Implemented as FTRMA: a portable fault-tolerance library
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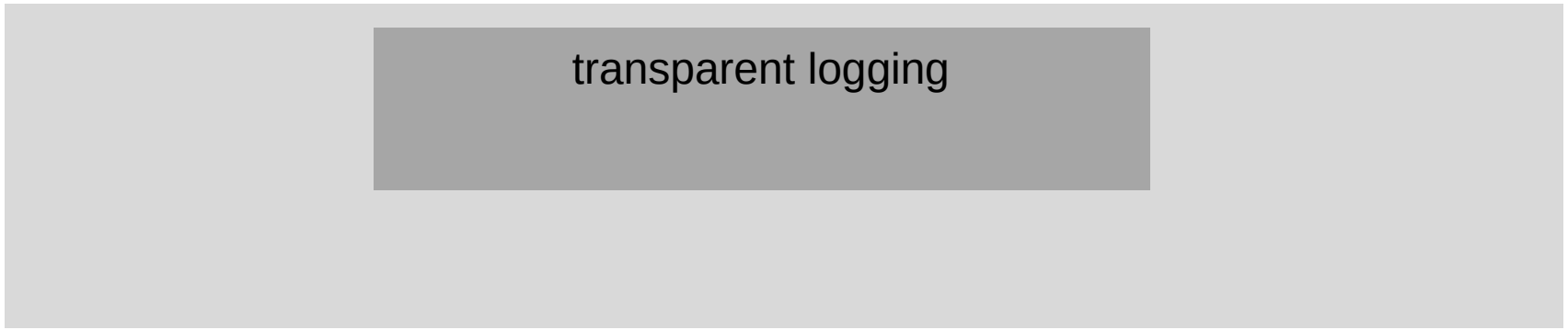

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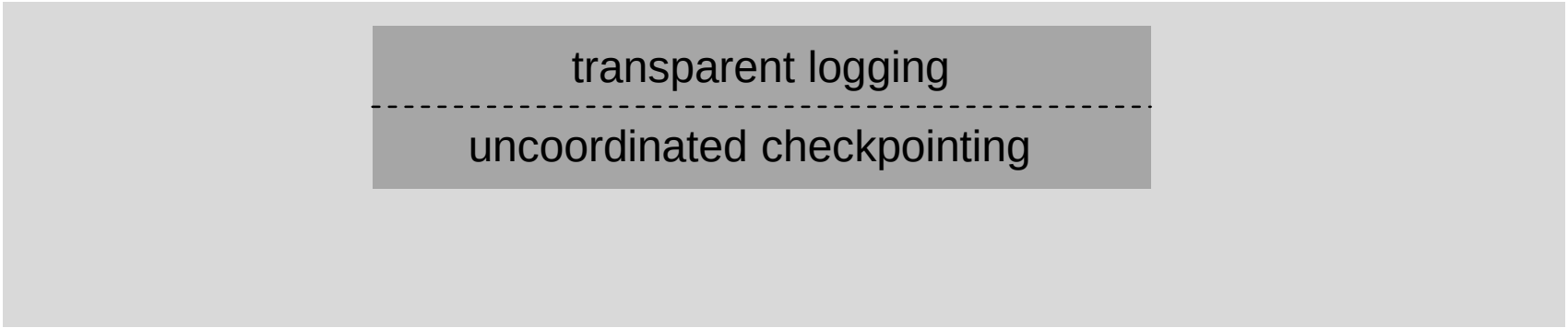

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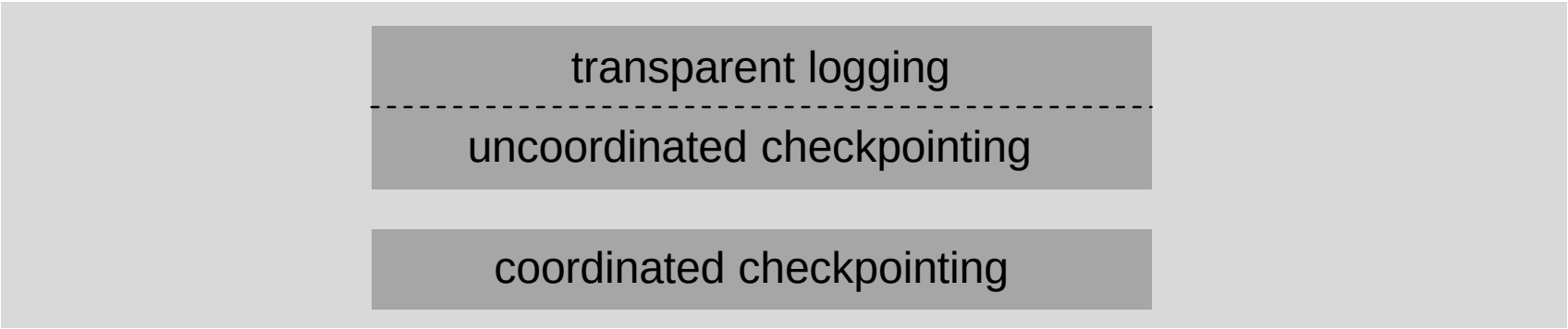

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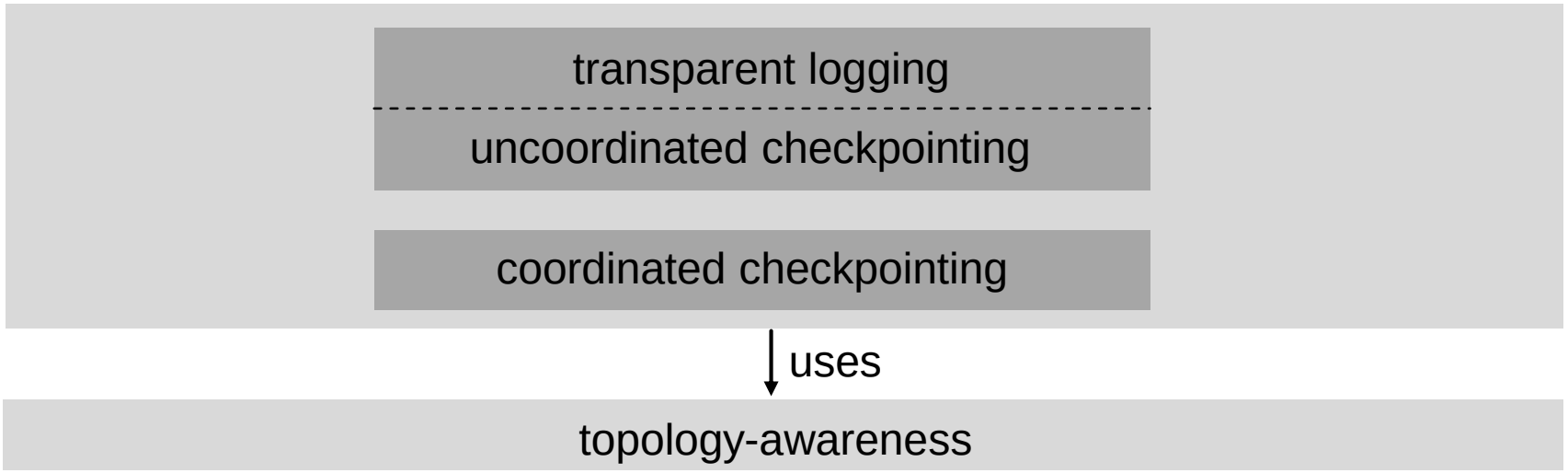

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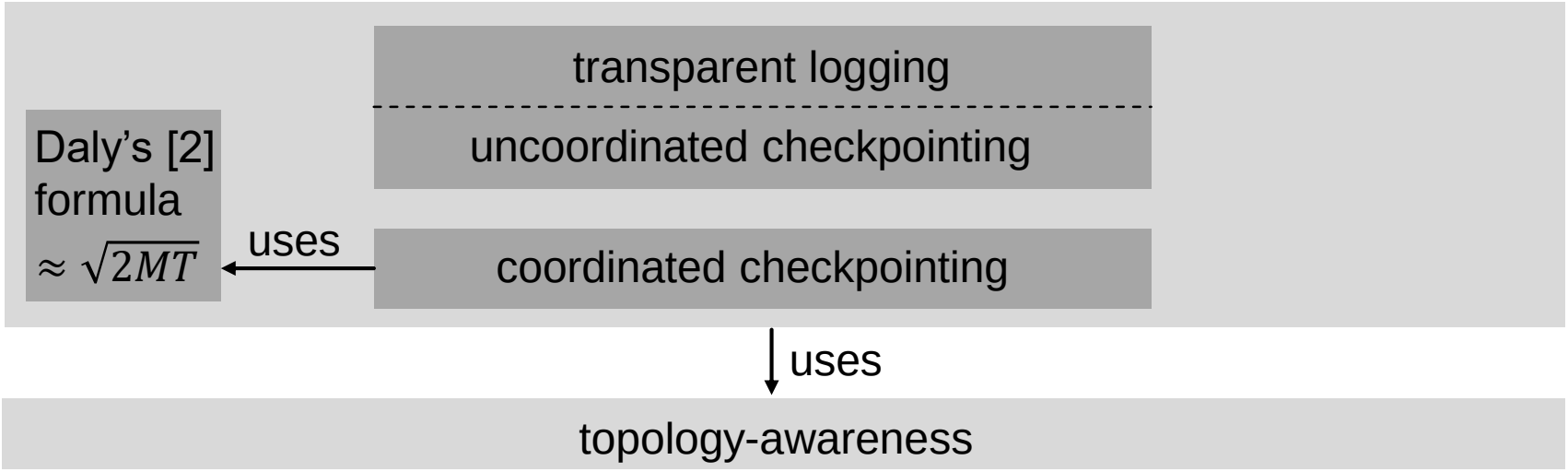

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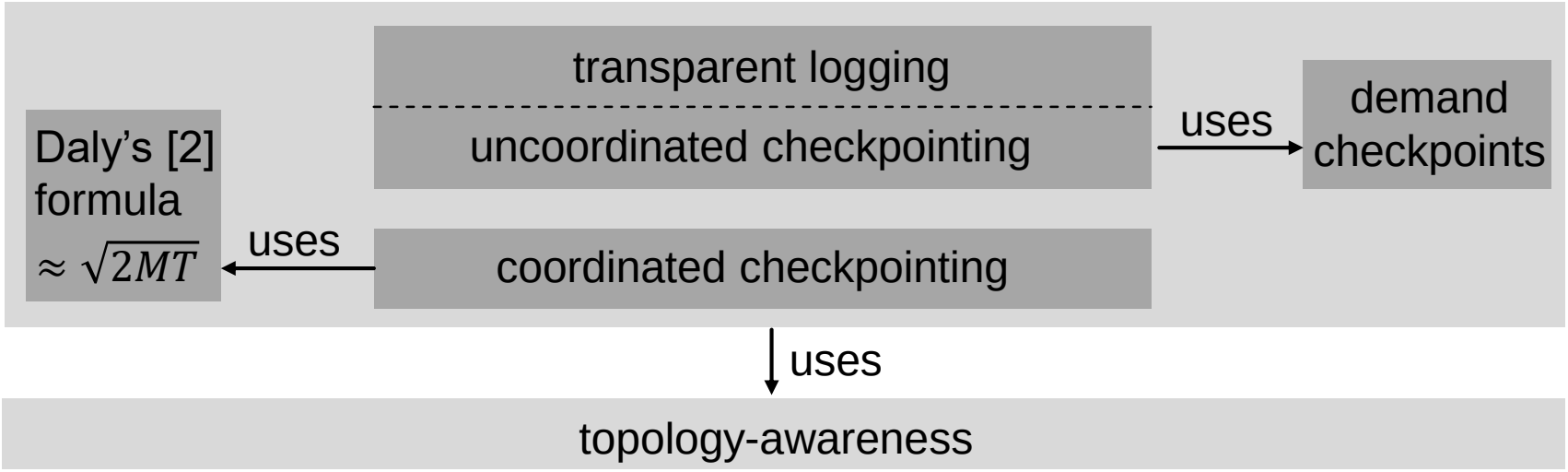
[2] J.T.Daly, A higher order estimate of the optimum checkpoint interval for restart dumps. Future Generation Computer Systems, Volume 22 Issue 3, February 2006, Pages 303-312

HOLISTIC RESILIENCE PROTOCOL FOR RMA
THE OVERVIEW

- Implemented as FTRMA: a portable fault-tolerance library
  - Based on C and foMPI, an available MPI-3 RMA implementation [1]

The layered protocol:



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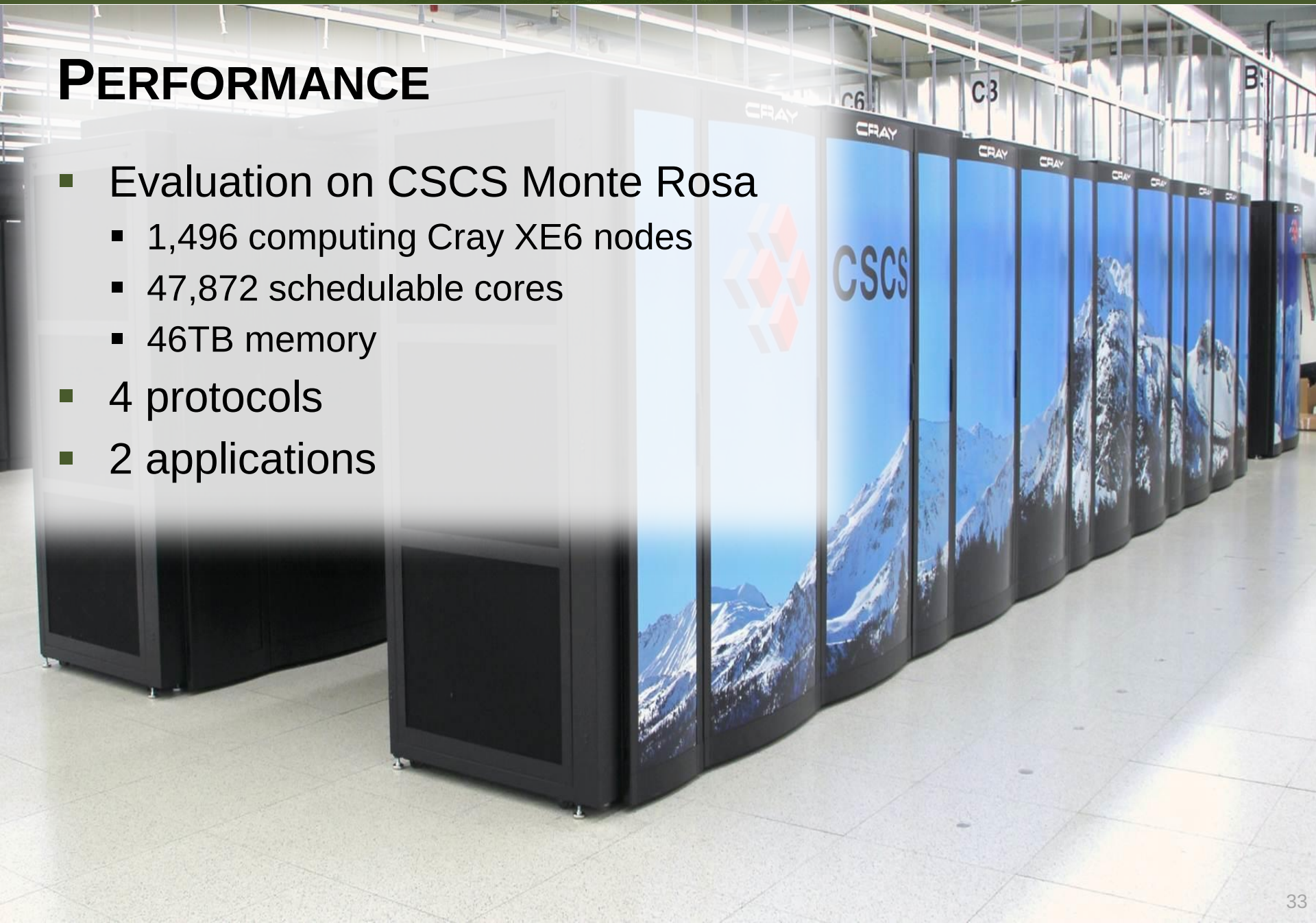
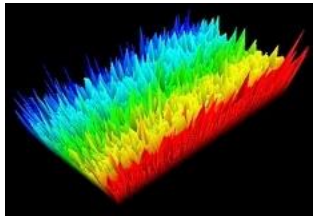
PERFORMANCE

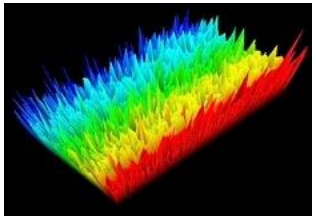


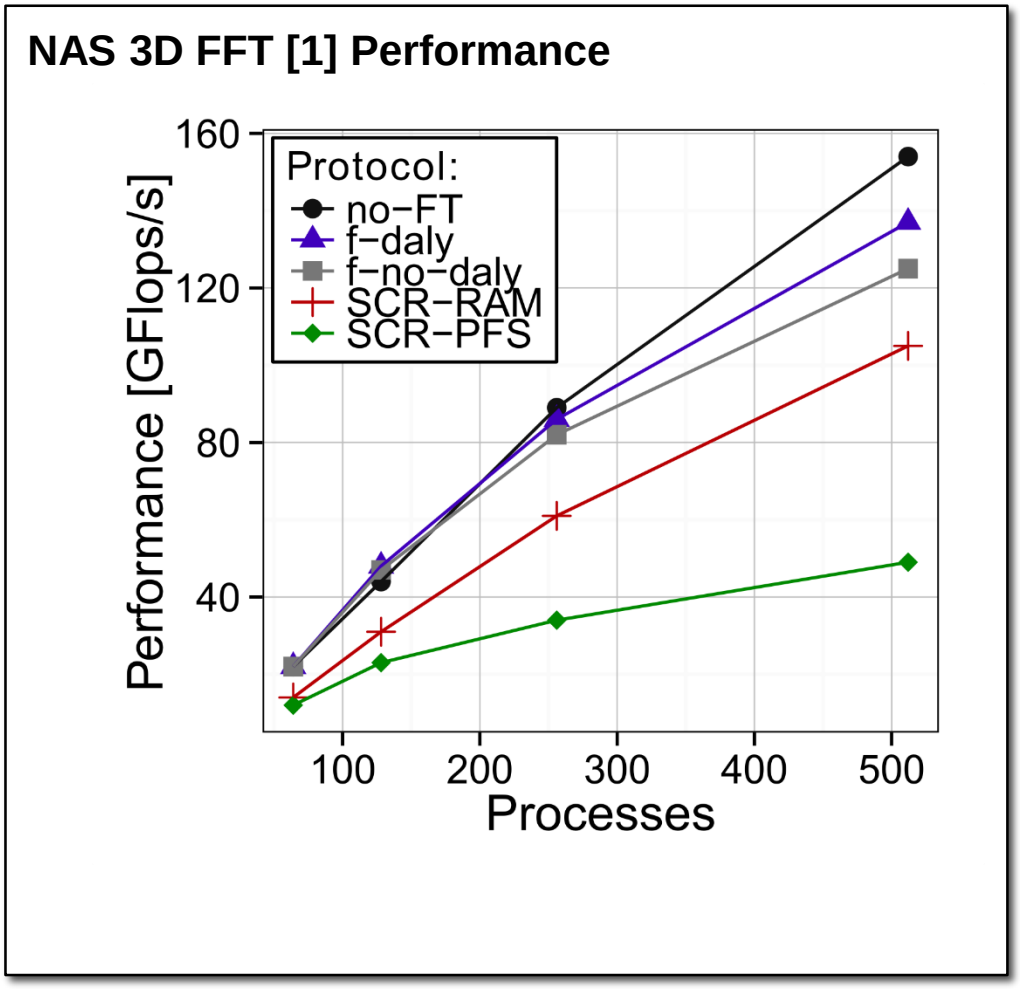
- Evaluation on CSCS Monte Rosa
  - 1,496 computing Cray XE6 nodes
  - 47,872 schedulable cores
  - 46TB memory
- 4 protocols
- 2 applications

Performance: Coordinated Checkpointing NAS 3D FFT



PERFORMANCE: COORDINATED CHECKPOINTING NAS 3D FFT





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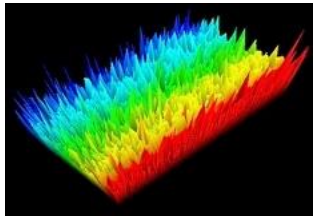

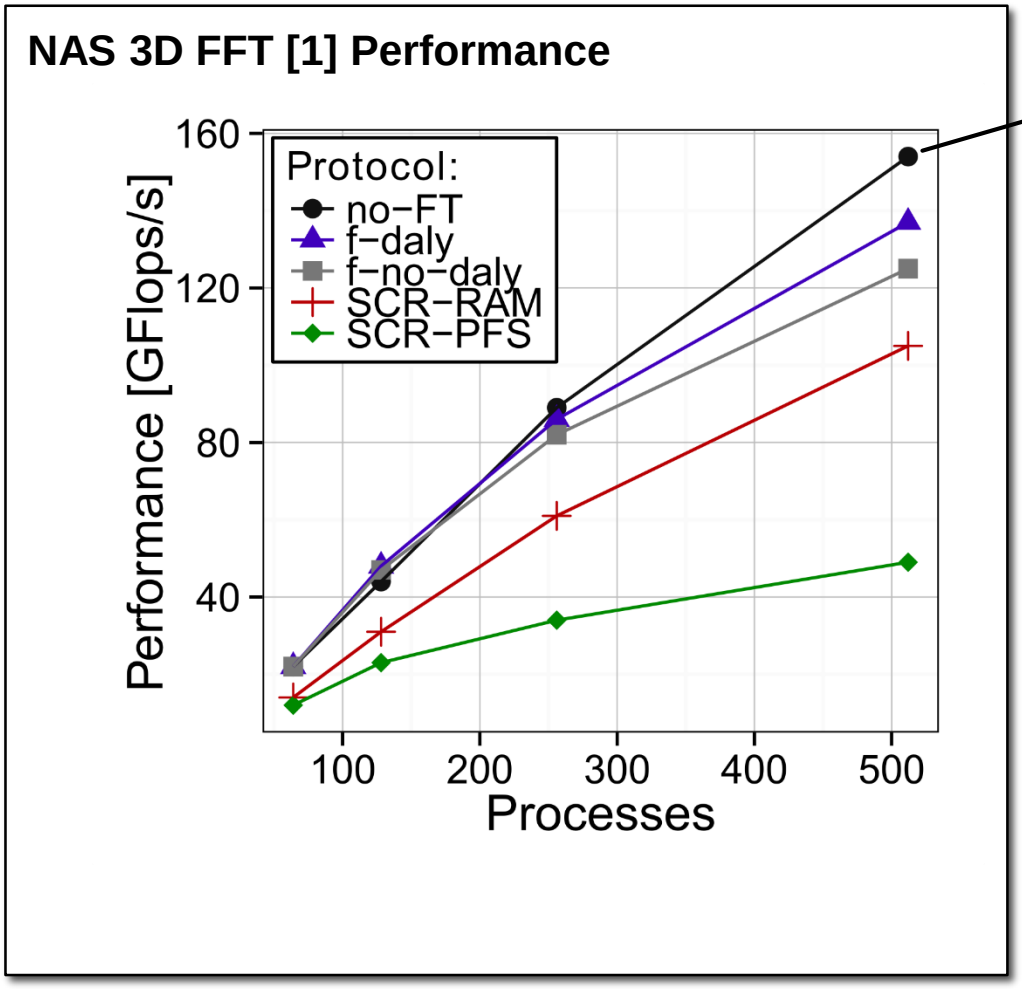

no-FT: no fault tolerance

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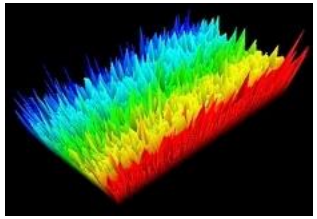

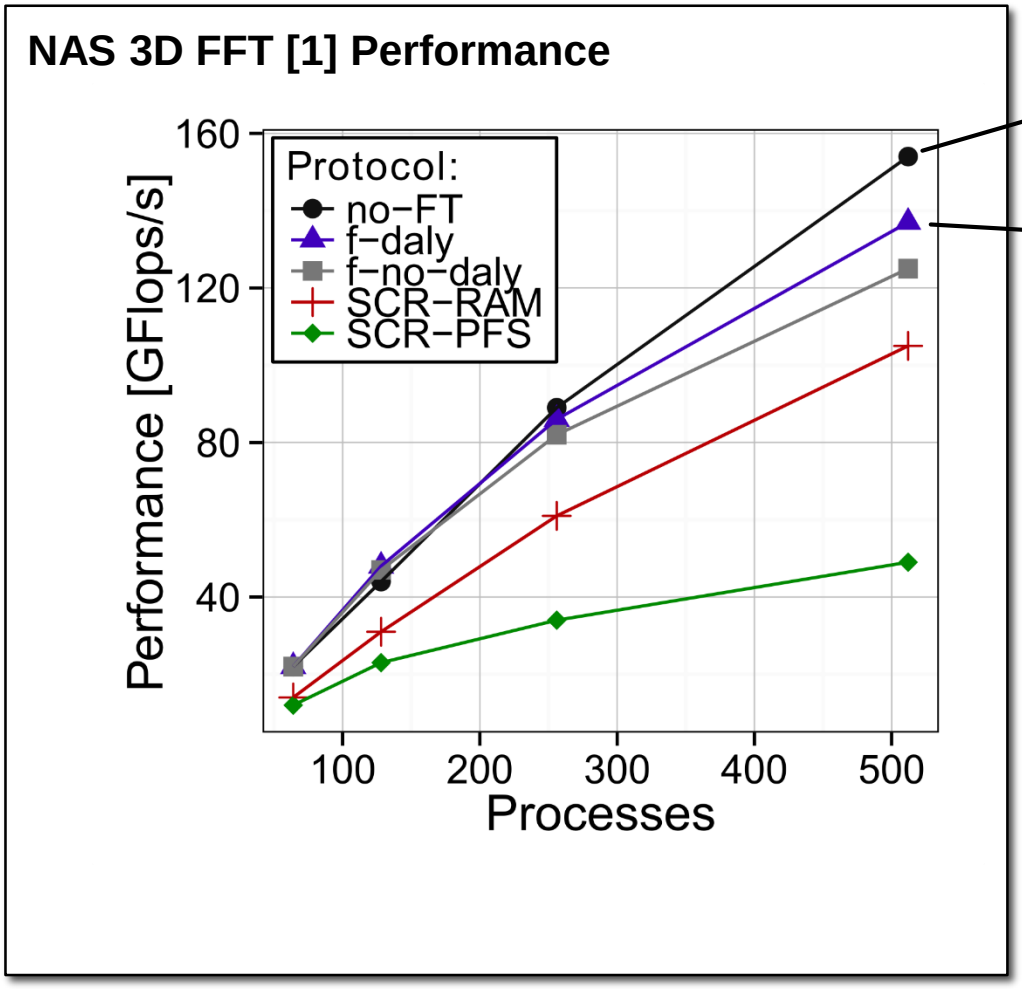

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f-daly: using Daly's interval
1-5% slower than no-FT

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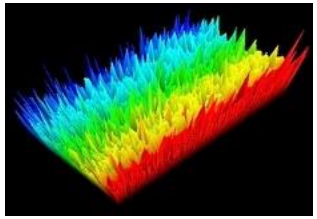

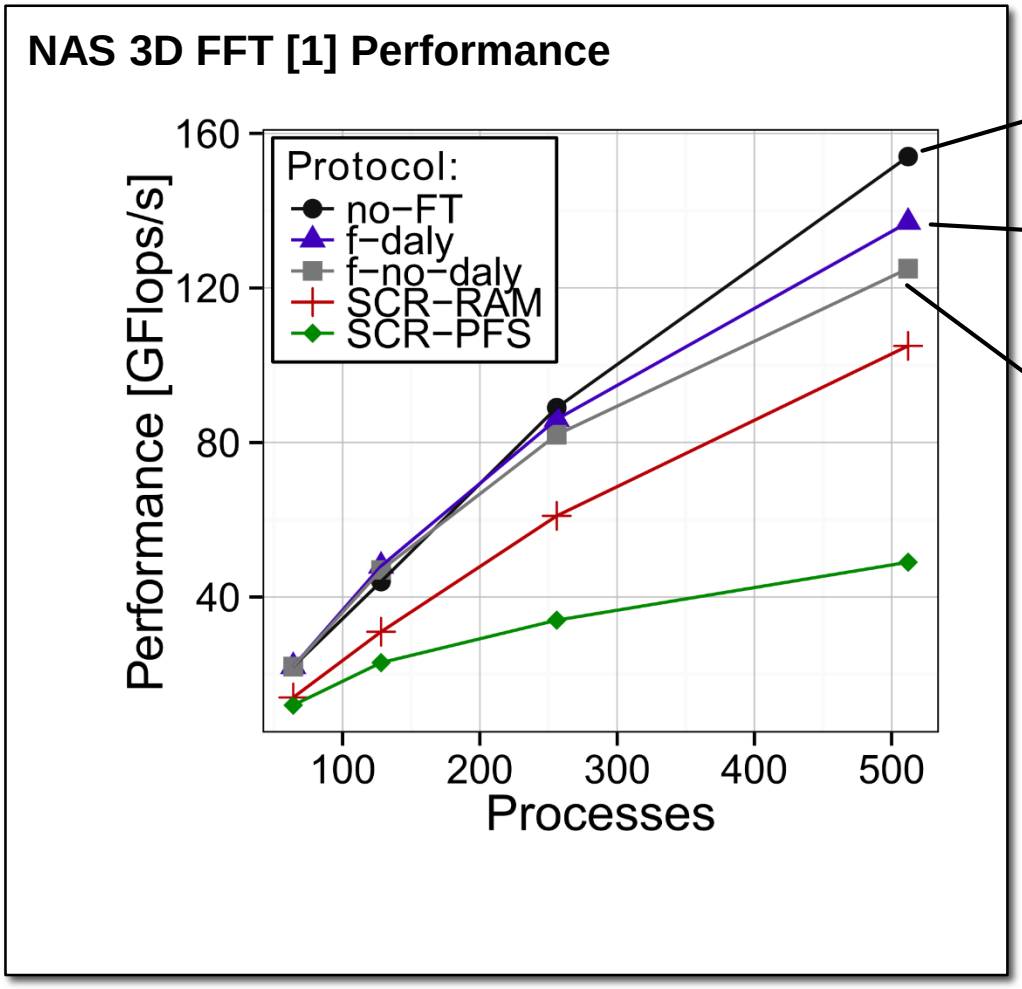

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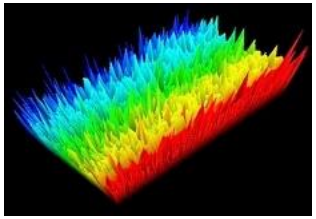

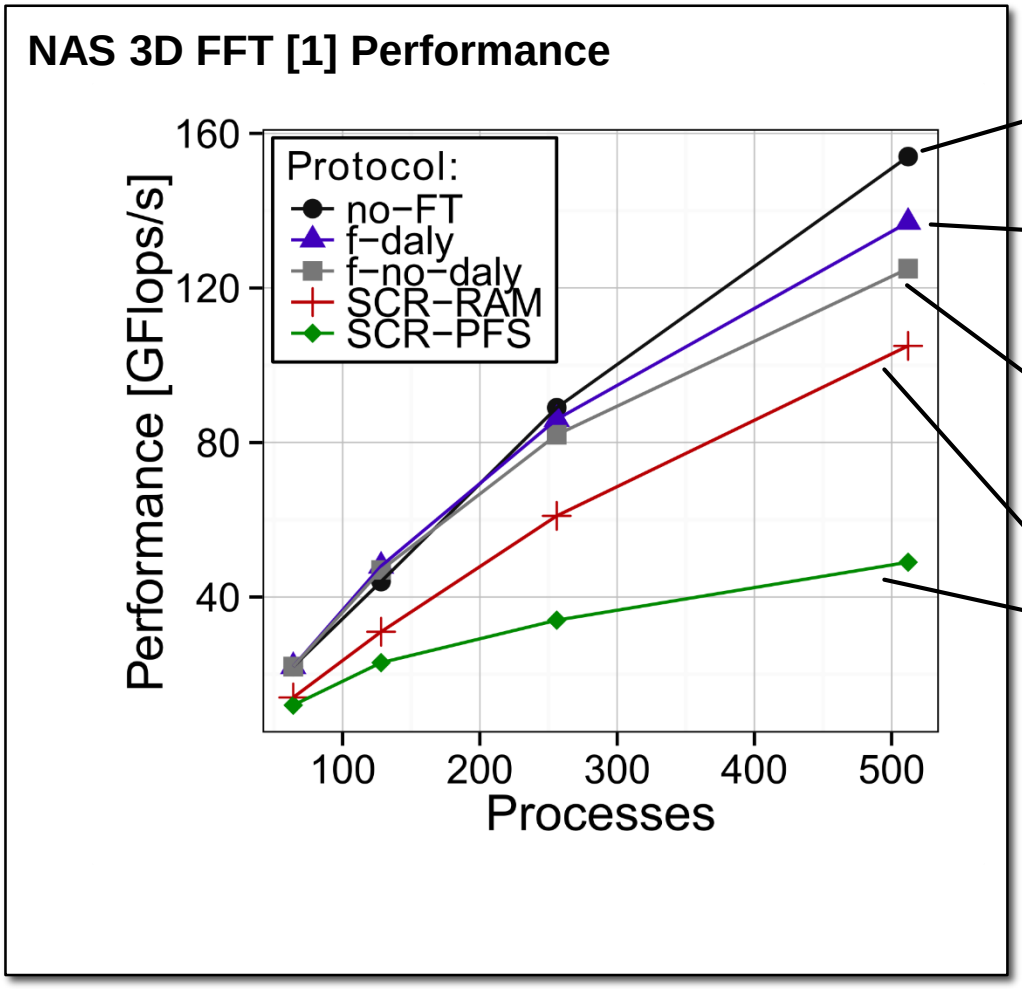

no-FT: no fault tolerance

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SCR: a popular checkpoint / restart library
21-67% slower than no-FT

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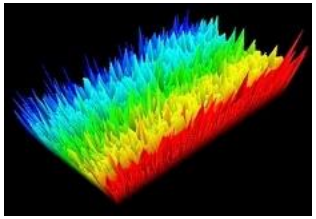
Performance: Uncoordinated Checkpointing NAS 3D FFT



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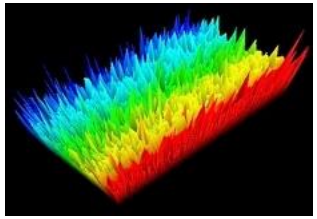

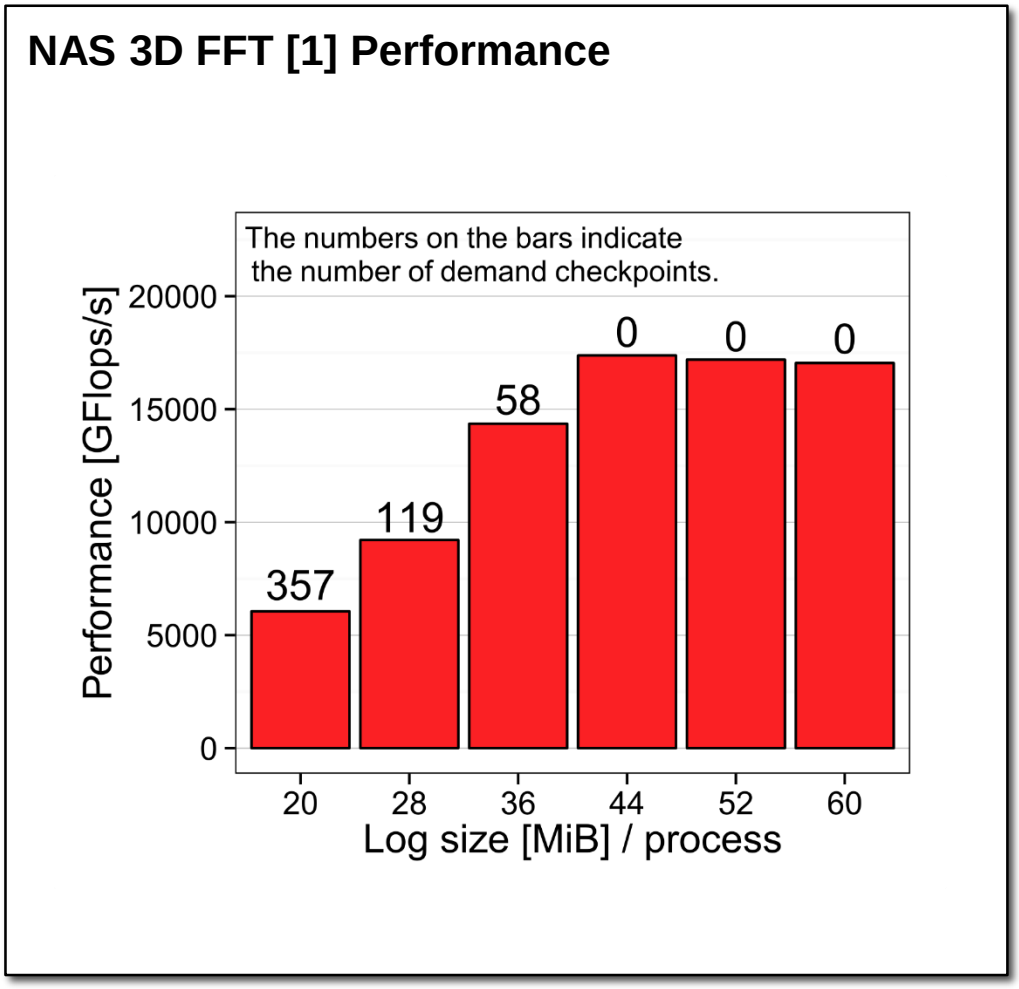

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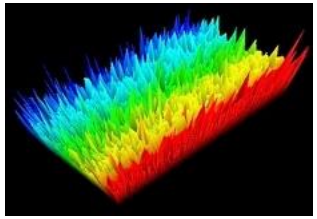

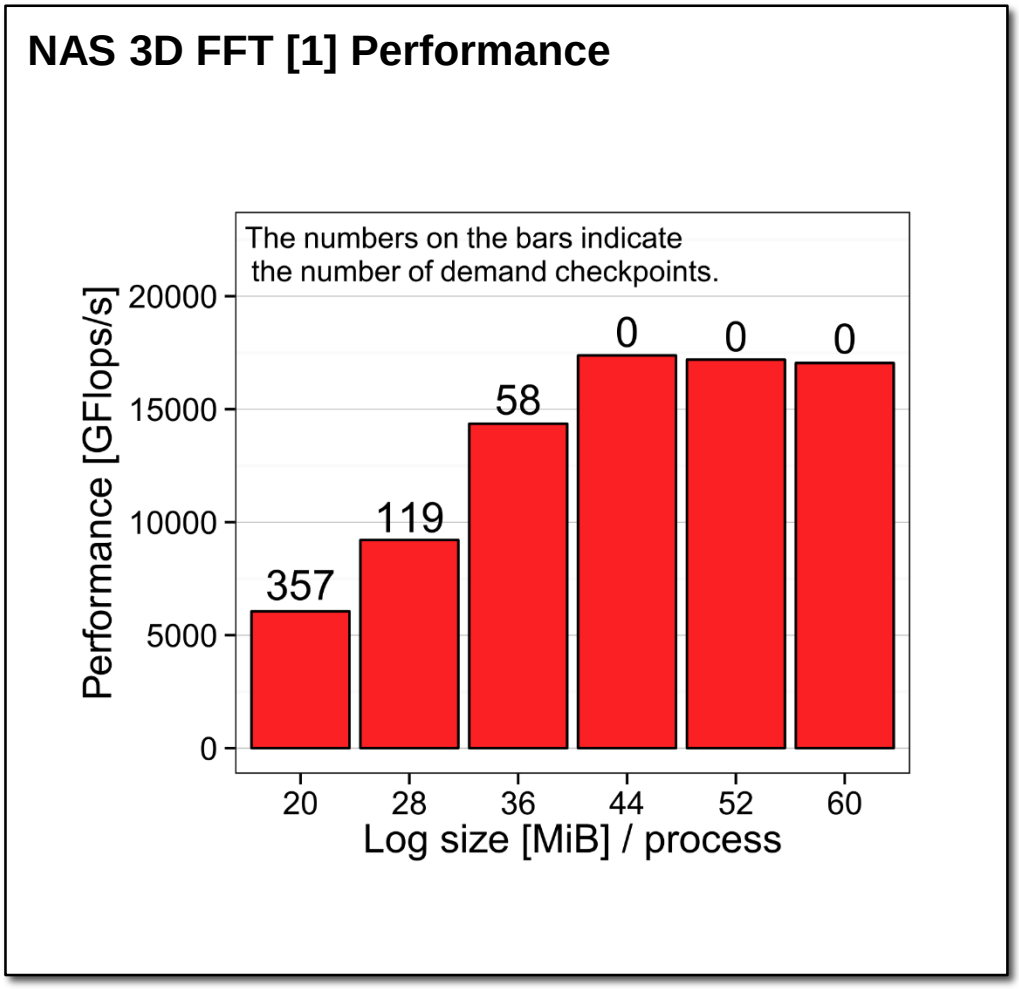

How the log size impacts the number of uncoordinated checkpoints and the performance of the code?

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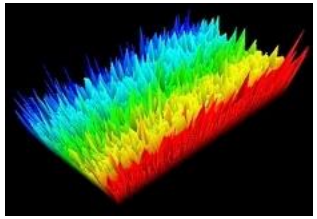

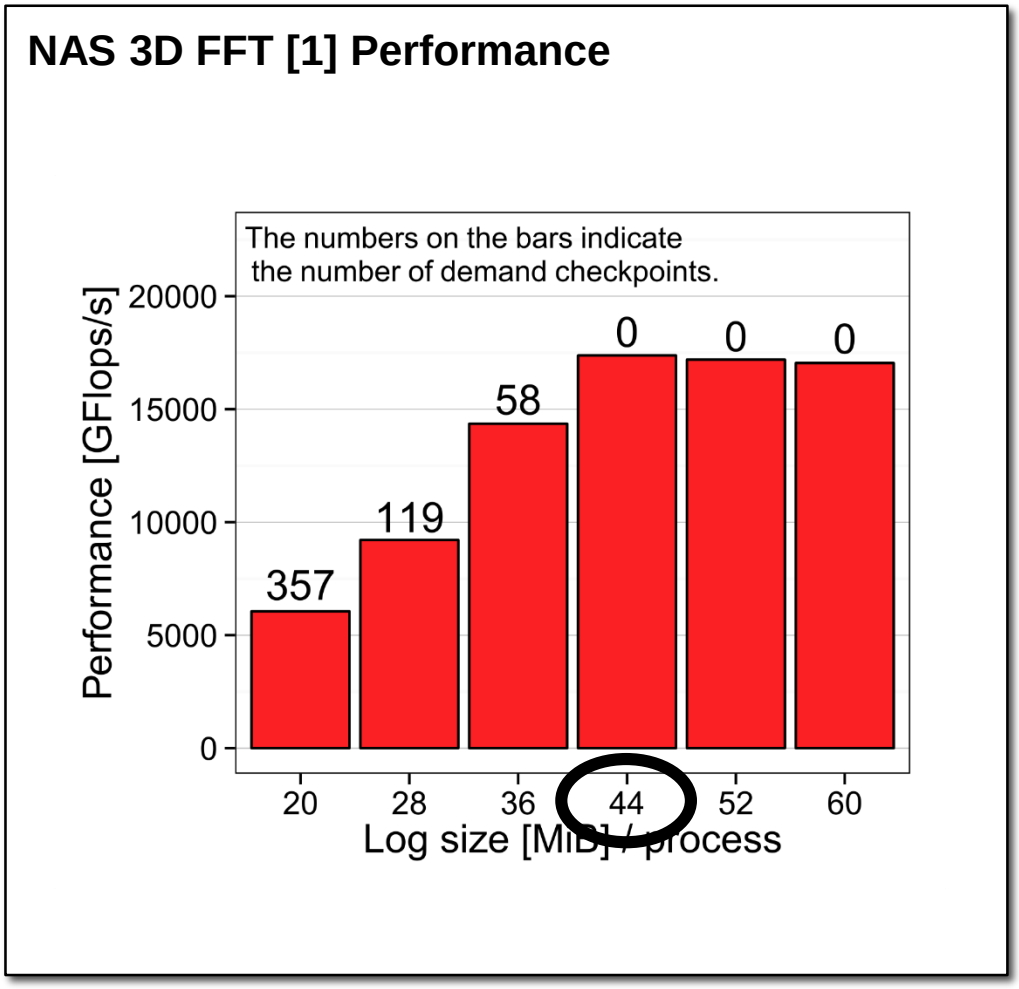

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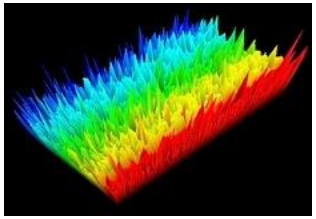

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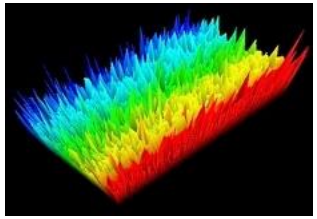

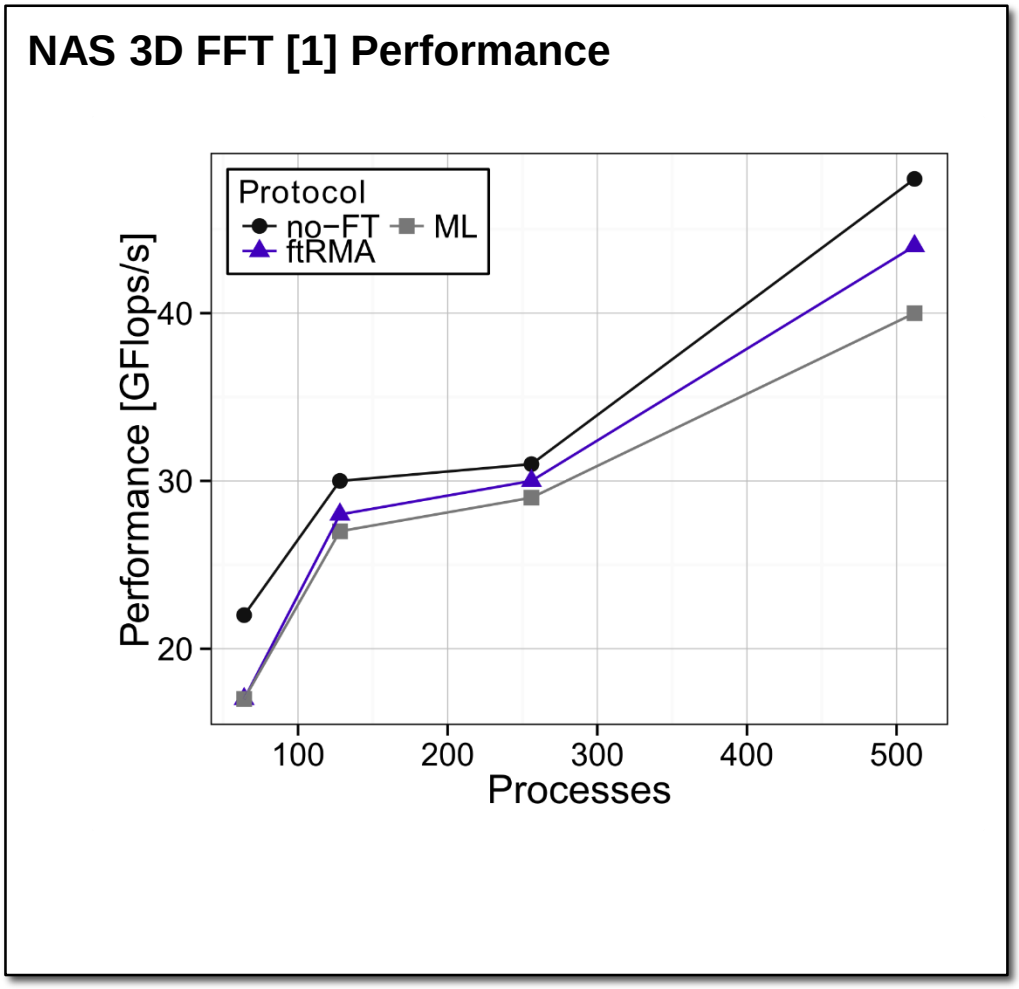

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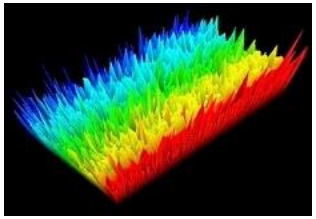

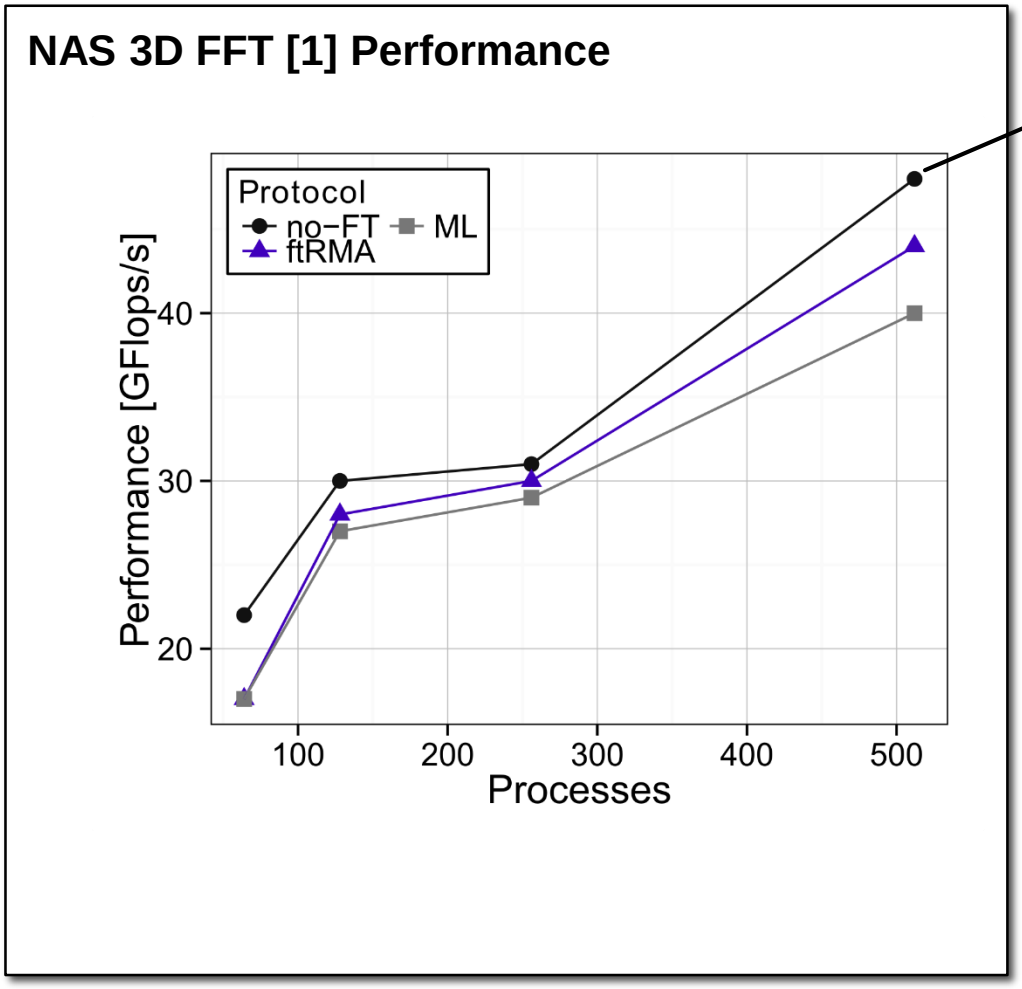

no-FT: no fault tolerance

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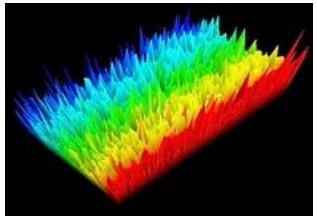

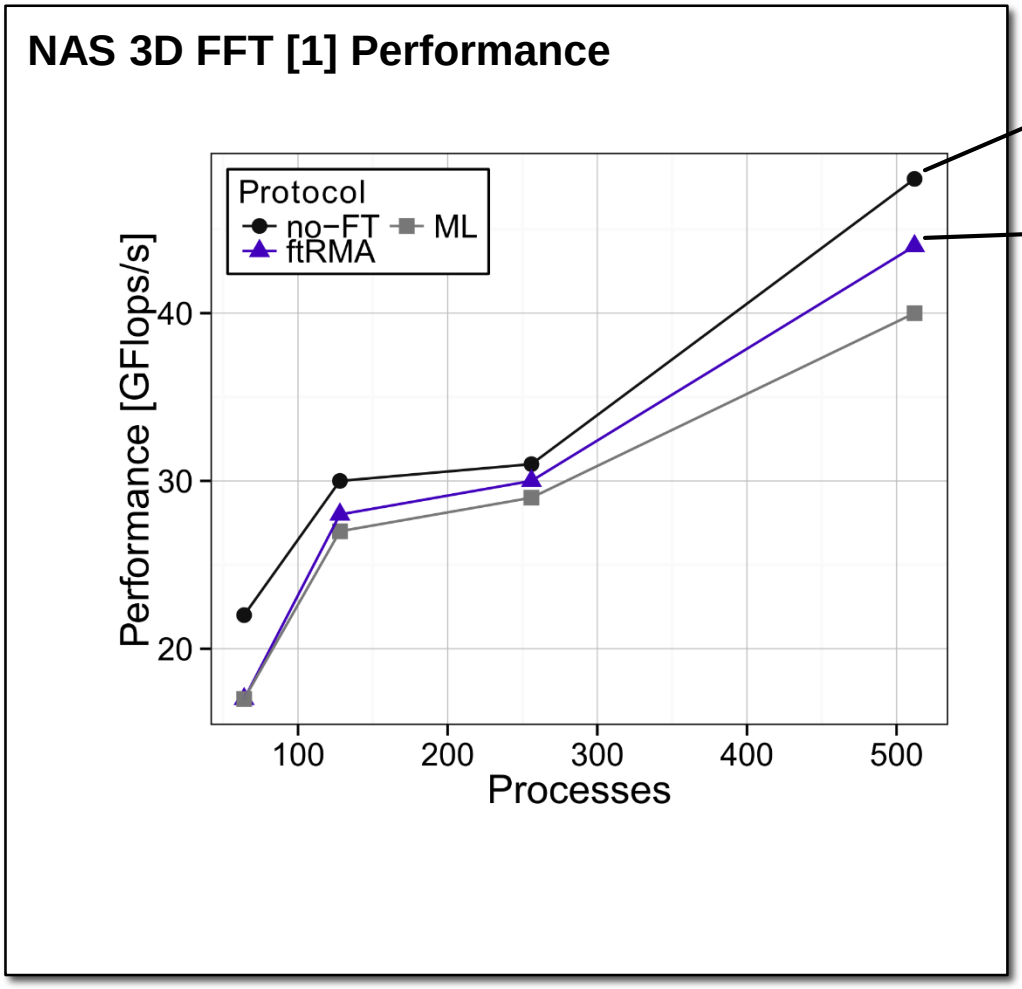

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FTRMA: logging puts (FFT code does not use gets)
8-9% slower than no-FT

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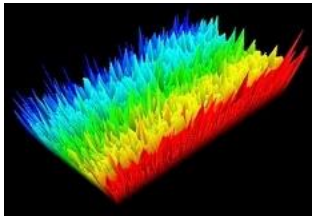

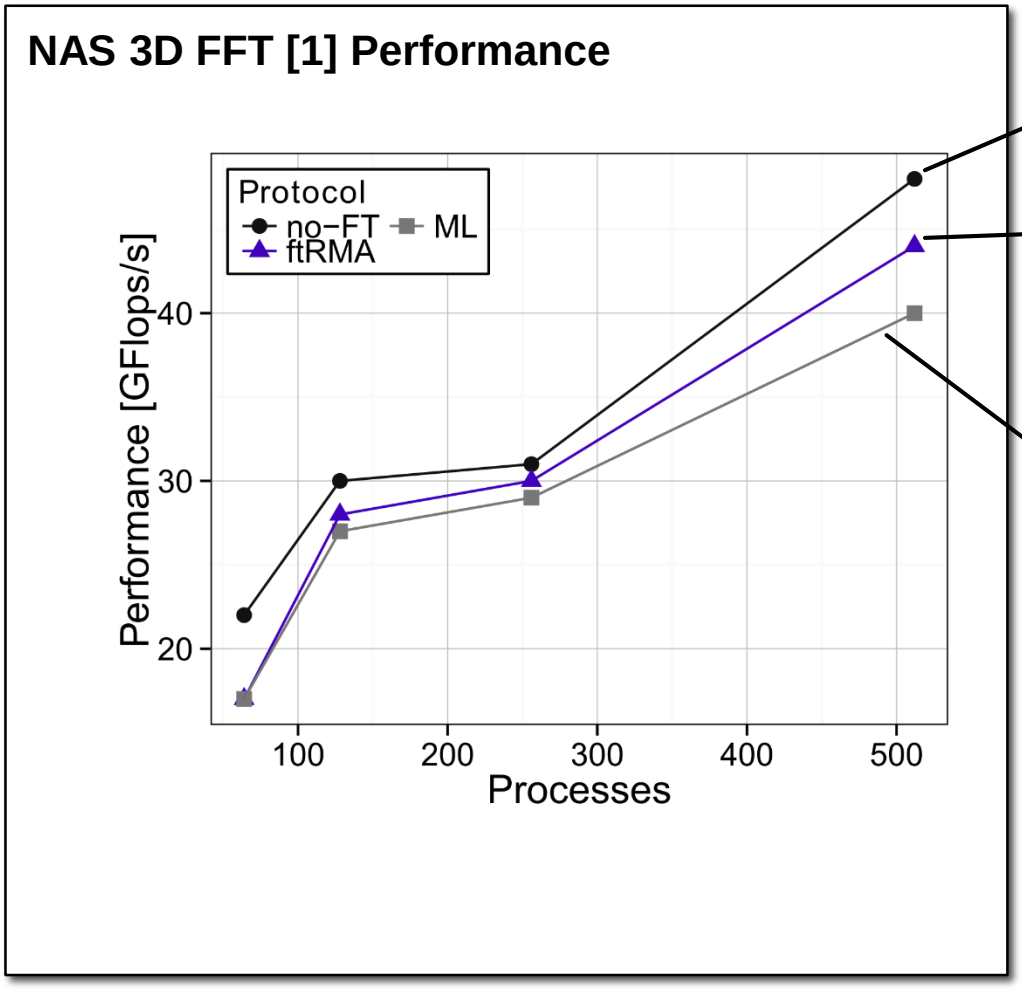

no-FT: no fault tolerance

FTRMA: logging puts (FFT code does not use gets) 8-9% slower than no-FT

ML: a simple protocol based on message logging 18% slower than no-FT

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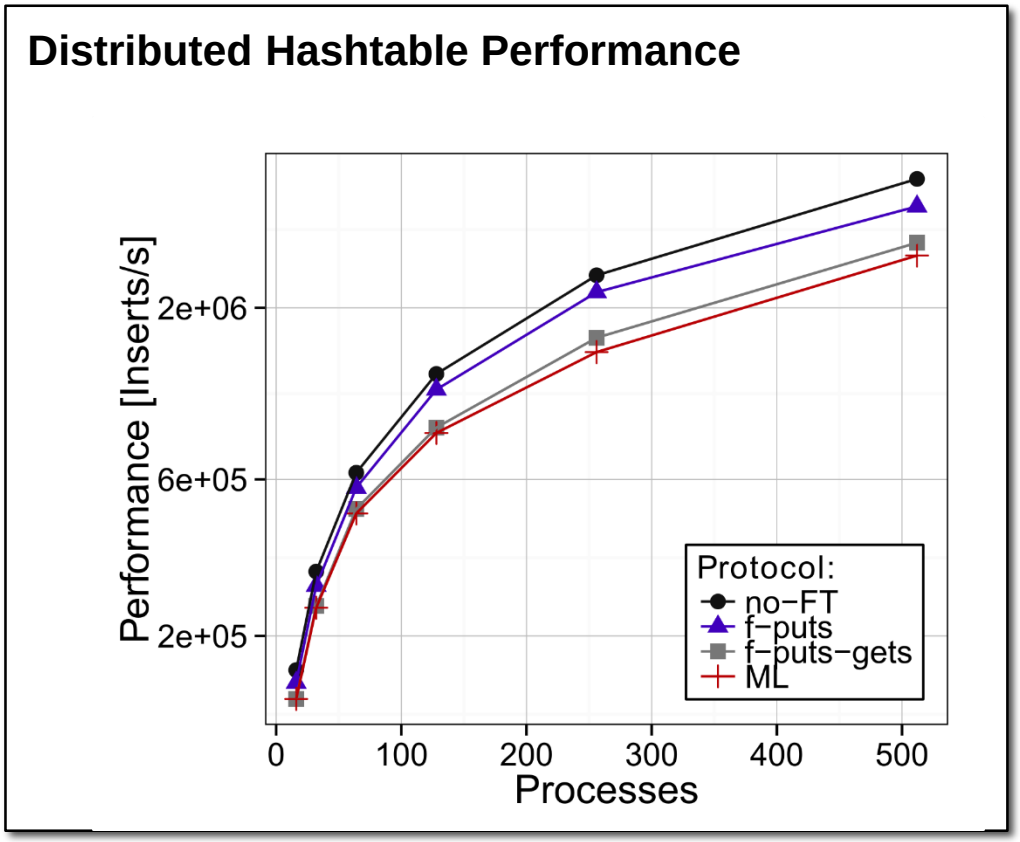
Performance: Access Logging
Distributed Hashtable

PERFORMANCE: ACCESS LOGGING
DISTRIBUTED HASHTABLE



Performance: Access Logging
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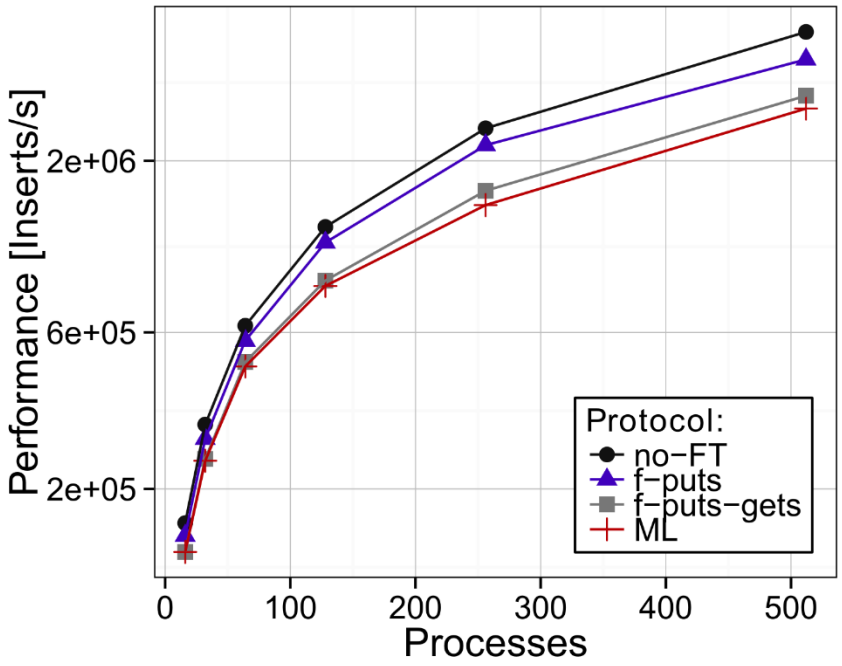
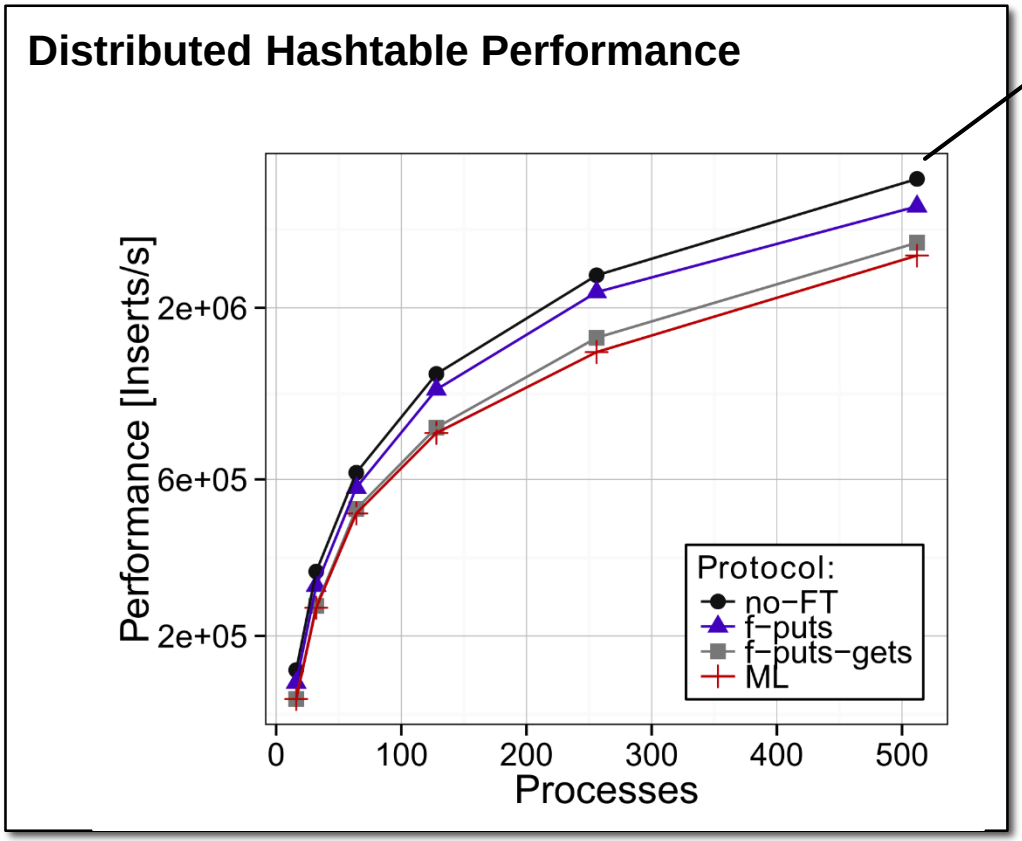
Distributed Hashtable Performance



An insert: 1 get and 1 put are logged
A collision: 4 gets and 6 puts are logged

Performance: Access Logging
Distributed Hashtable



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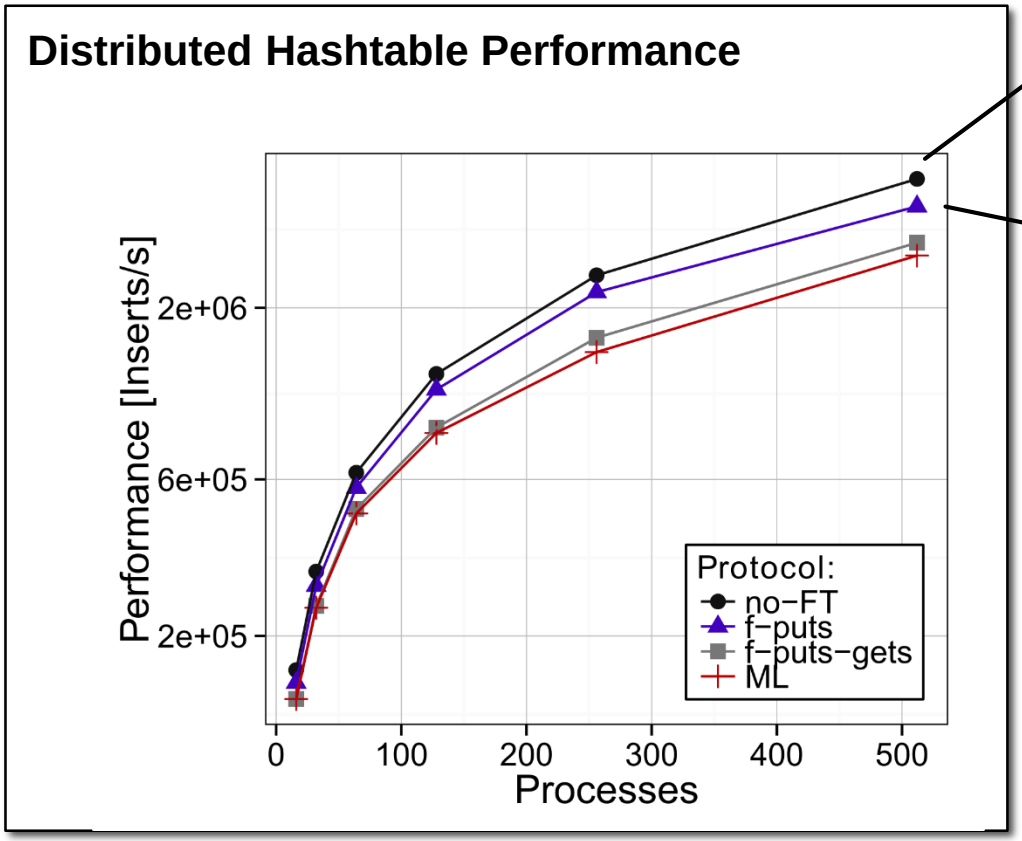

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f-puts: logging puts
12% slower than no-FT

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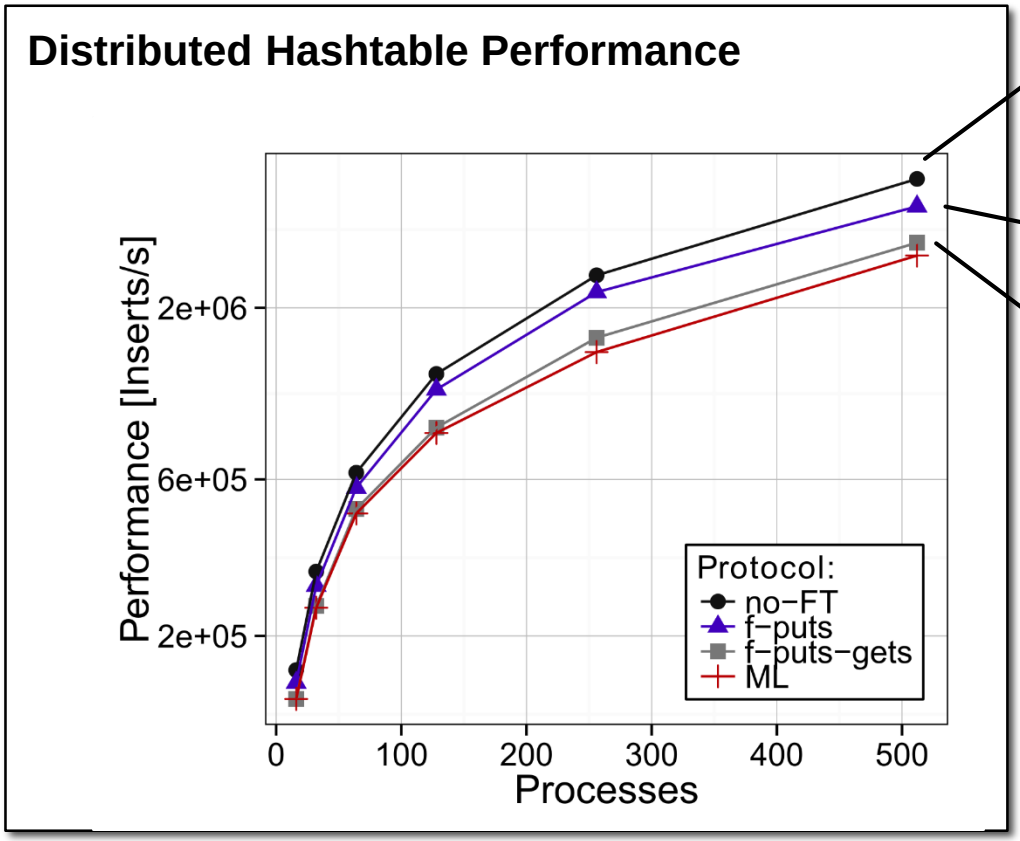

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f-puts-gets: logging puts and gets
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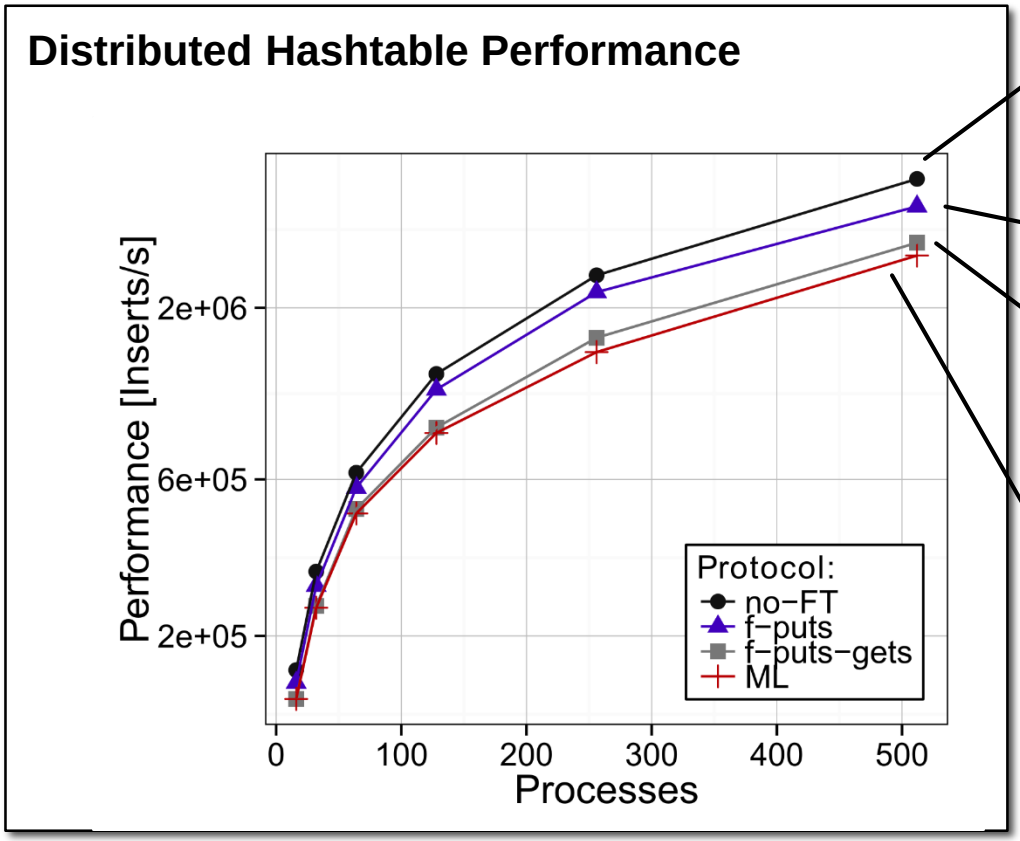

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f-puts: logging puts
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f-puts-gets: logging puts and gets
33% slower than no-FT

ML: logging puts and gets
40% slower than no-FT

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Overview of our Research

Generic model

$\mathcal{D} = \langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co} \rangle,$

$\mathrm{PUT}(p \rightrightarrows q)$
$\mathrm{GET}(p \leftrightarrows q)$

MPI-2
PGAS

CC in RMA

MP vs. RMA

Schemes

Recovery in RMA

Basic scheme

Extended RMA semantics

Proofs

Theorem 4.2. *The recove rithm 2 preserves the* $\xrightarrow{cohb}$ *or ferred to as the* gsync order*).*

Deadlock freedom
Correct recovery

Holistic fault-tolerance library

Design

Checkpoints on demand

Optimizations

Performance

UC in RMA

MP vs. RMA

Checkpointing schemes

Logging accesses

Topology-awareness

$\langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \mathcal{H}, \mathcal{G}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co}, \mathcal{M} \rangle$

Model extensions

Distribution of processes

Decreasing failure prob.

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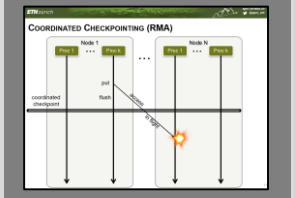

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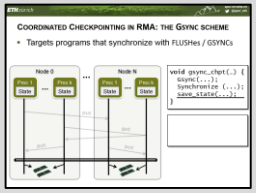

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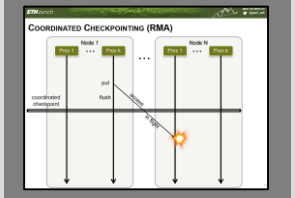

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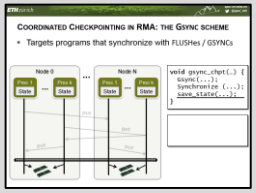

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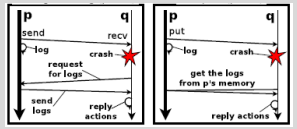

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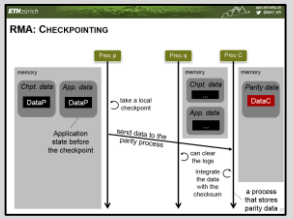

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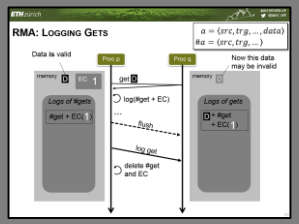

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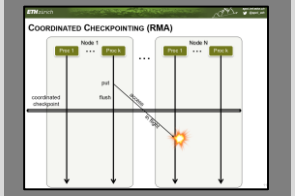

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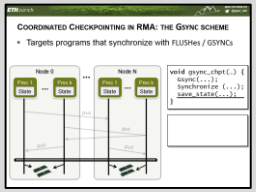

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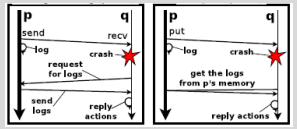

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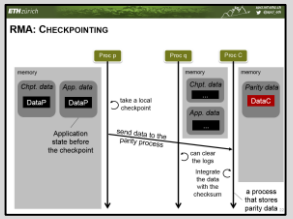

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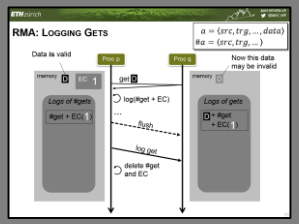

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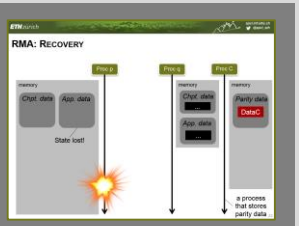

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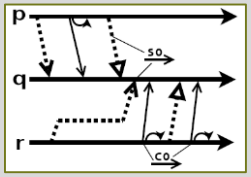

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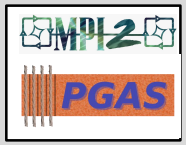

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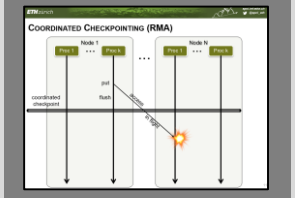

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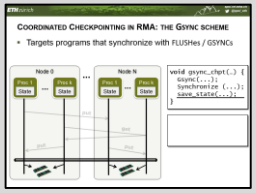

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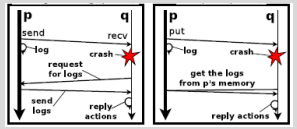

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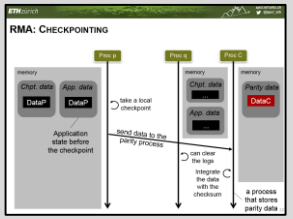

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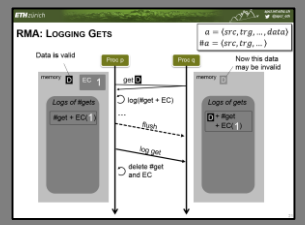

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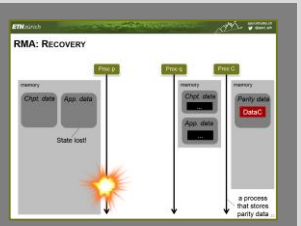

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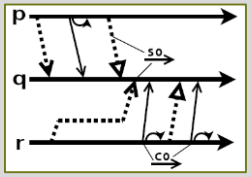

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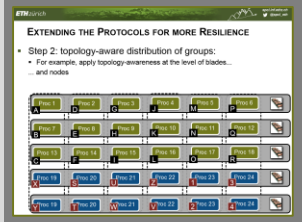

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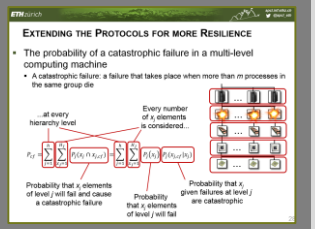

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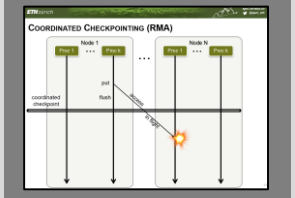

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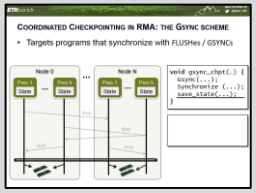

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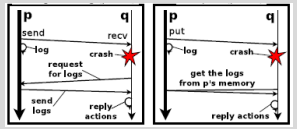

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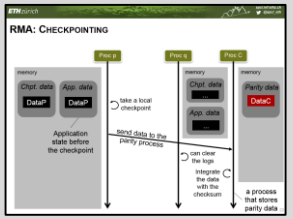

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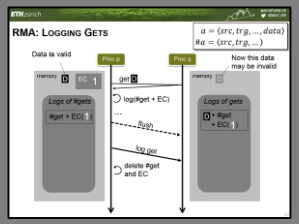

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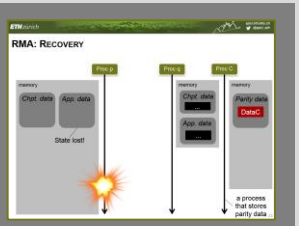

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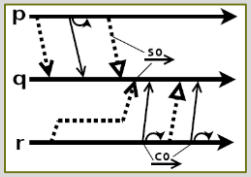

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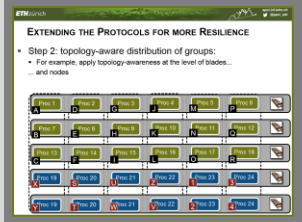

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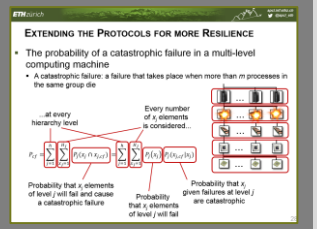

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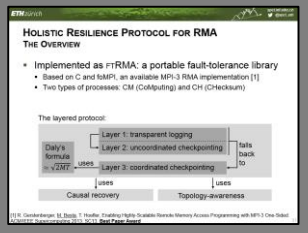

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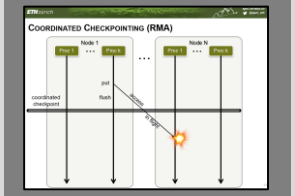

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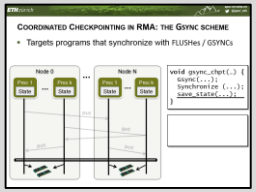

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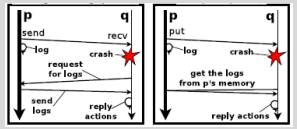

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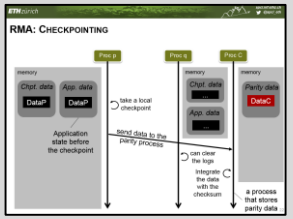

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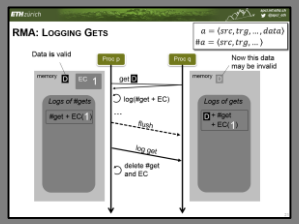

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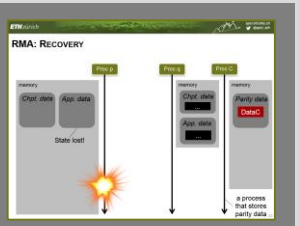

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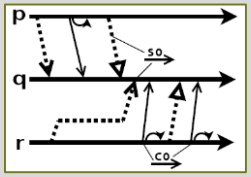
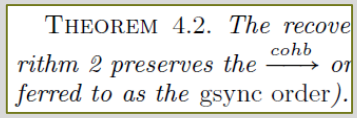


Proofs



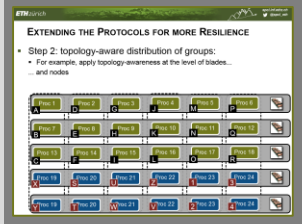
THEOREM 4.2. *The recove rithm 2 preserves the* $\xrightarrow{cohb}$ *or ferred to as the* gsync order*).*

Deadlock freedom
Correct recovery

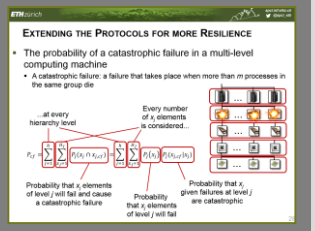
Topology-awareness

$\langle \mathcal{P}, \mathcal{E}, \mathcal{S}, \mathcal{H}, \mathcal{G}, \xrightarrow{po}, \xrightarrow{so}, \xrightarrow{hb}, \xrightarrow{co}, \mathcal{M} \rangle$

Model extensions

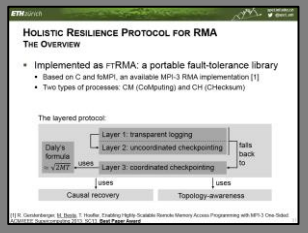


Distribution of processes



Decreasing failure prob.

Holistic fault-tolerance library



Design

Checkpoints on demand

Optimizations

Performance

ACKNOWLEDGMENTS

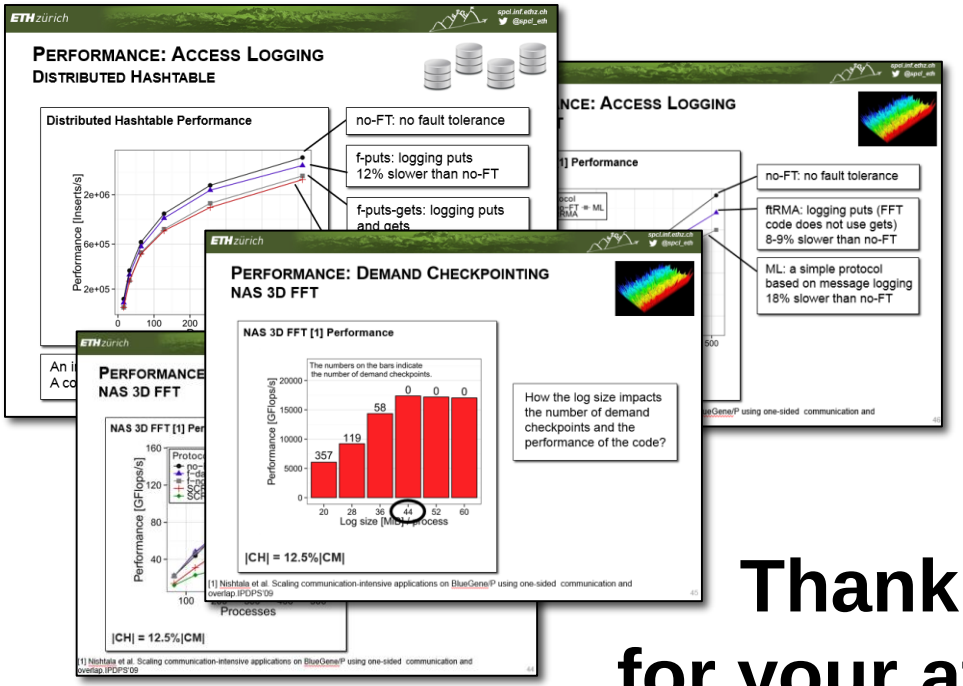
Thanks to:

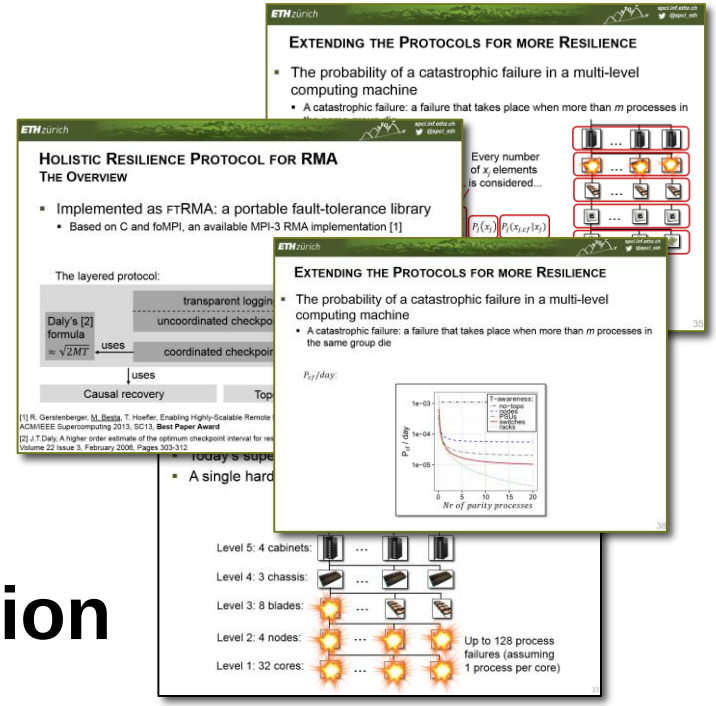
Paul Hargrove (and the whole UPC team)
and the MPI Forum RMA WG …

… and the institutions:

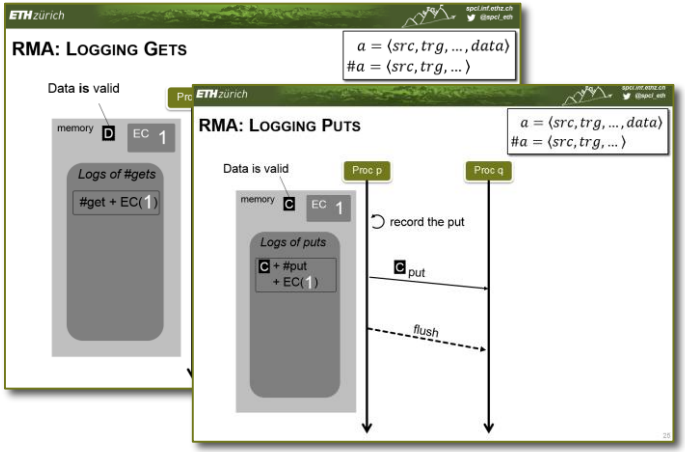
CSCS

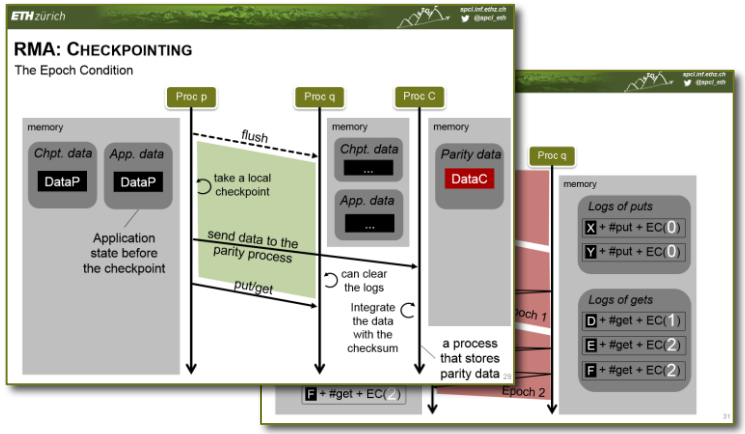
Google™



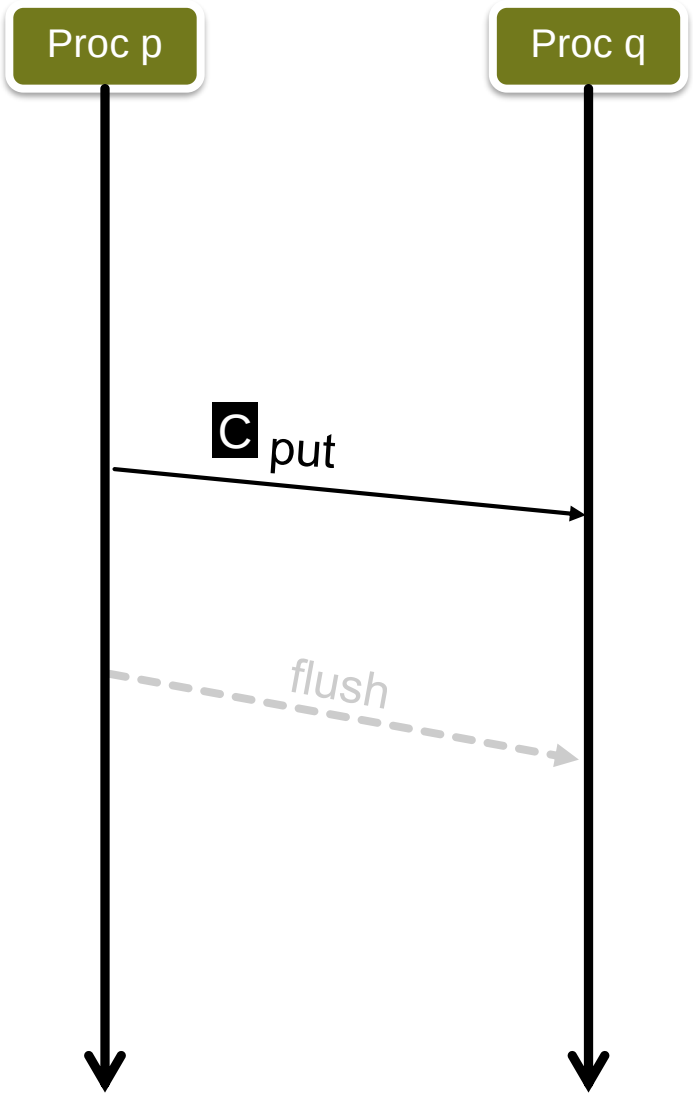


Thank you for your attention





RMA: Logging Puts



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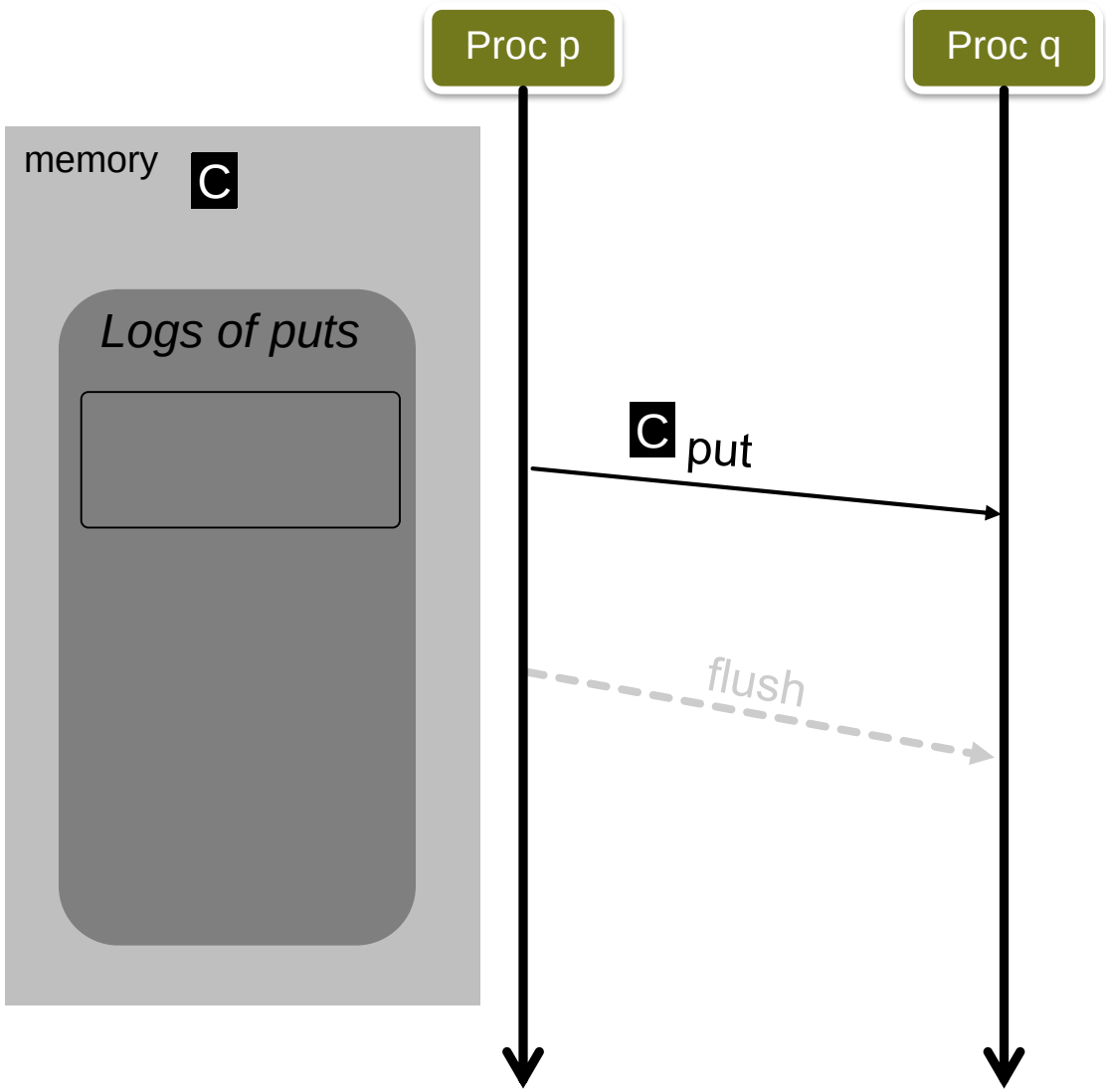

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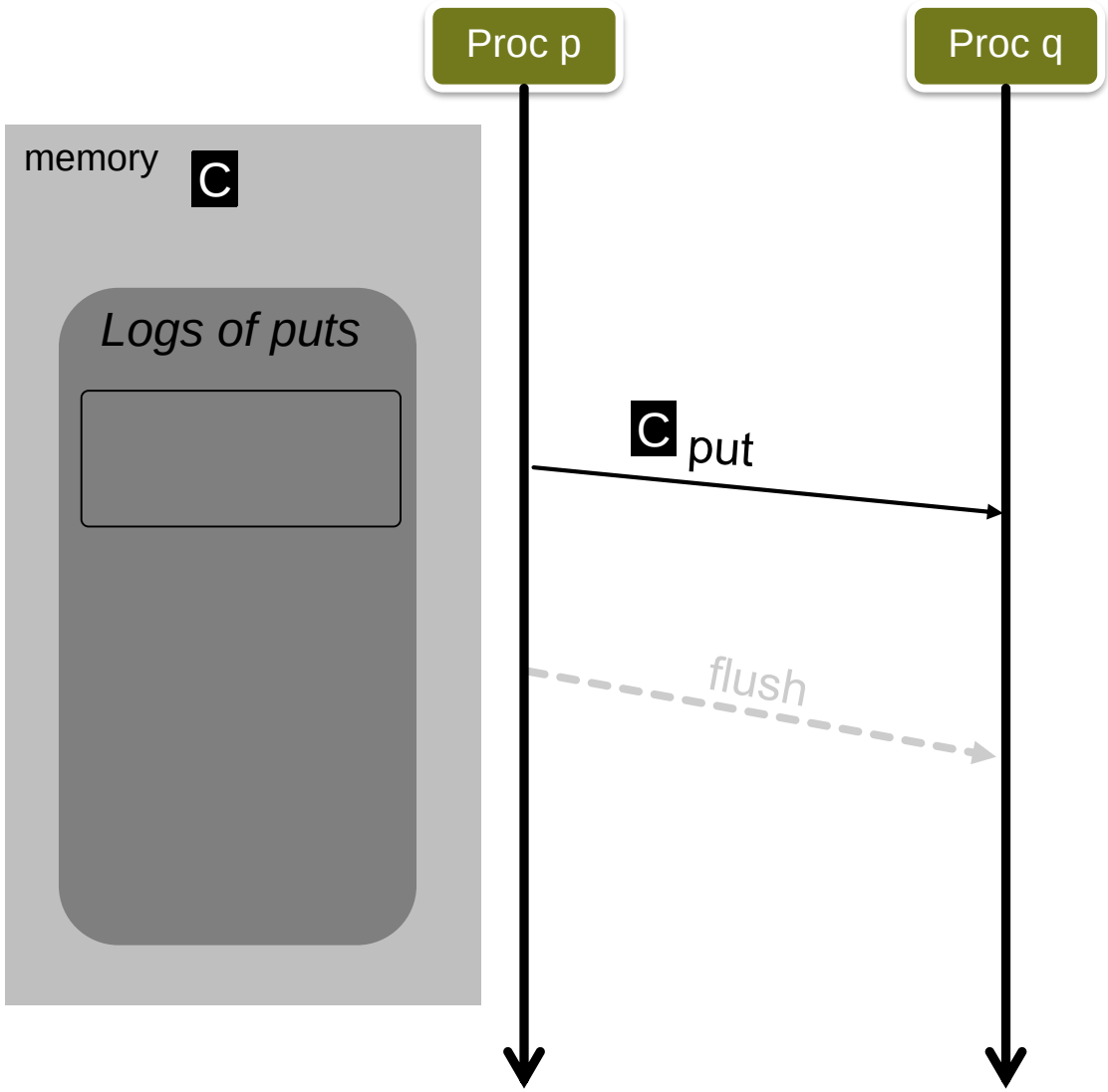

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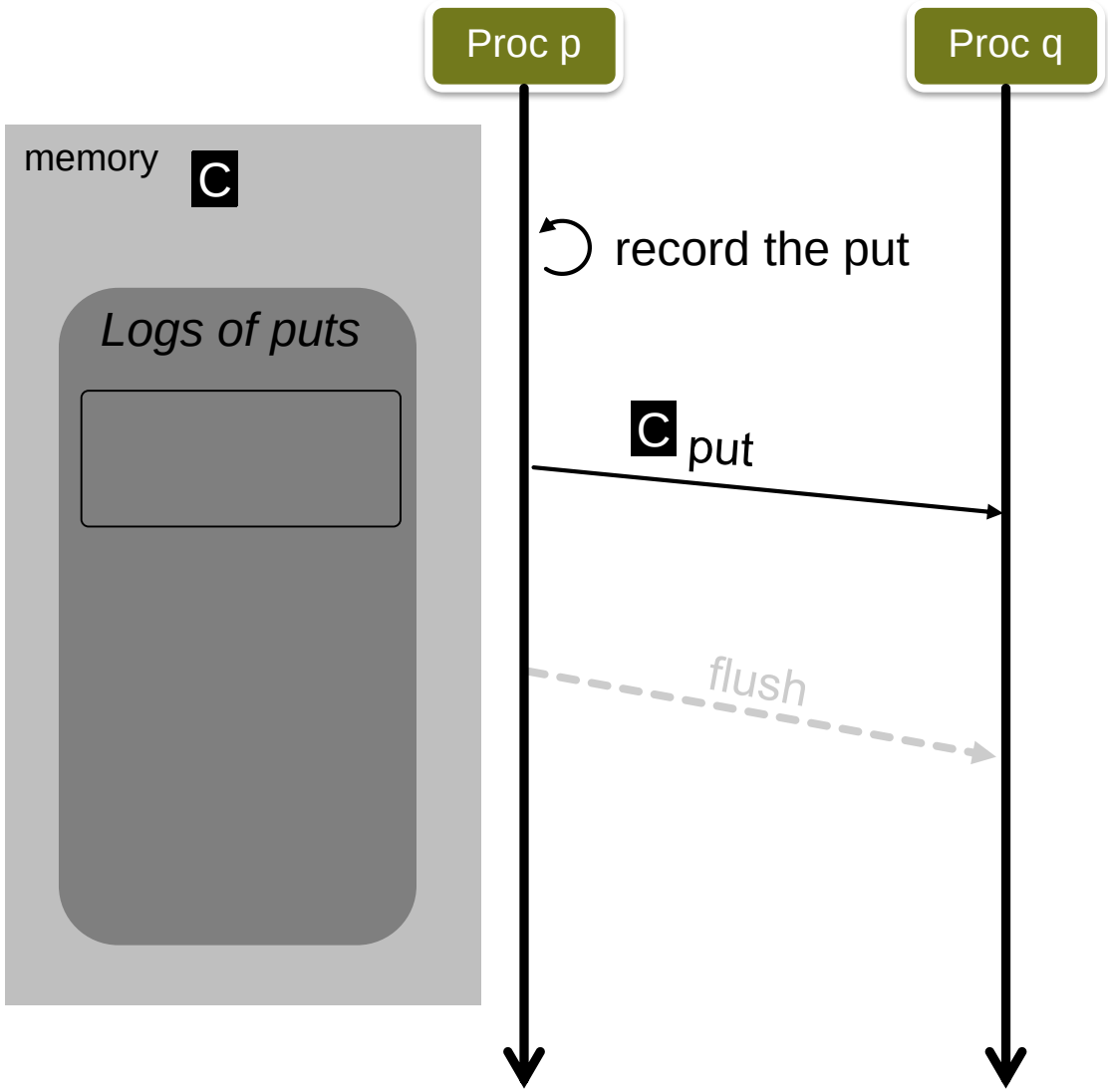

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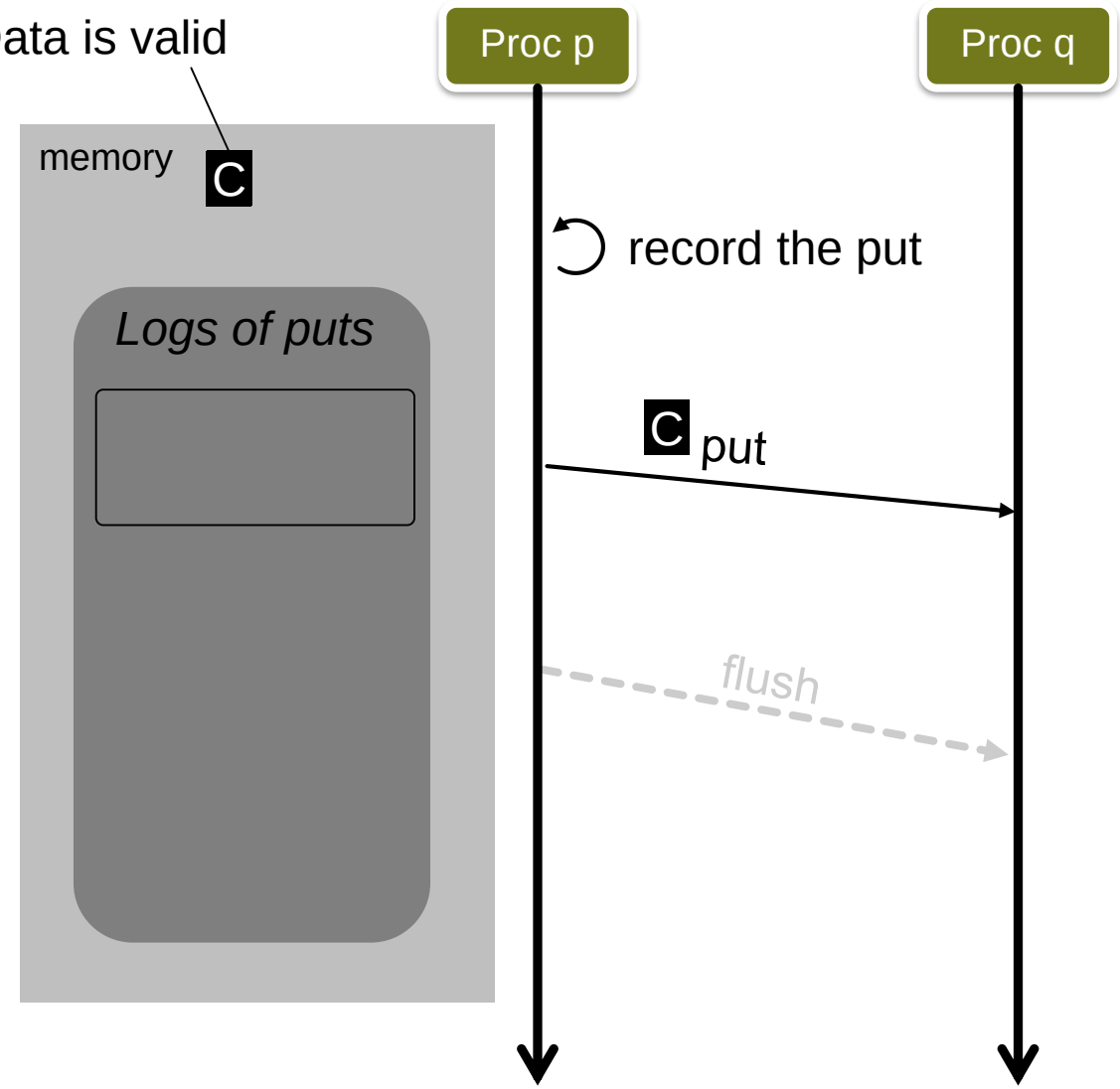

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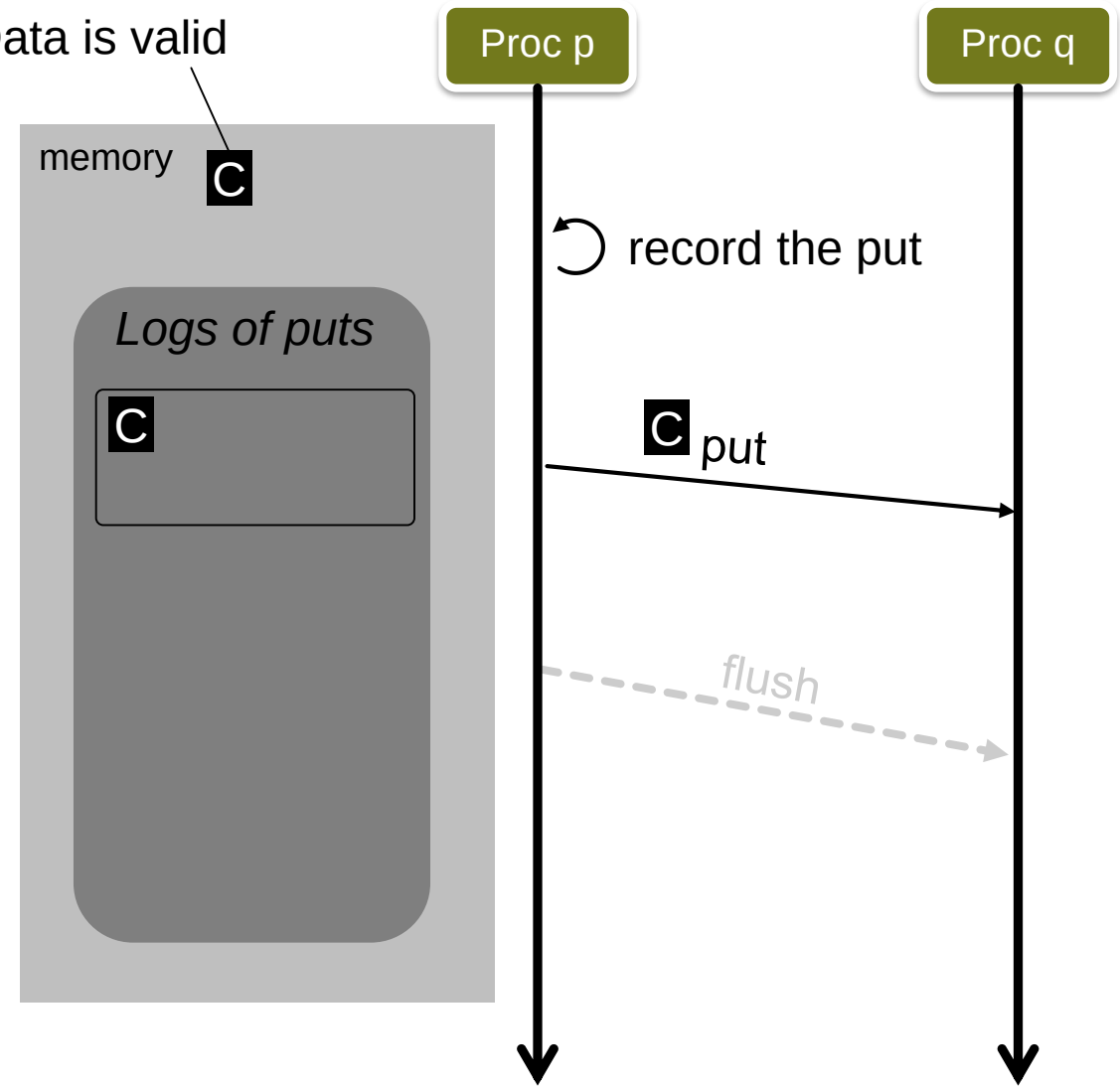

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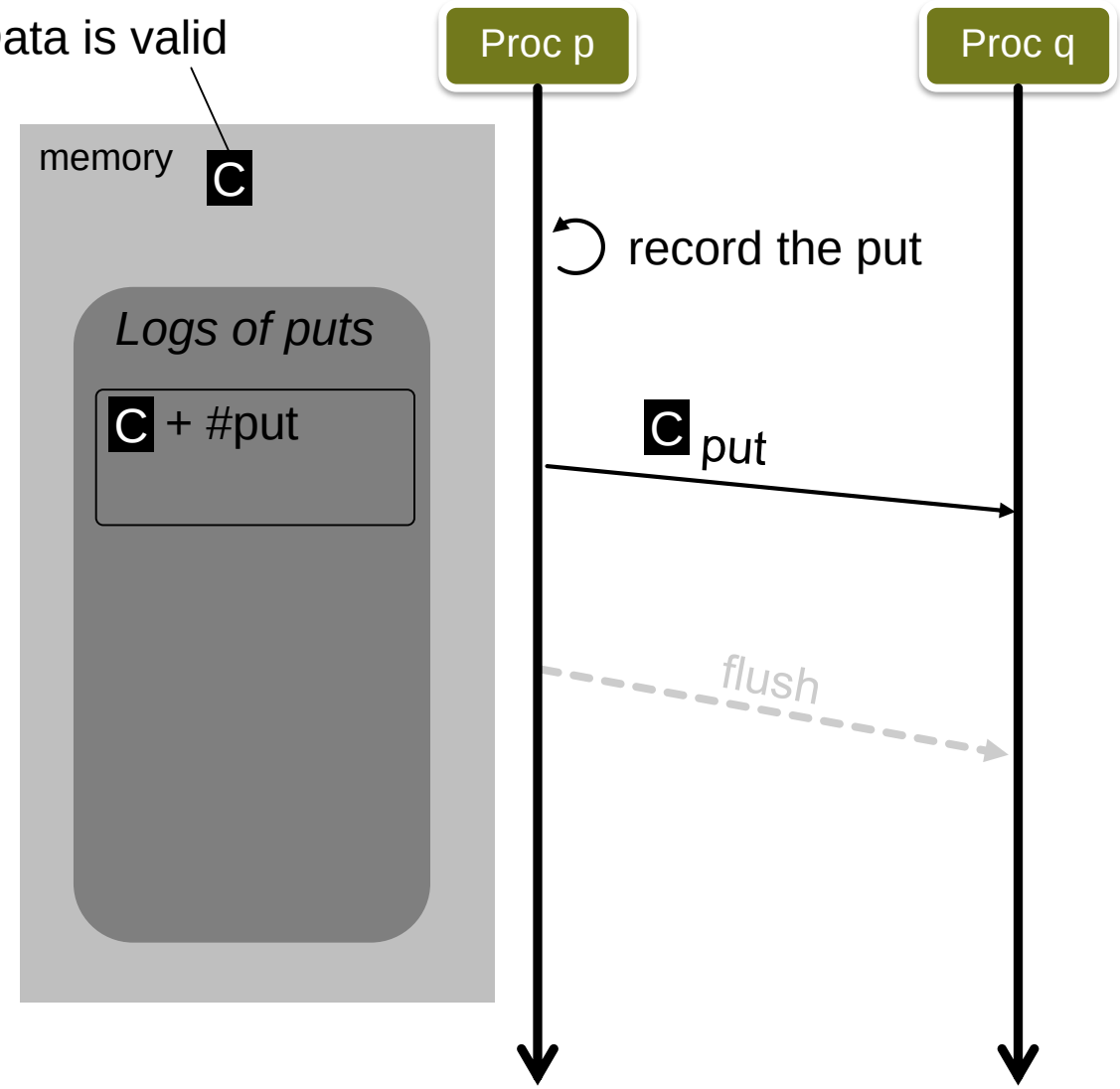

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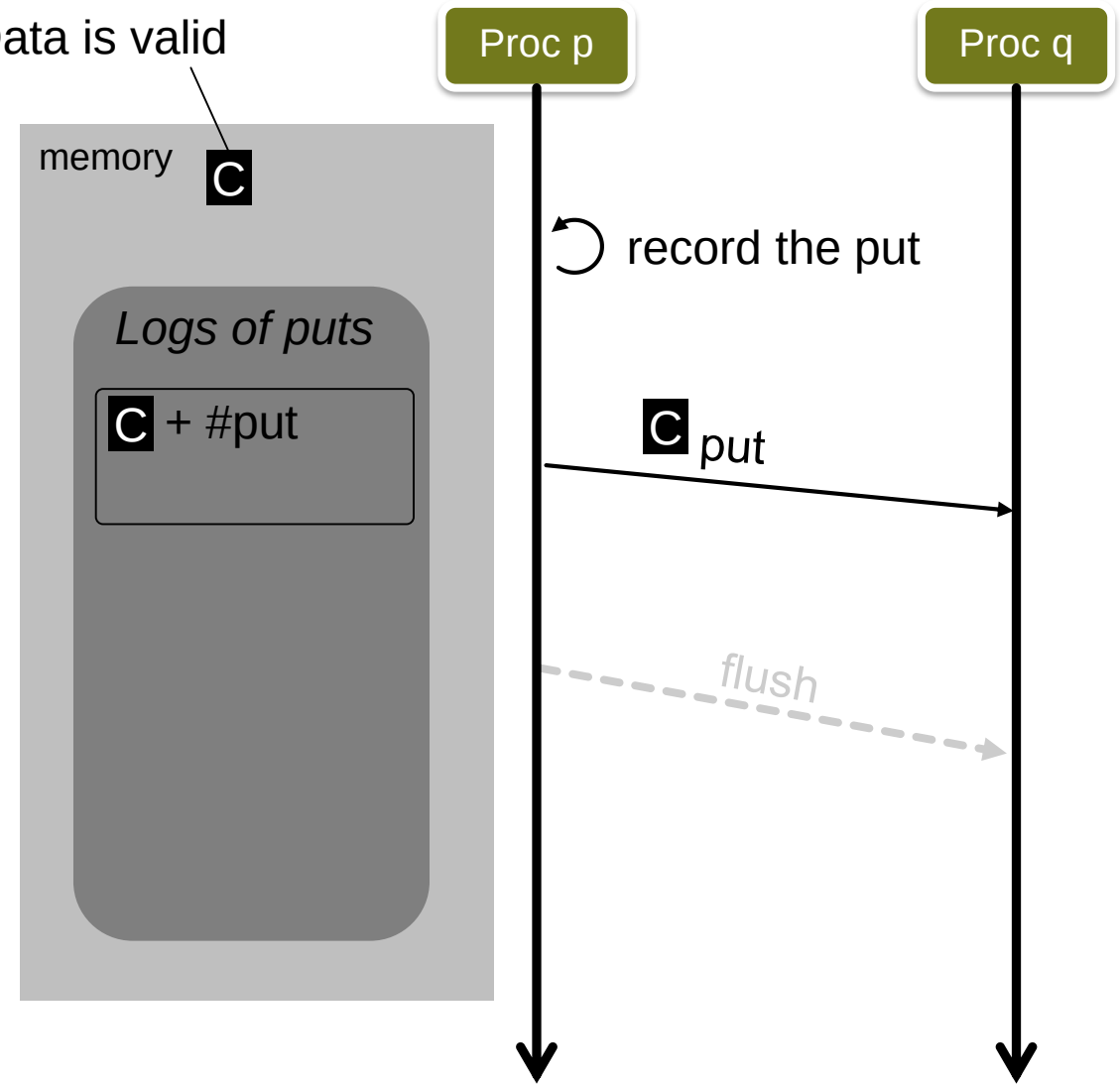

To replay the actions preserving $\xrightarrow{co}$, we also record **epoch counters**

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$$a = \langle src, trg, \dots, data \rangle$$
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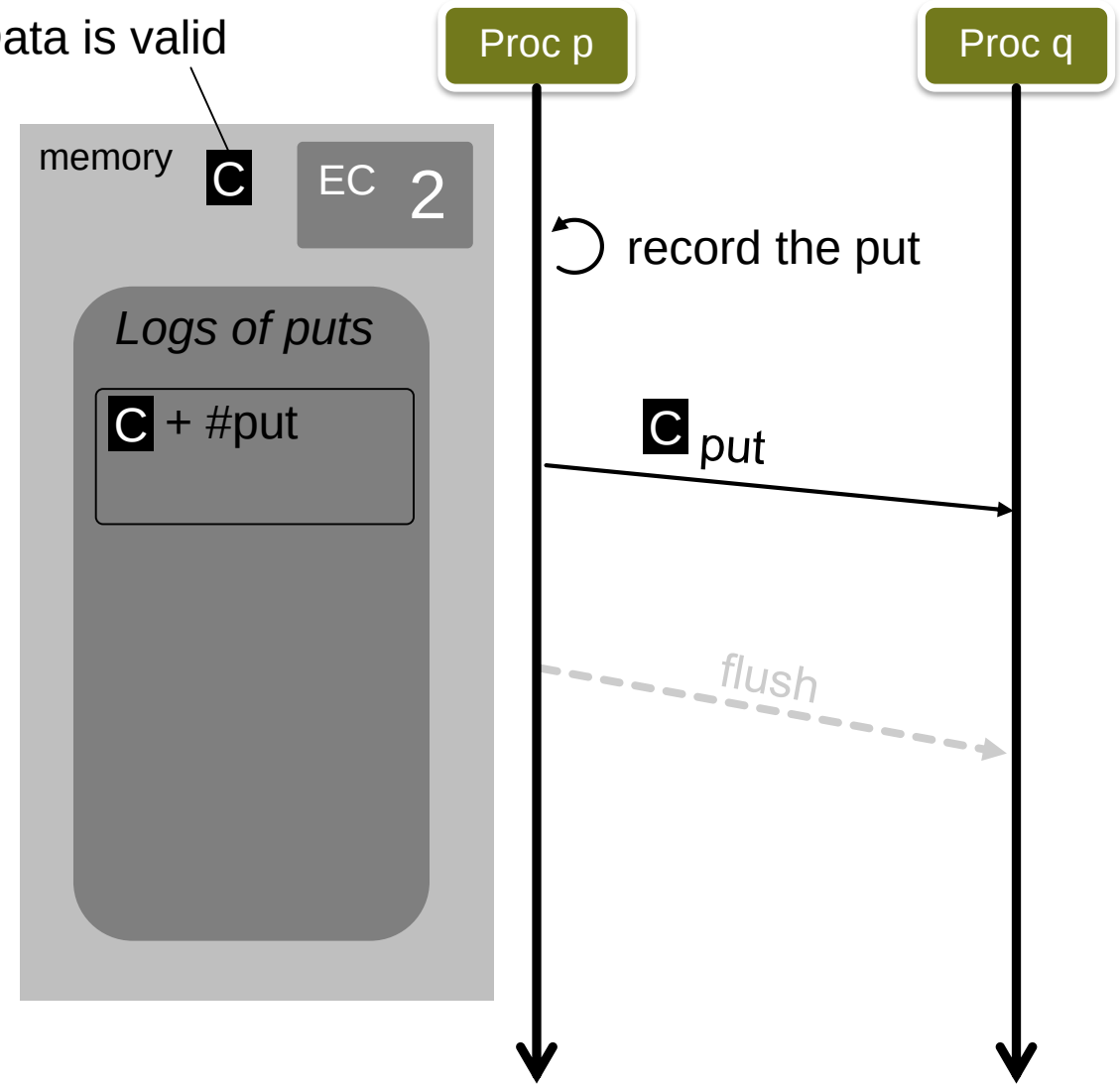

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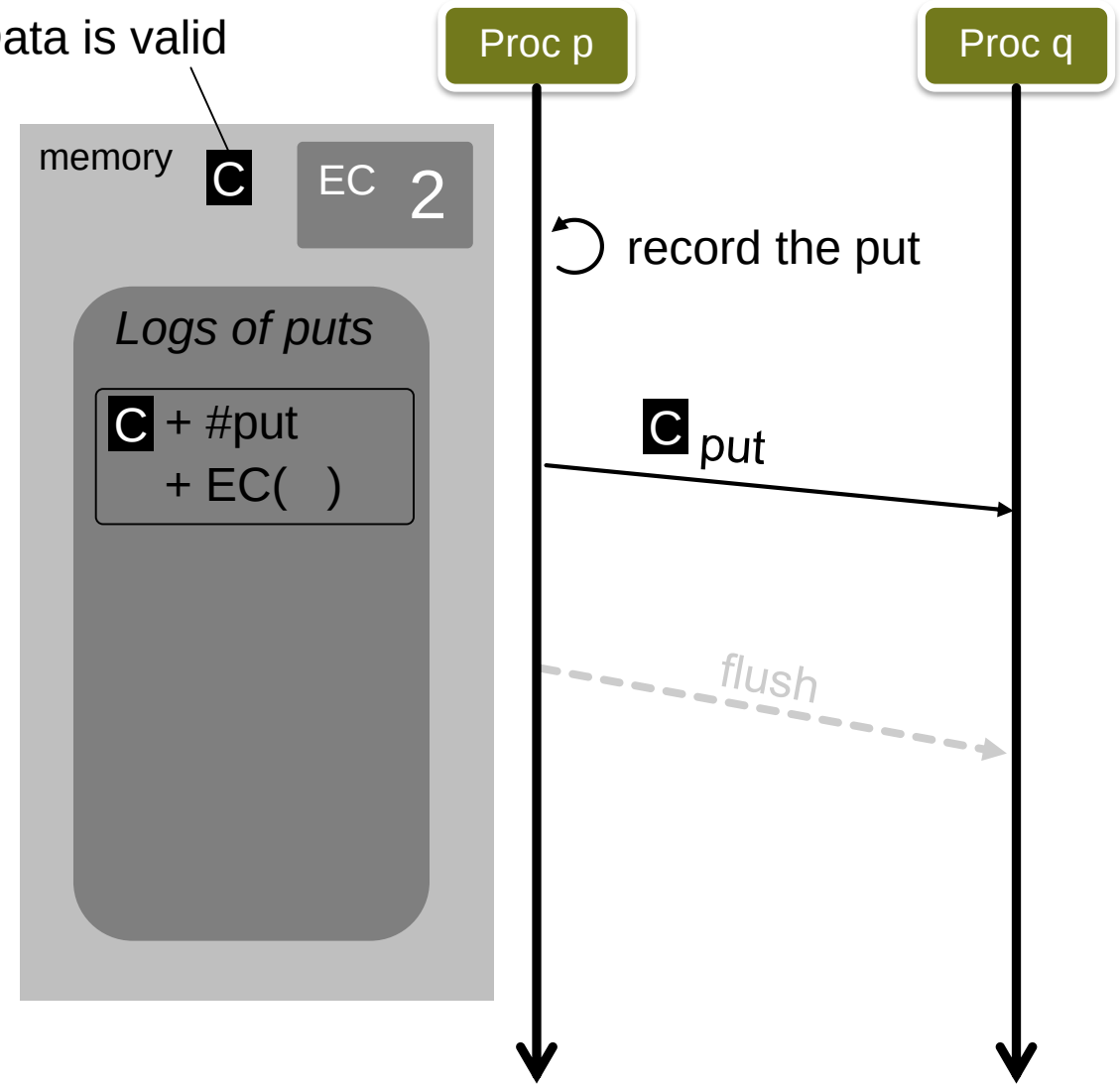

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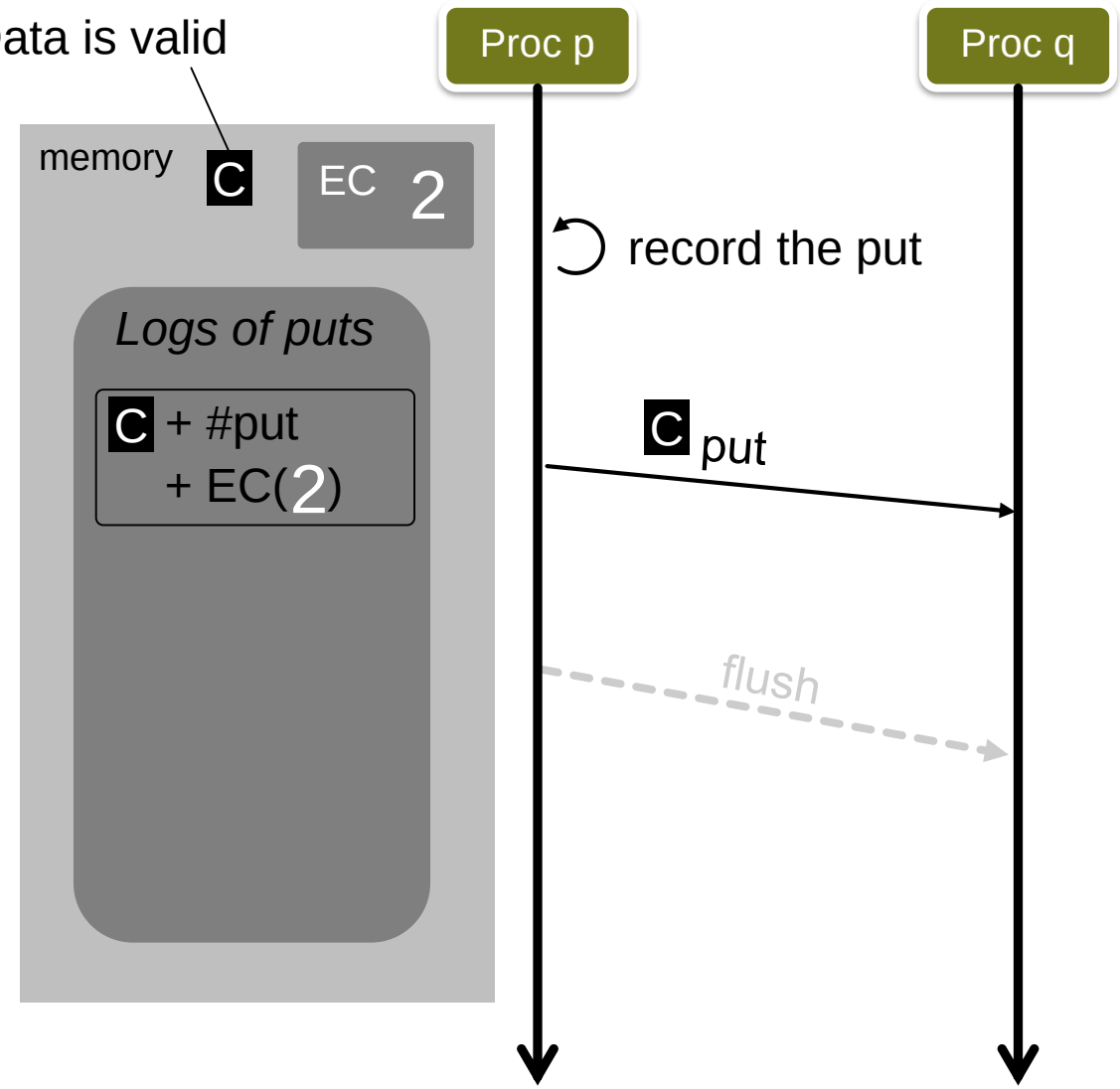

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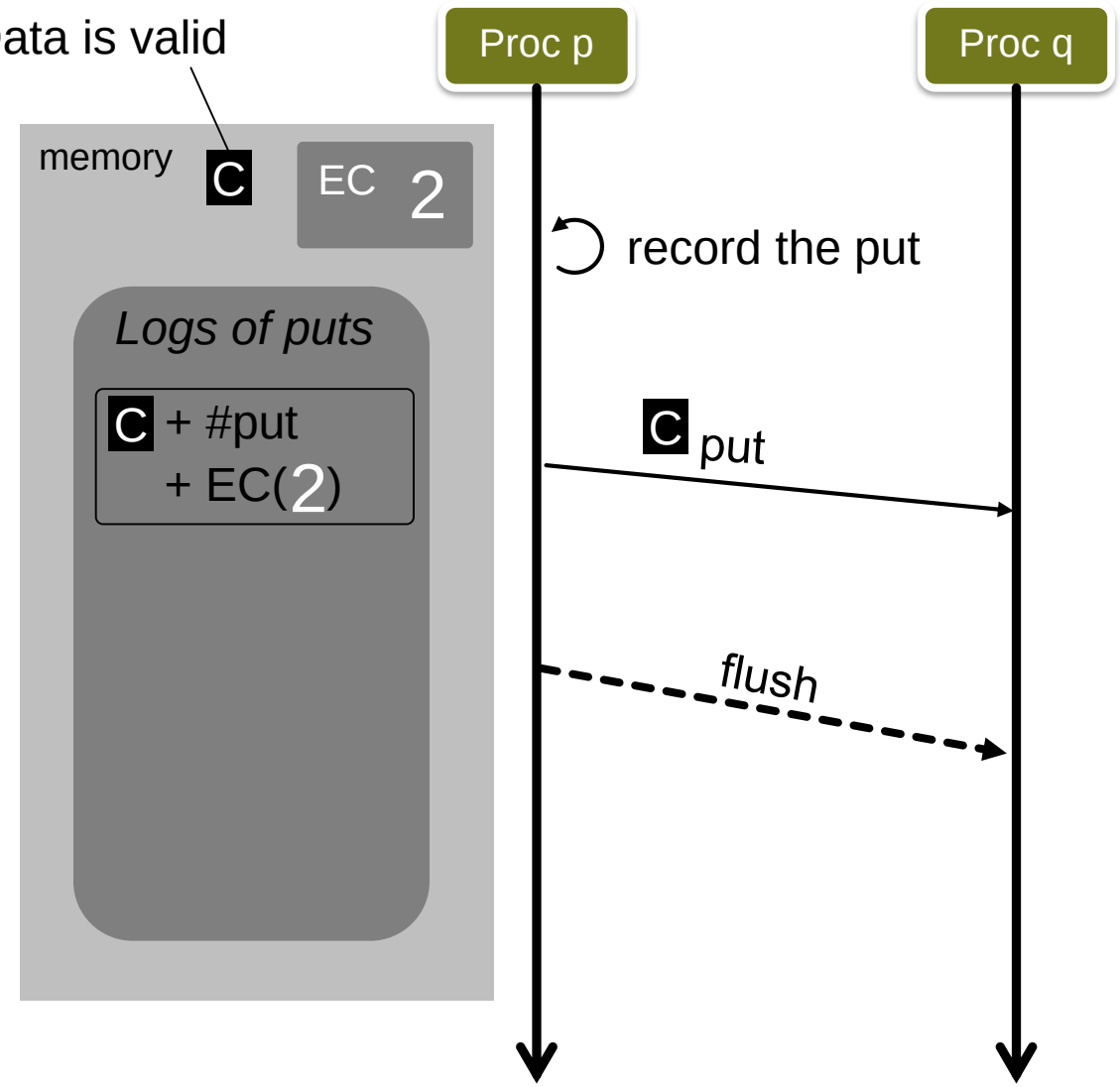

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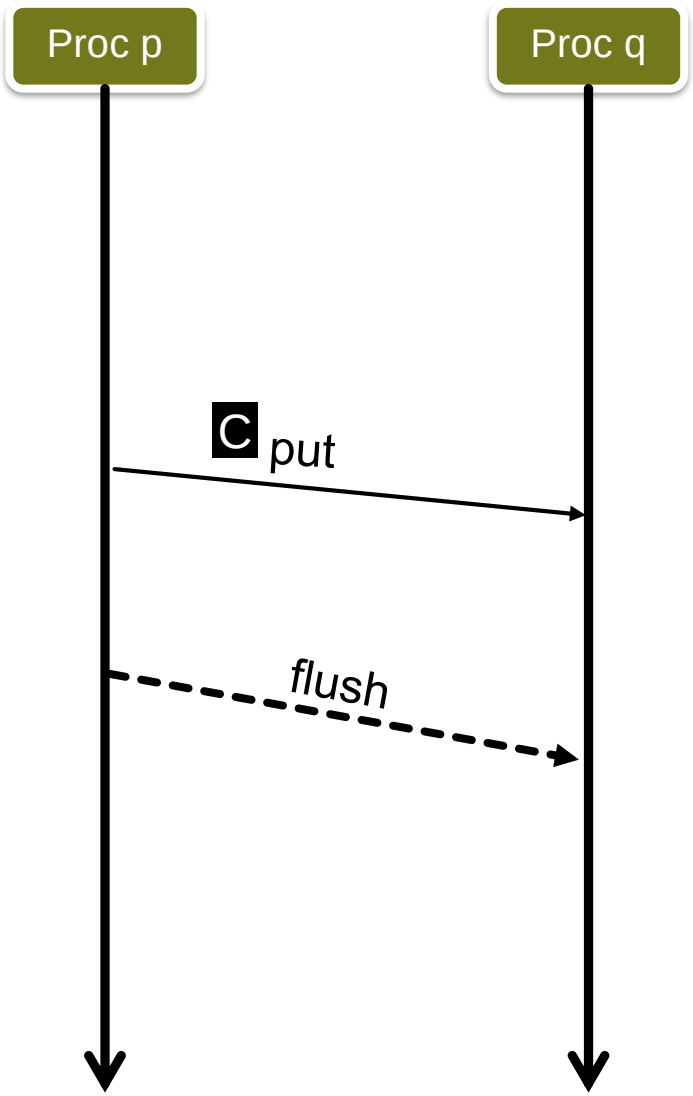
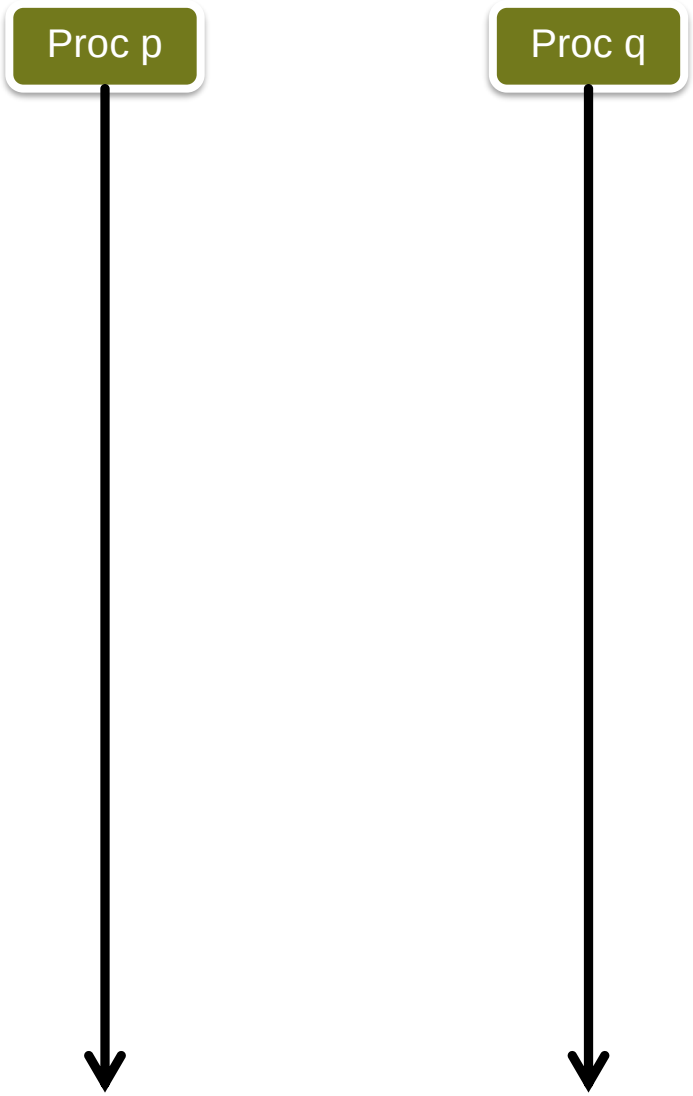
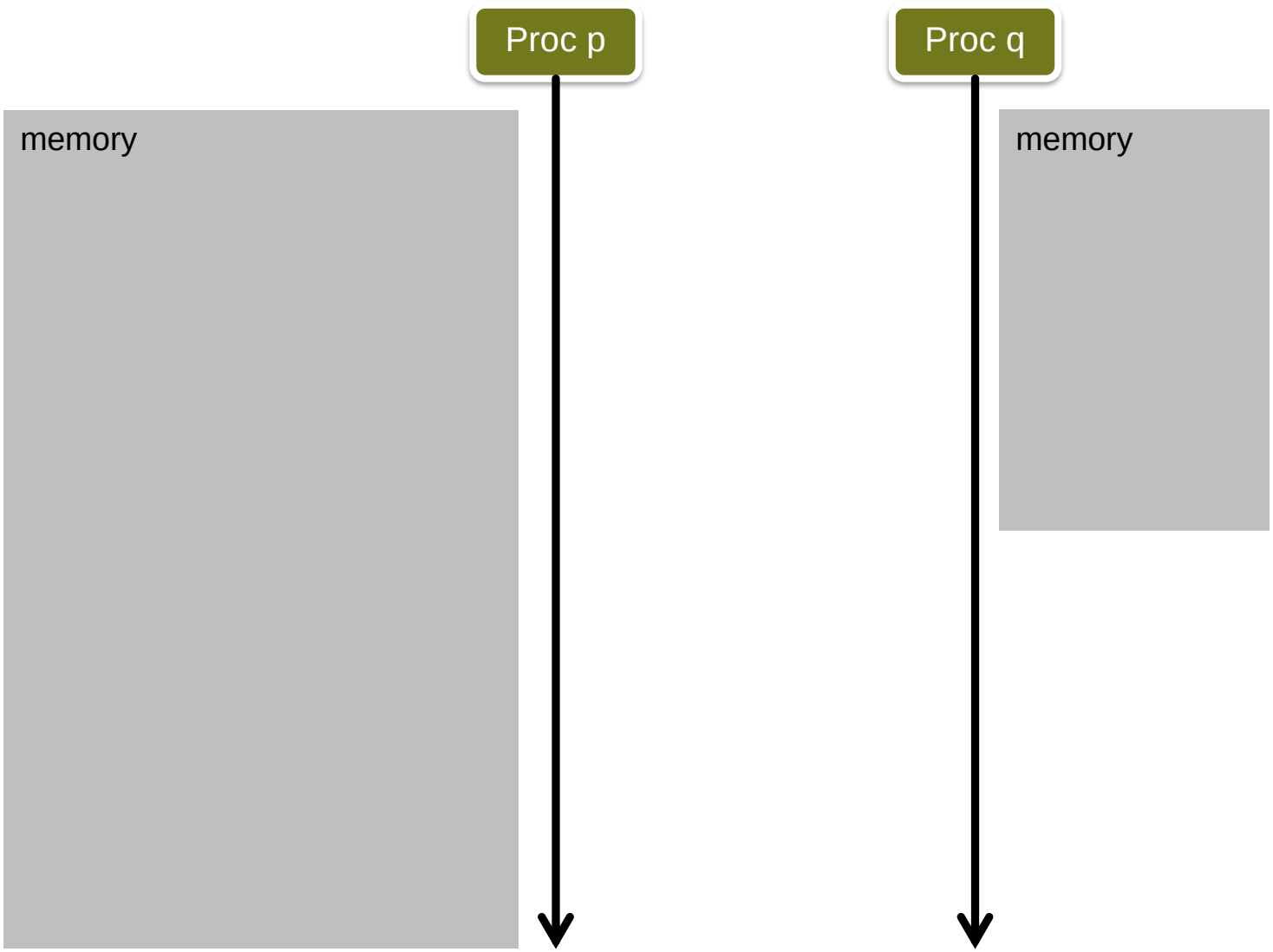


RMA: CHECKPOINTING



RMA: CHECKPOINTING



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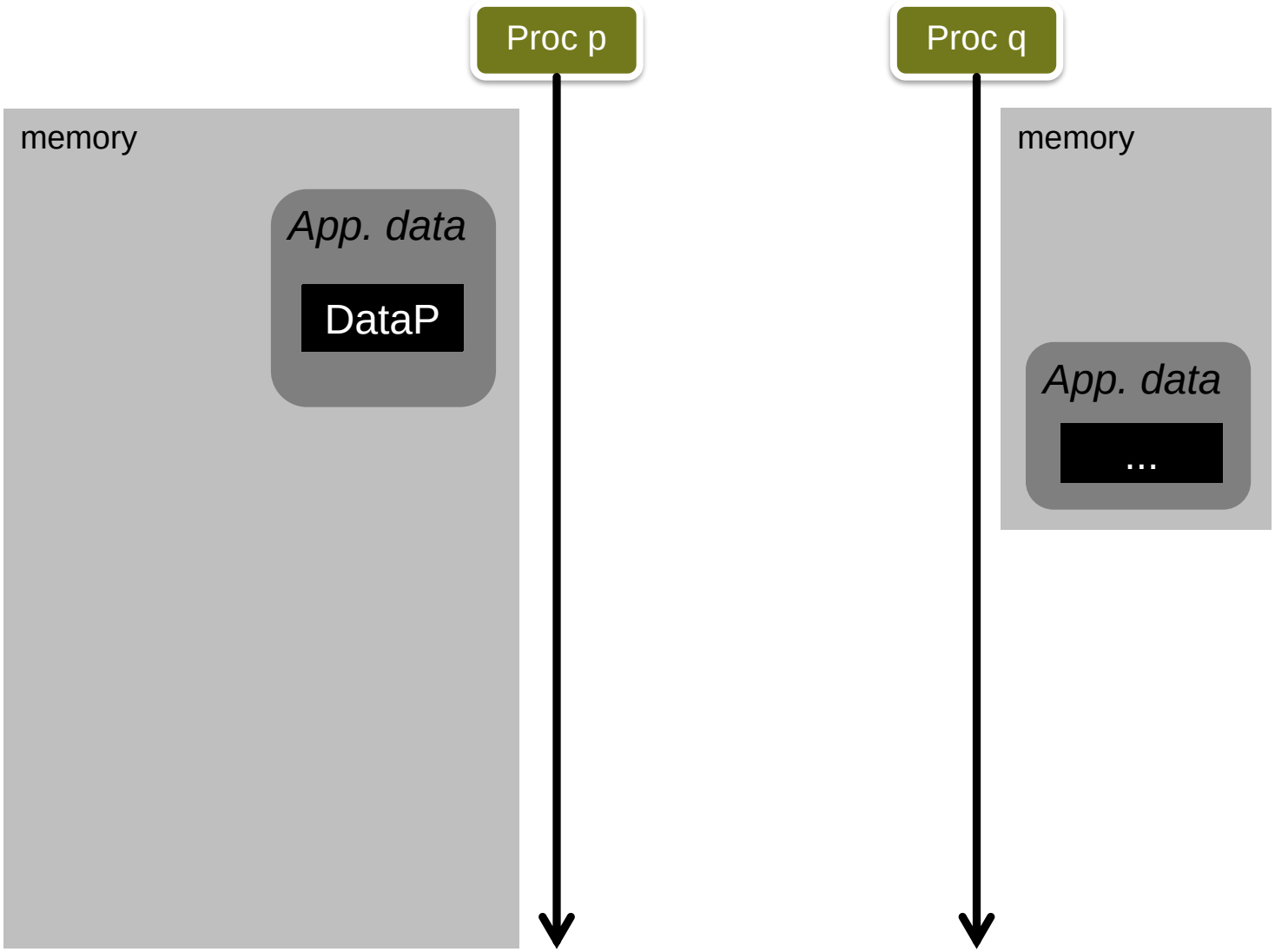

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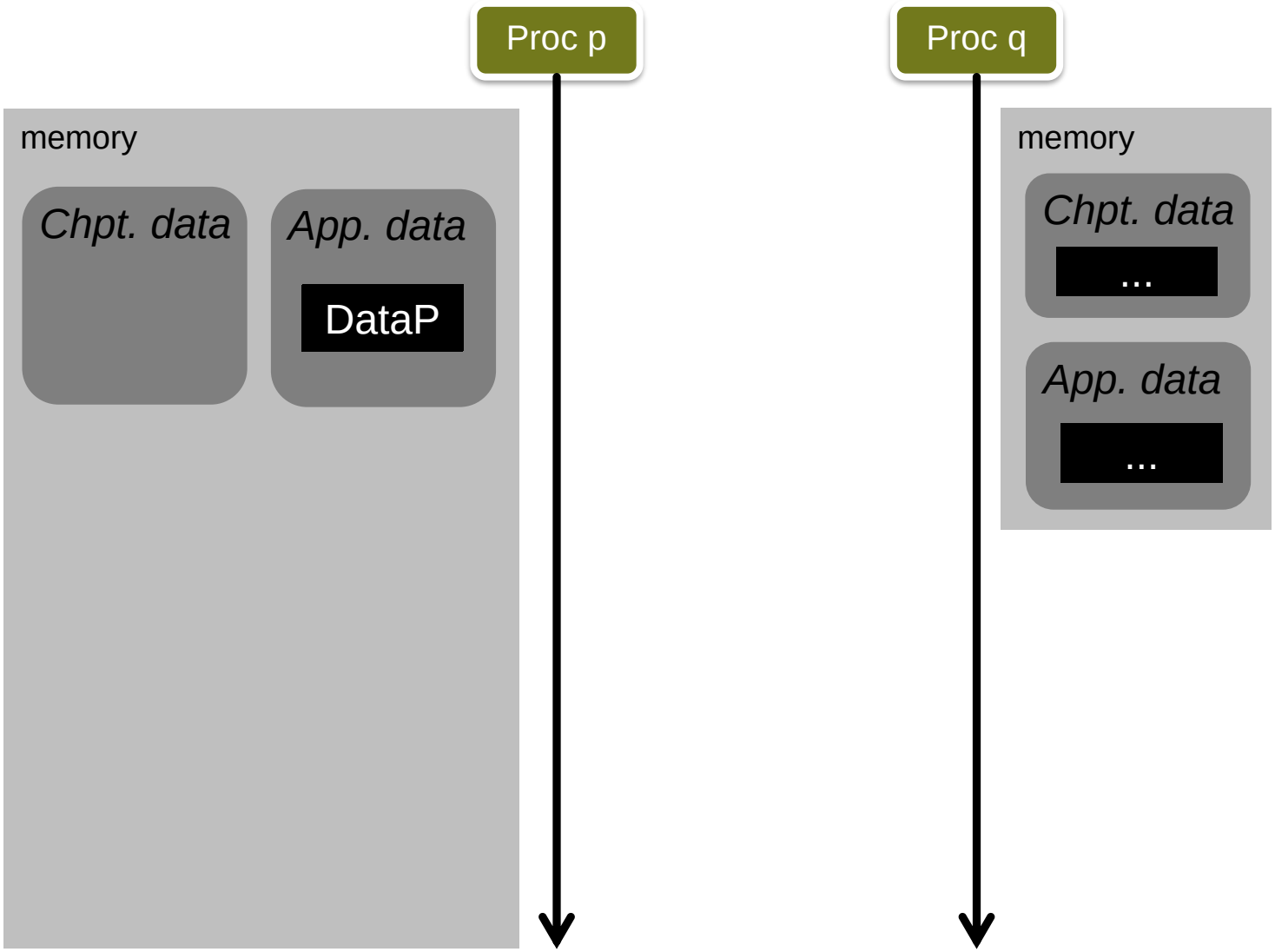

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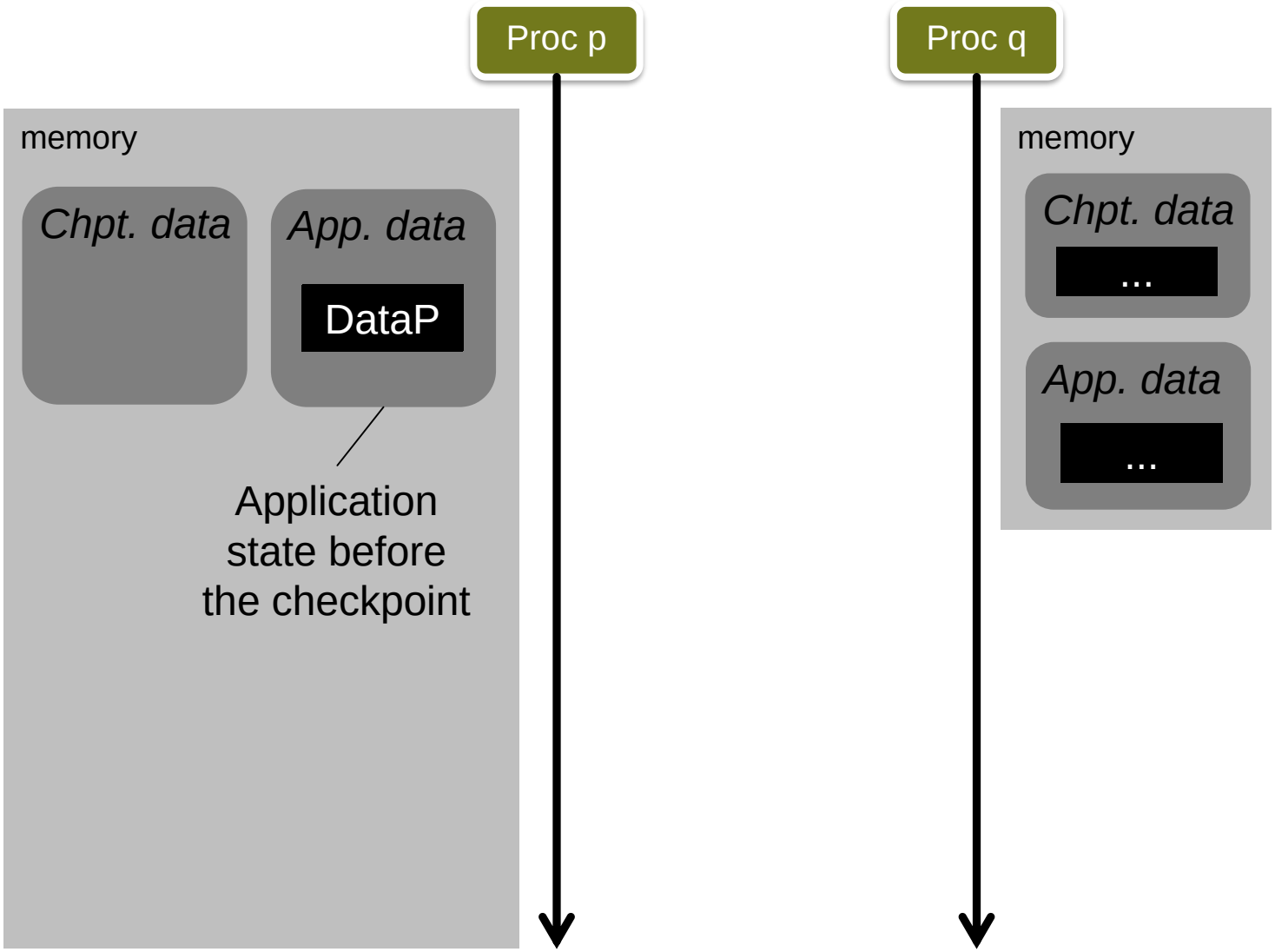

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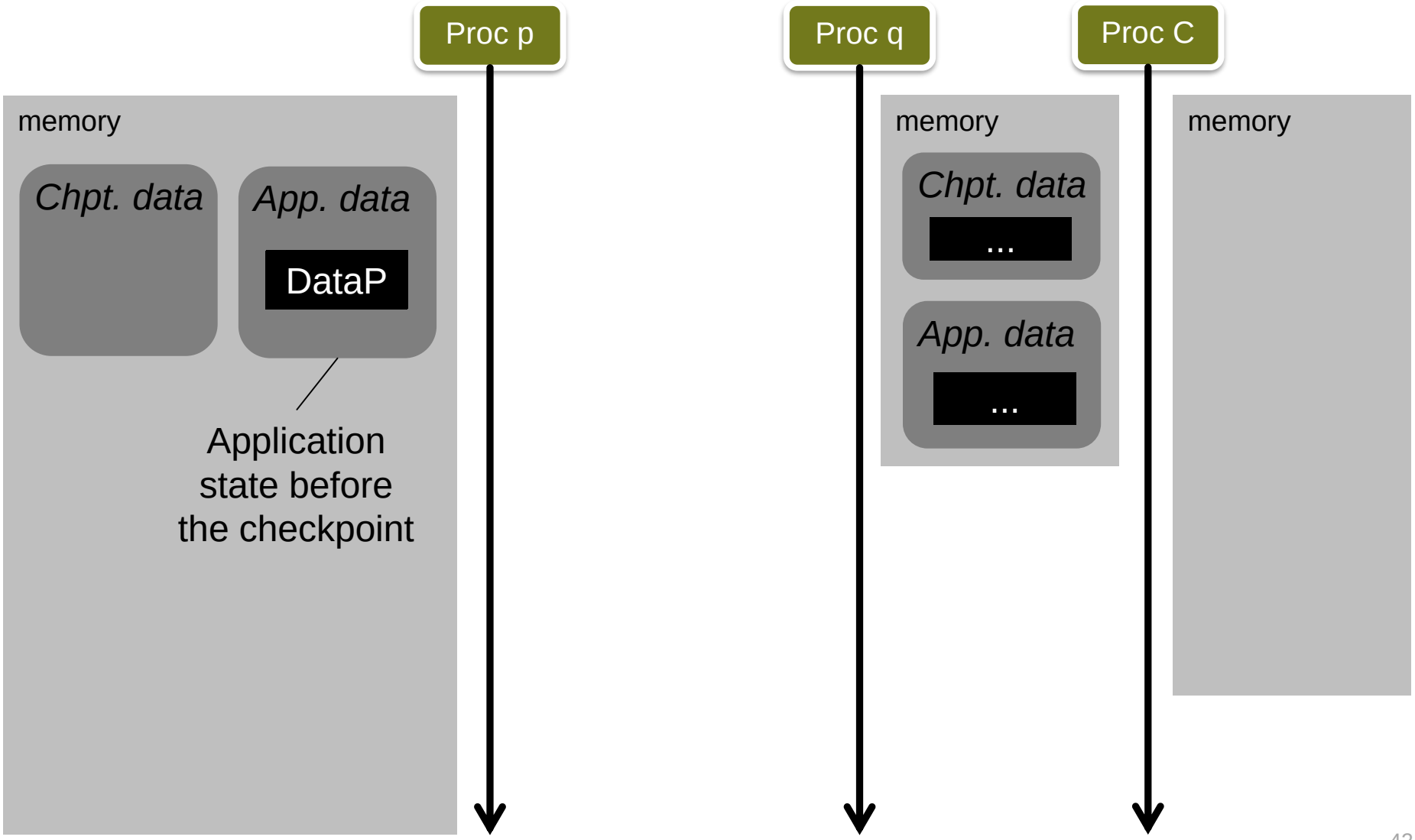

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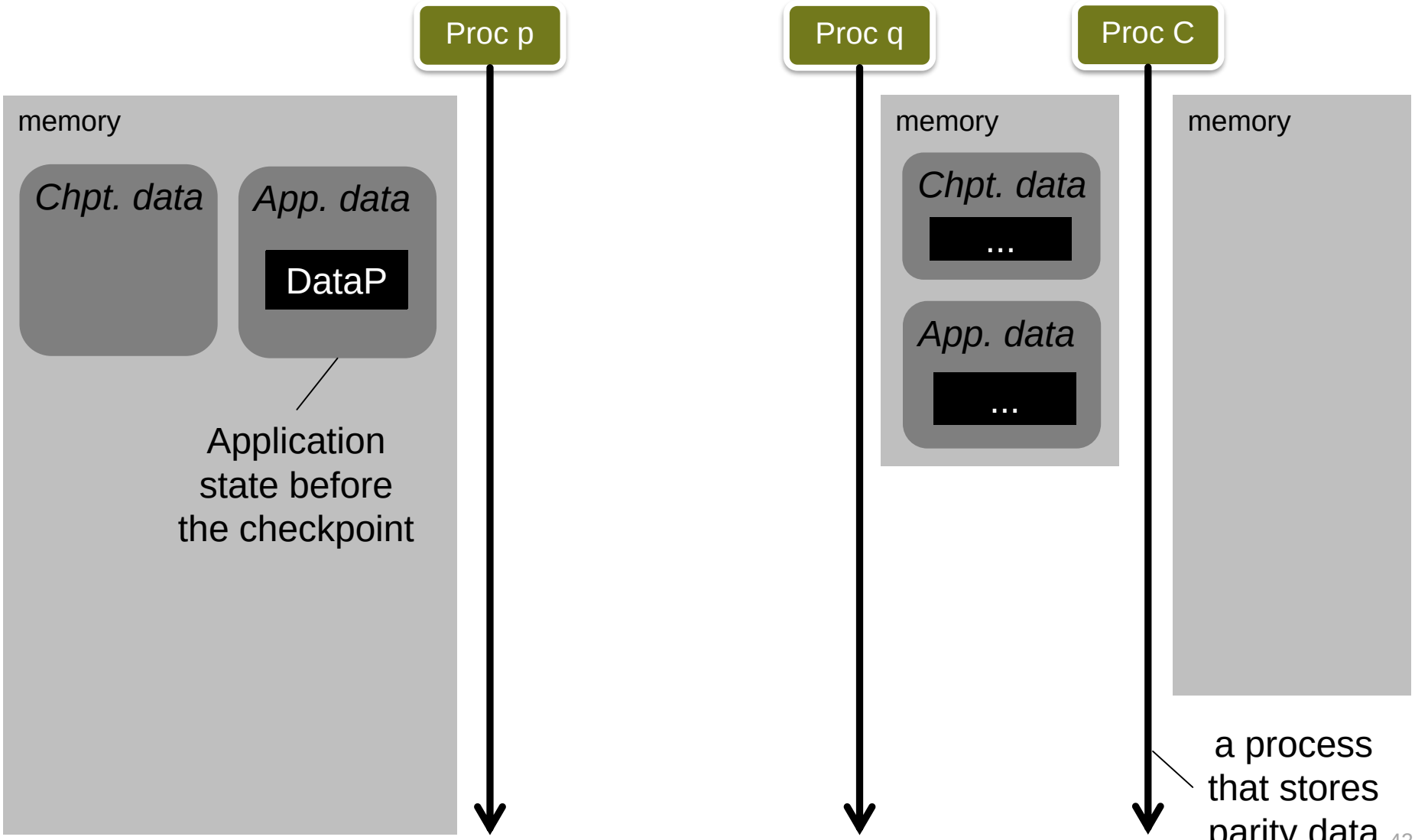

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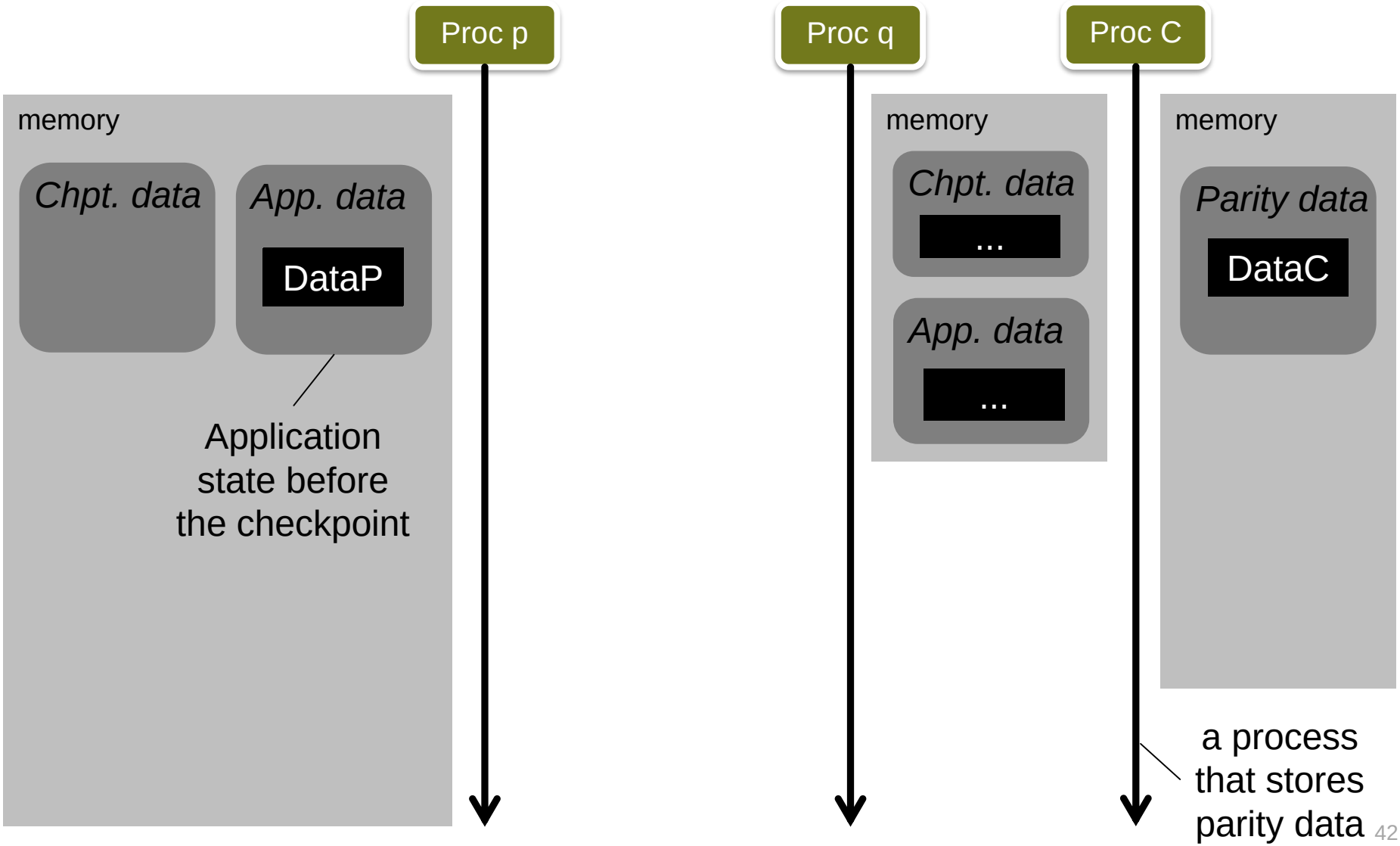

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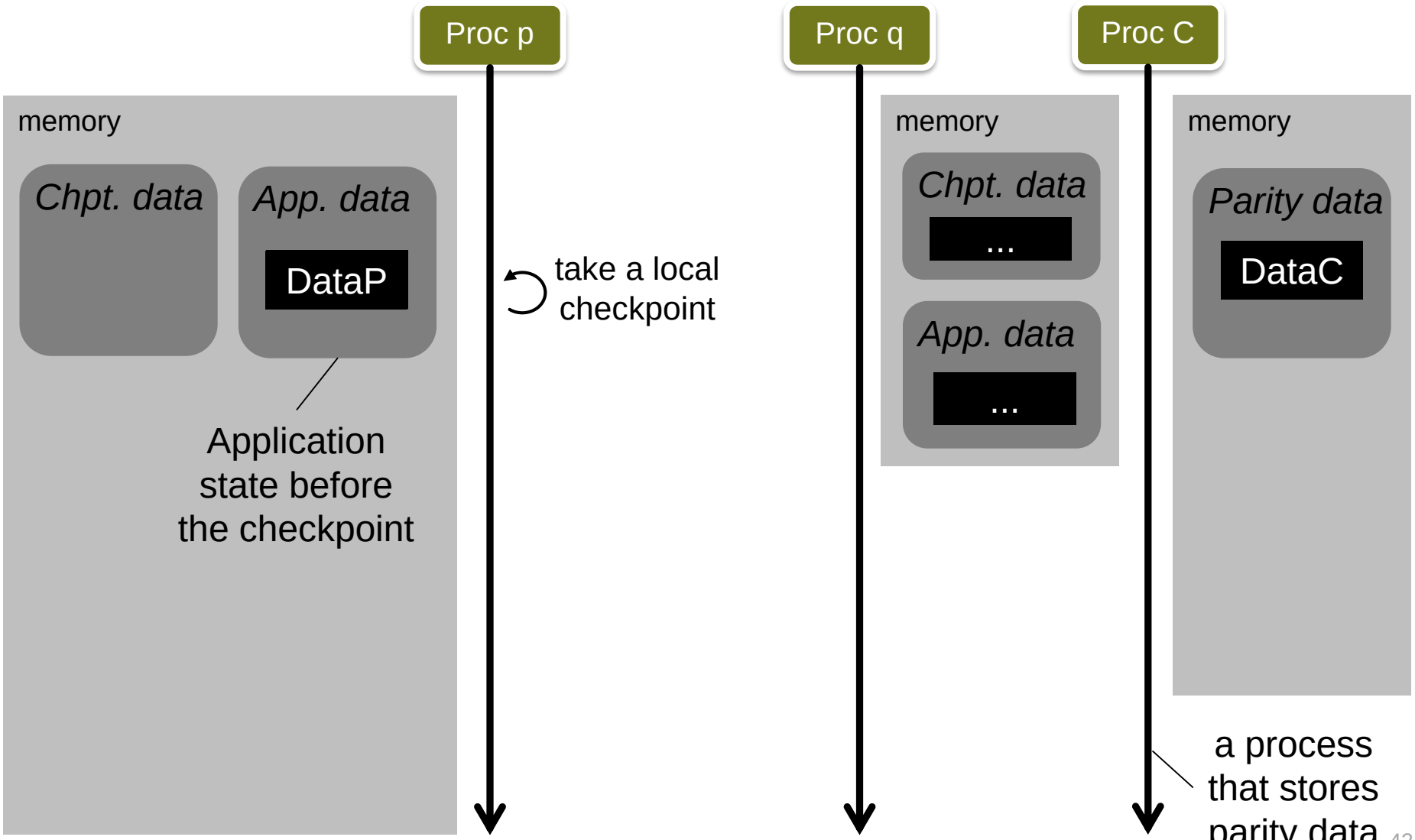

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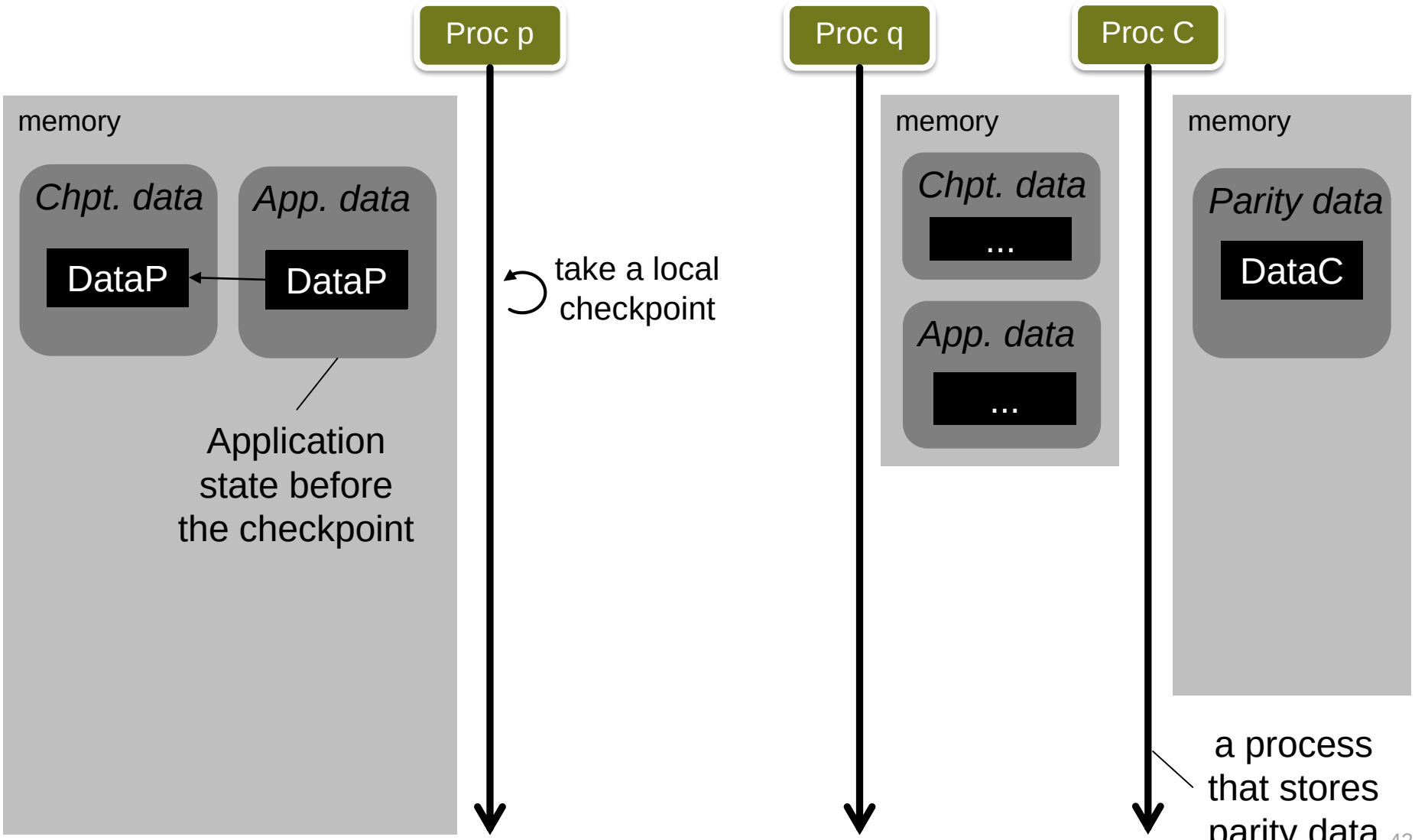

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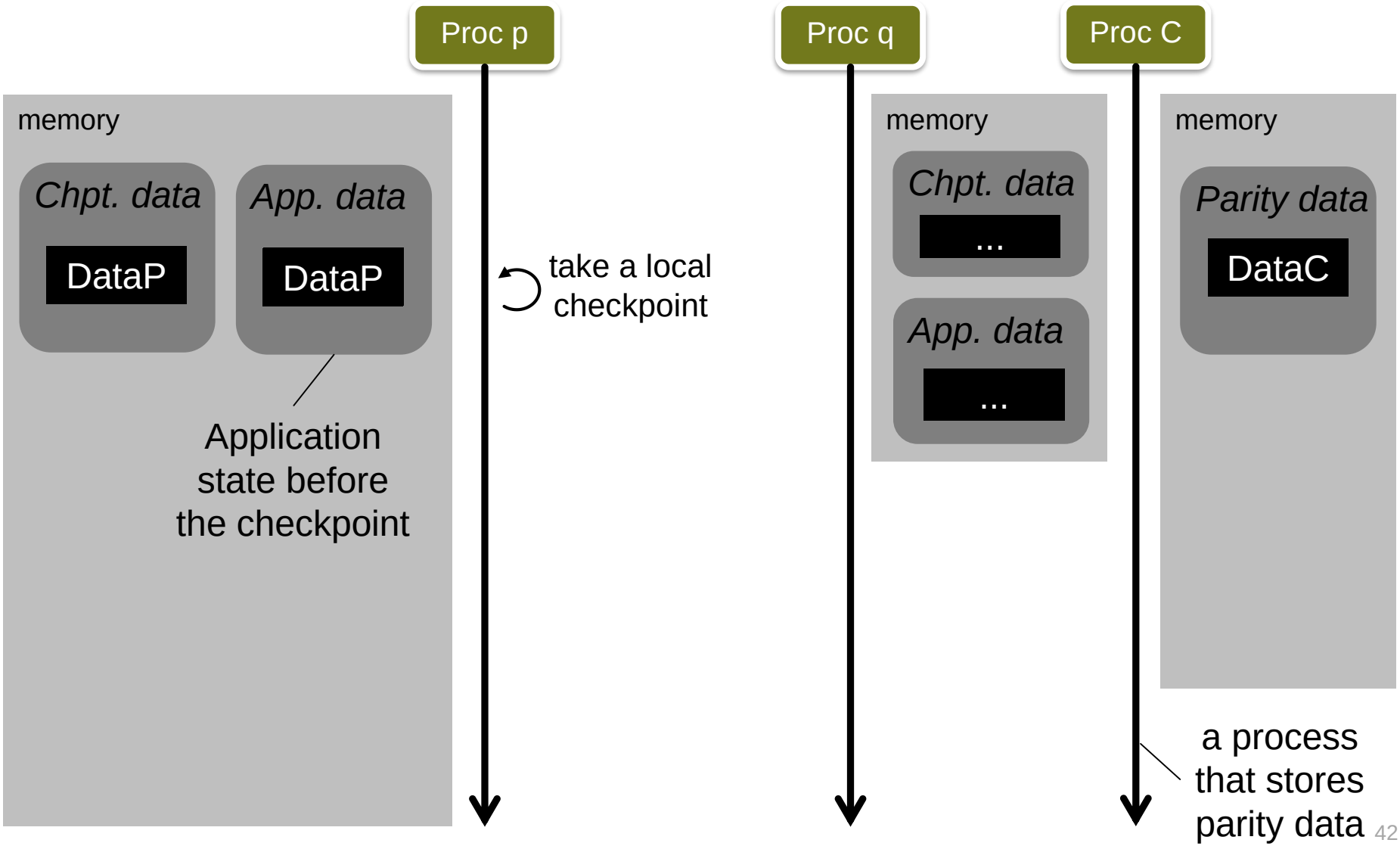

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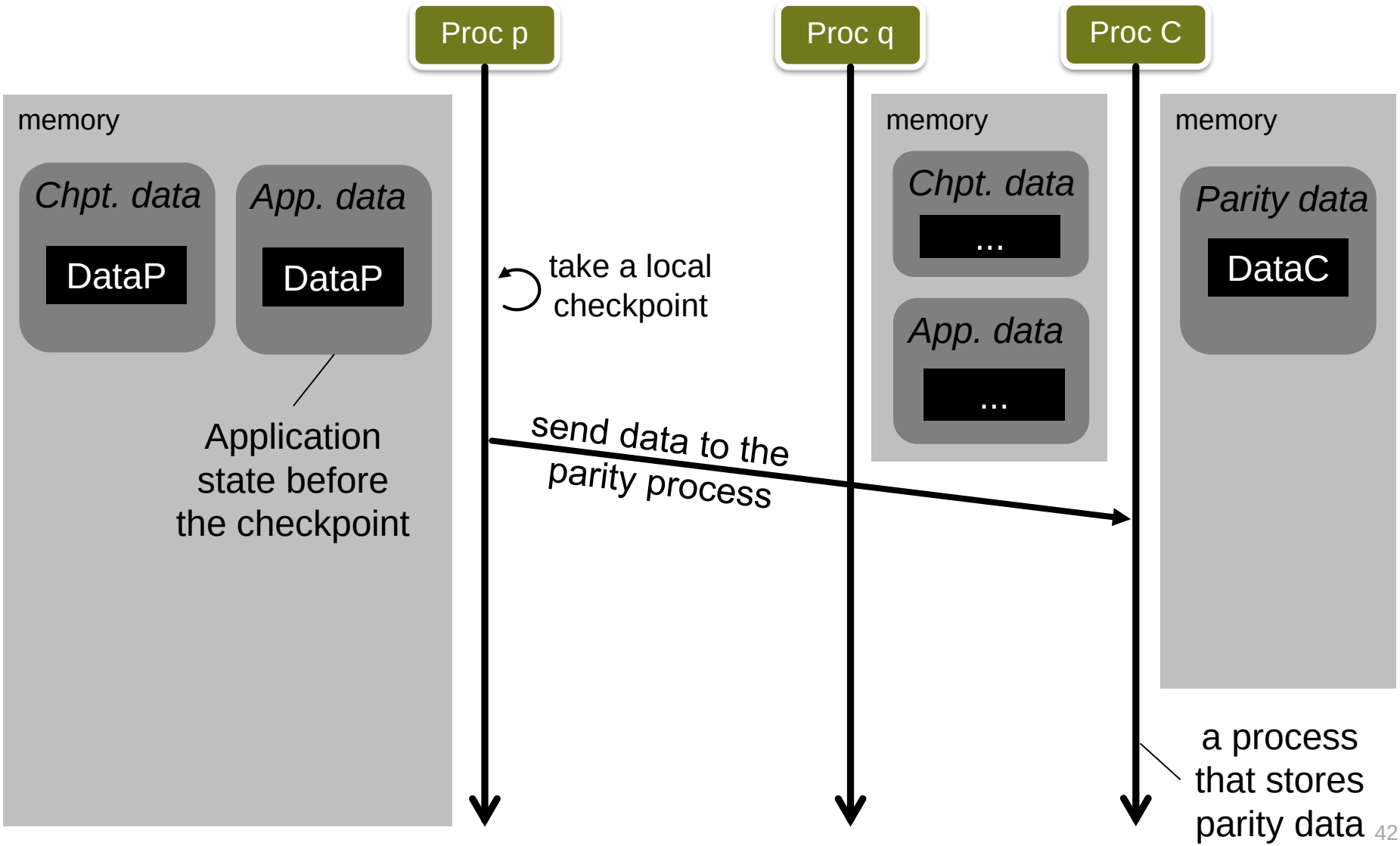

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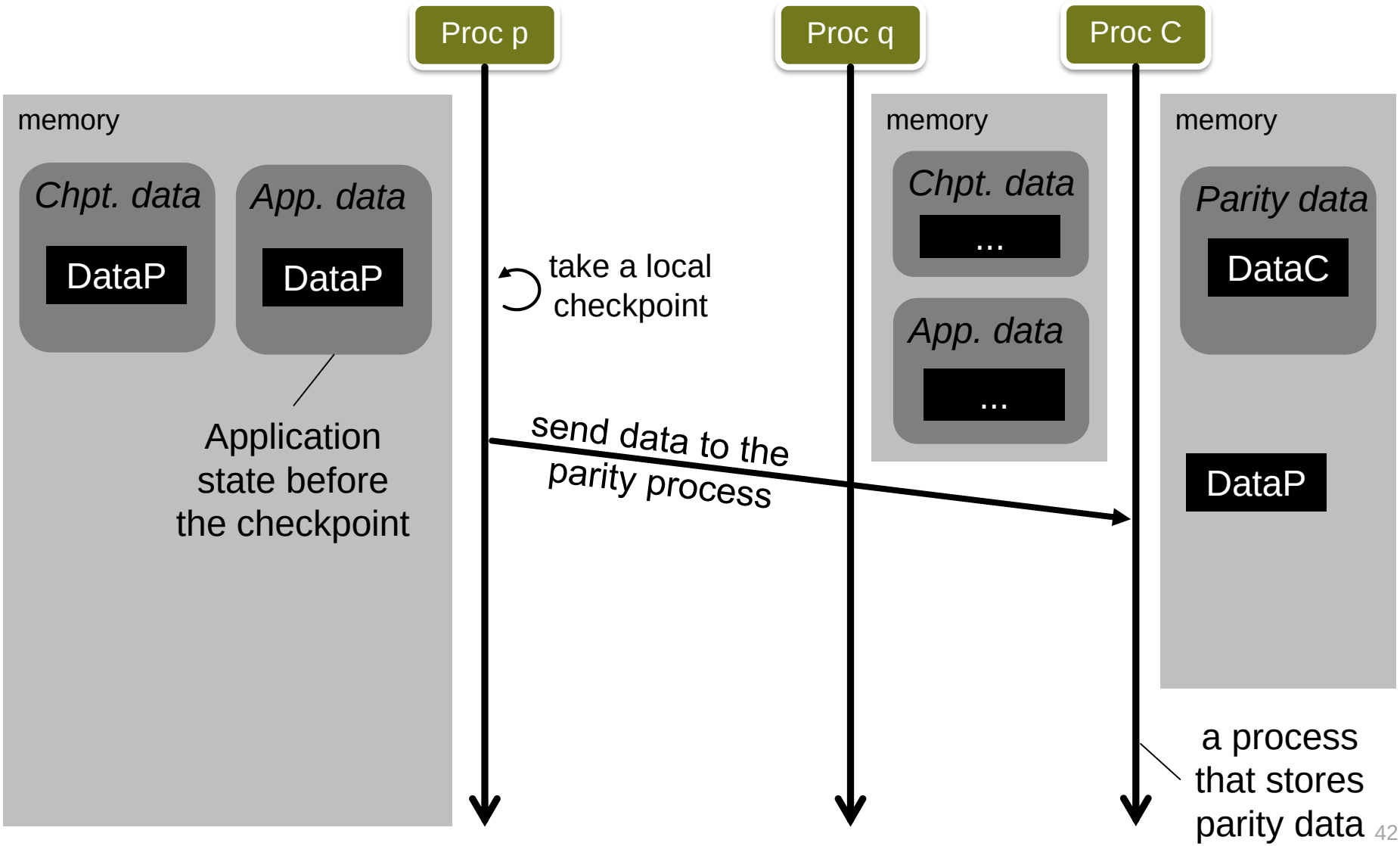

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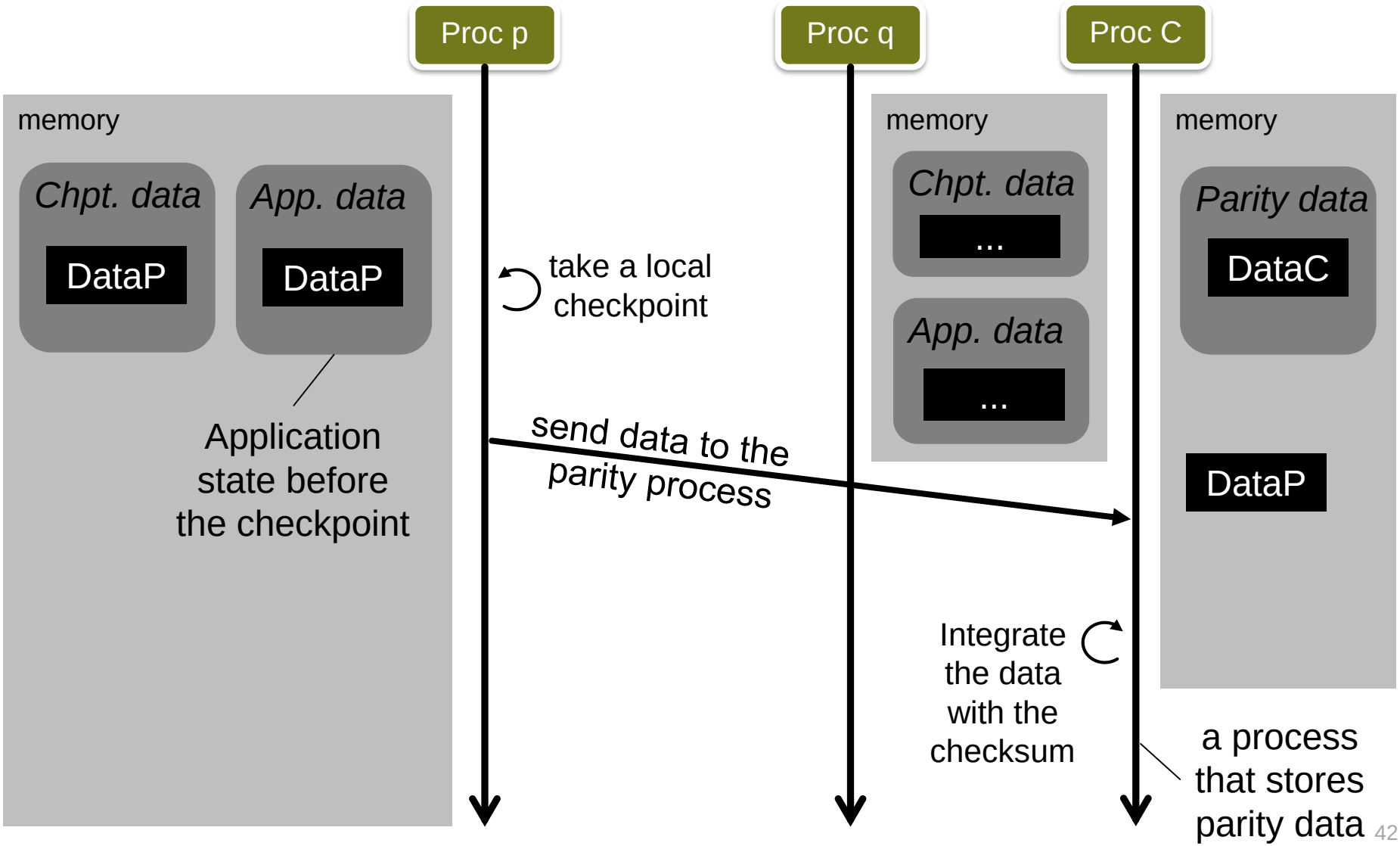

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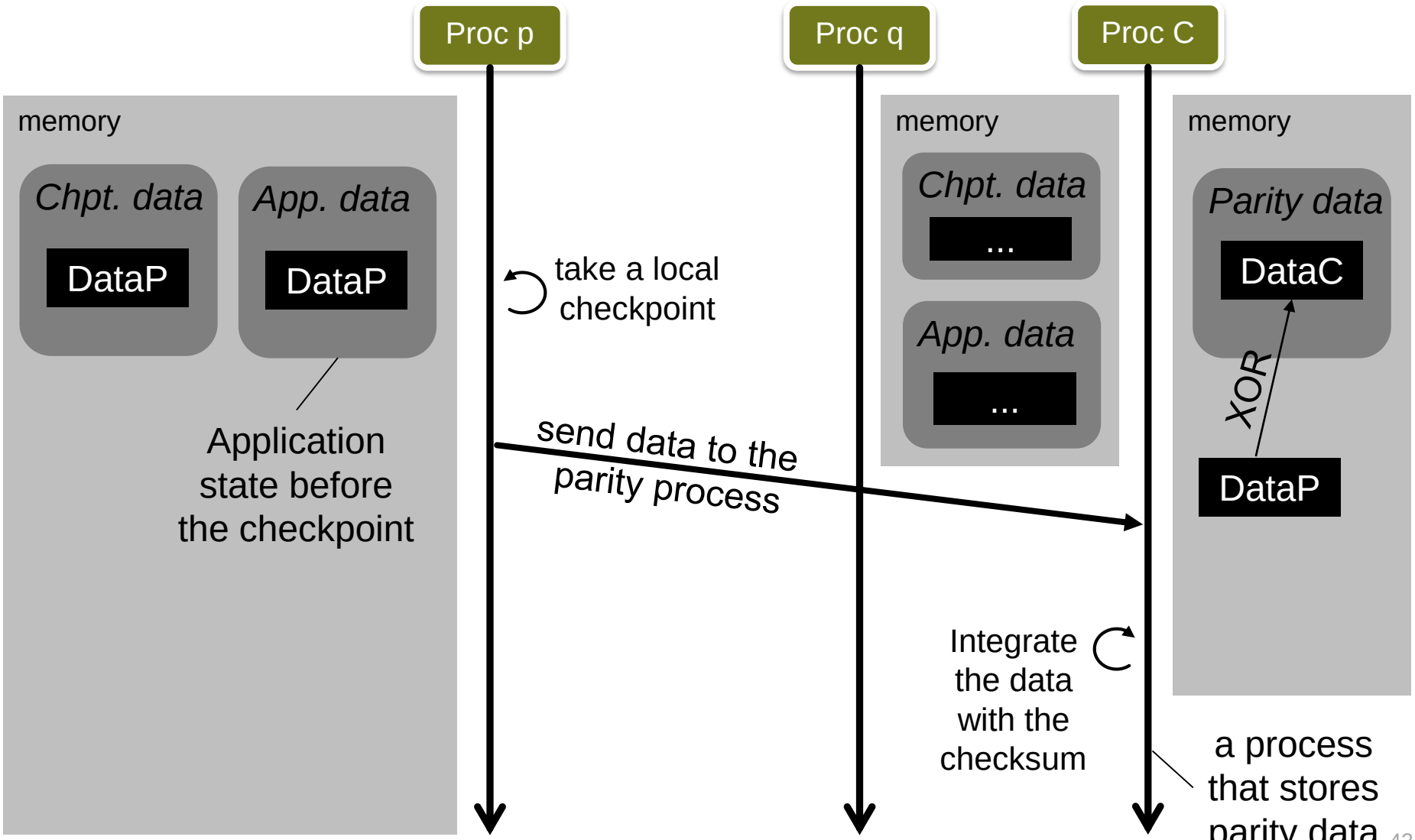

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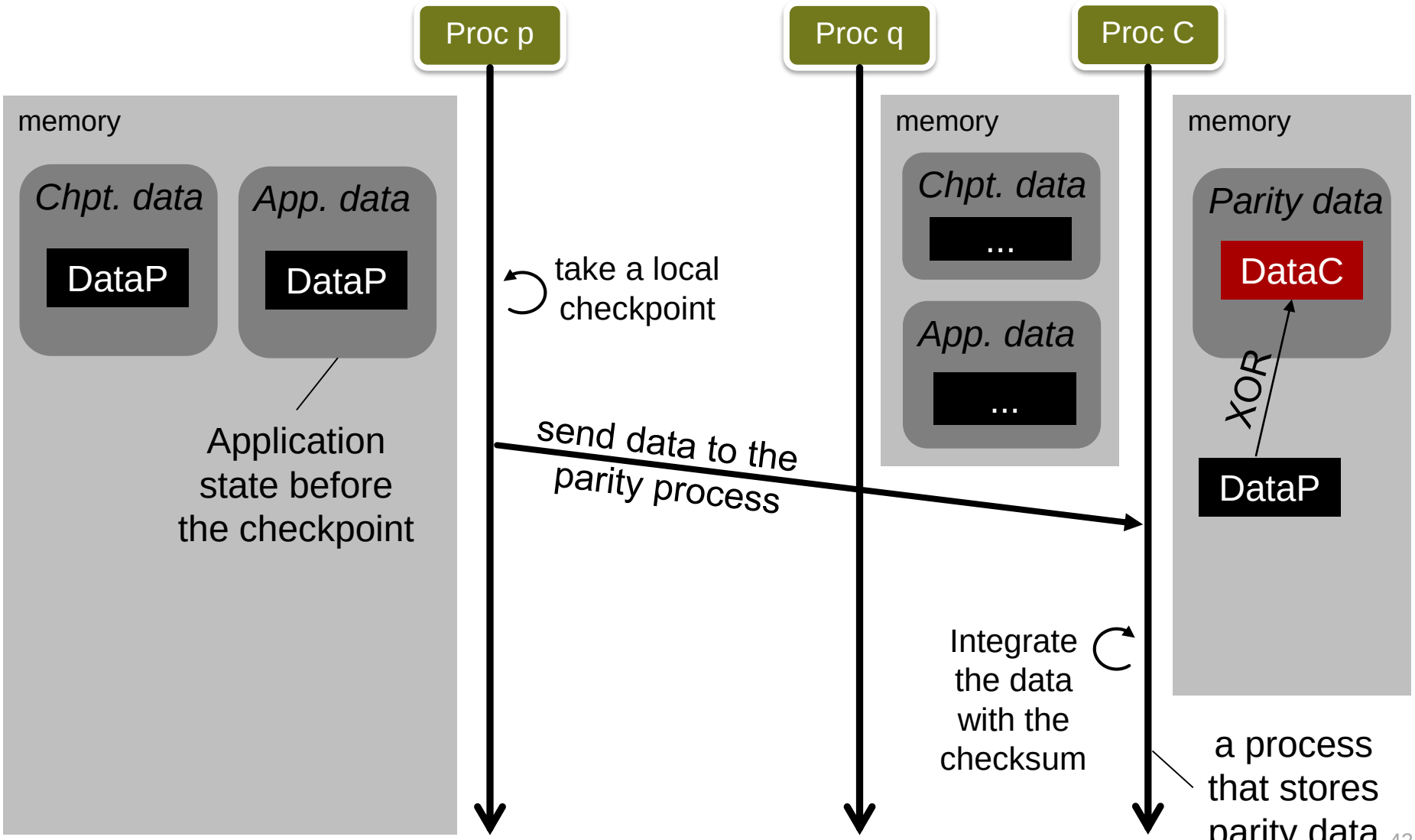

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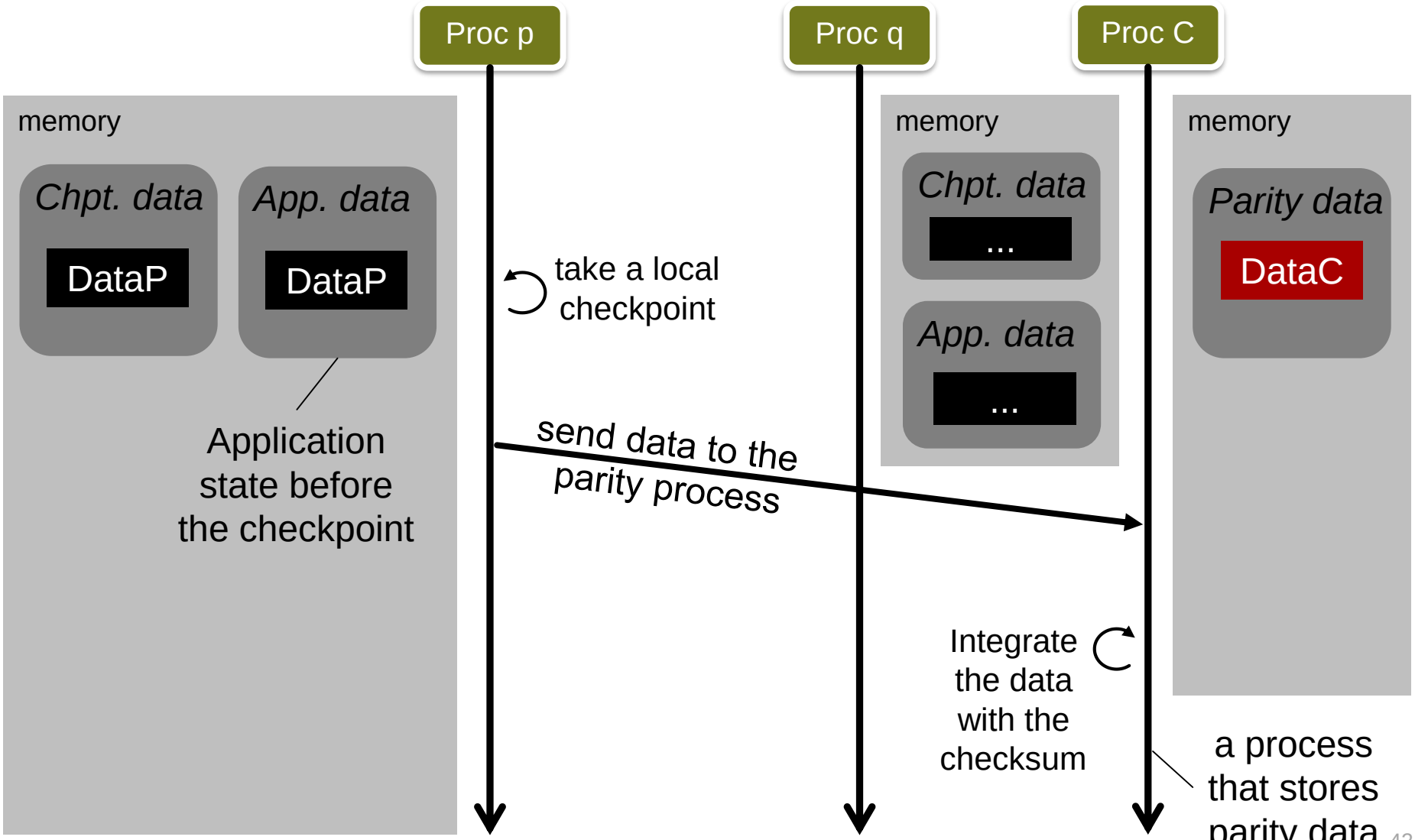

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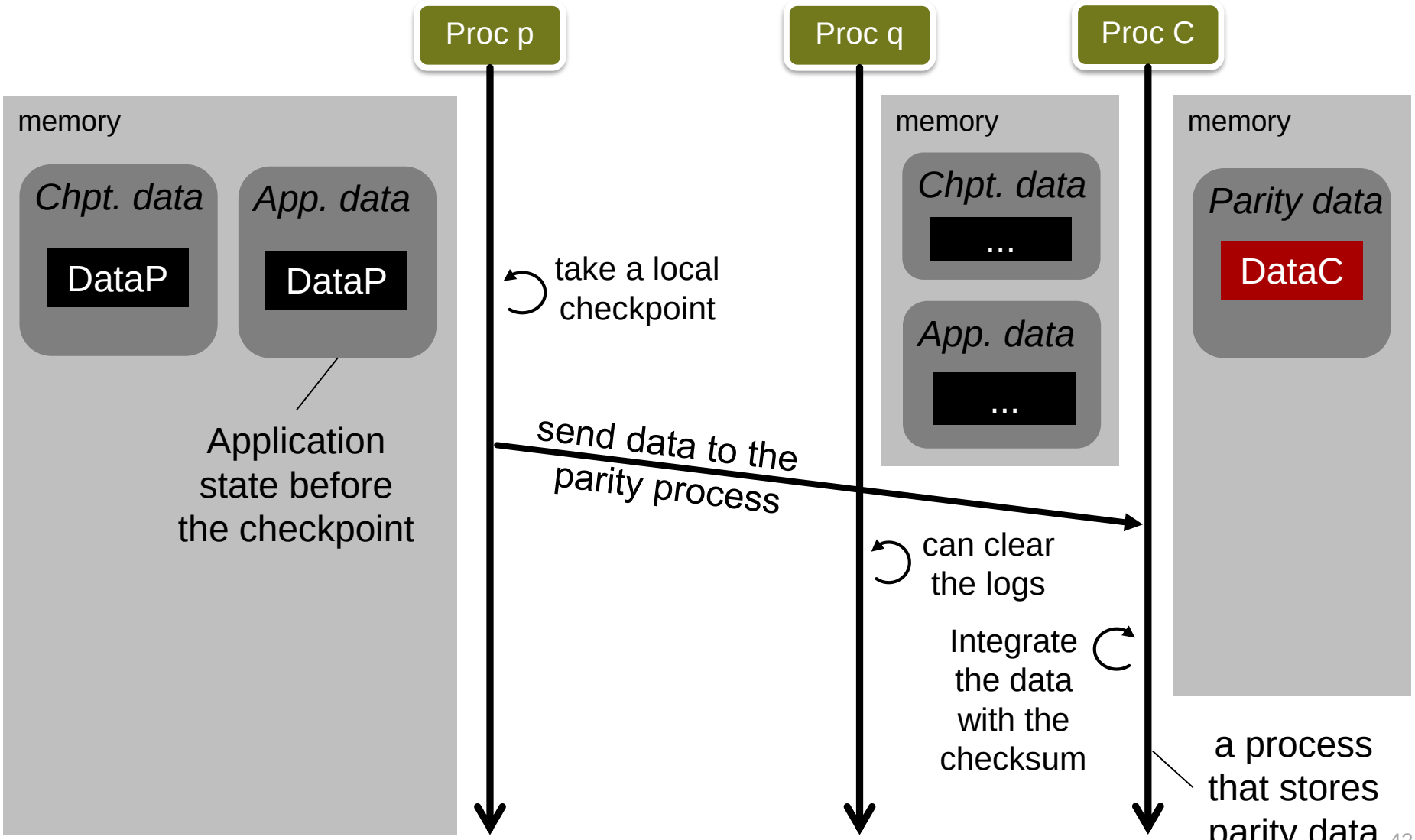
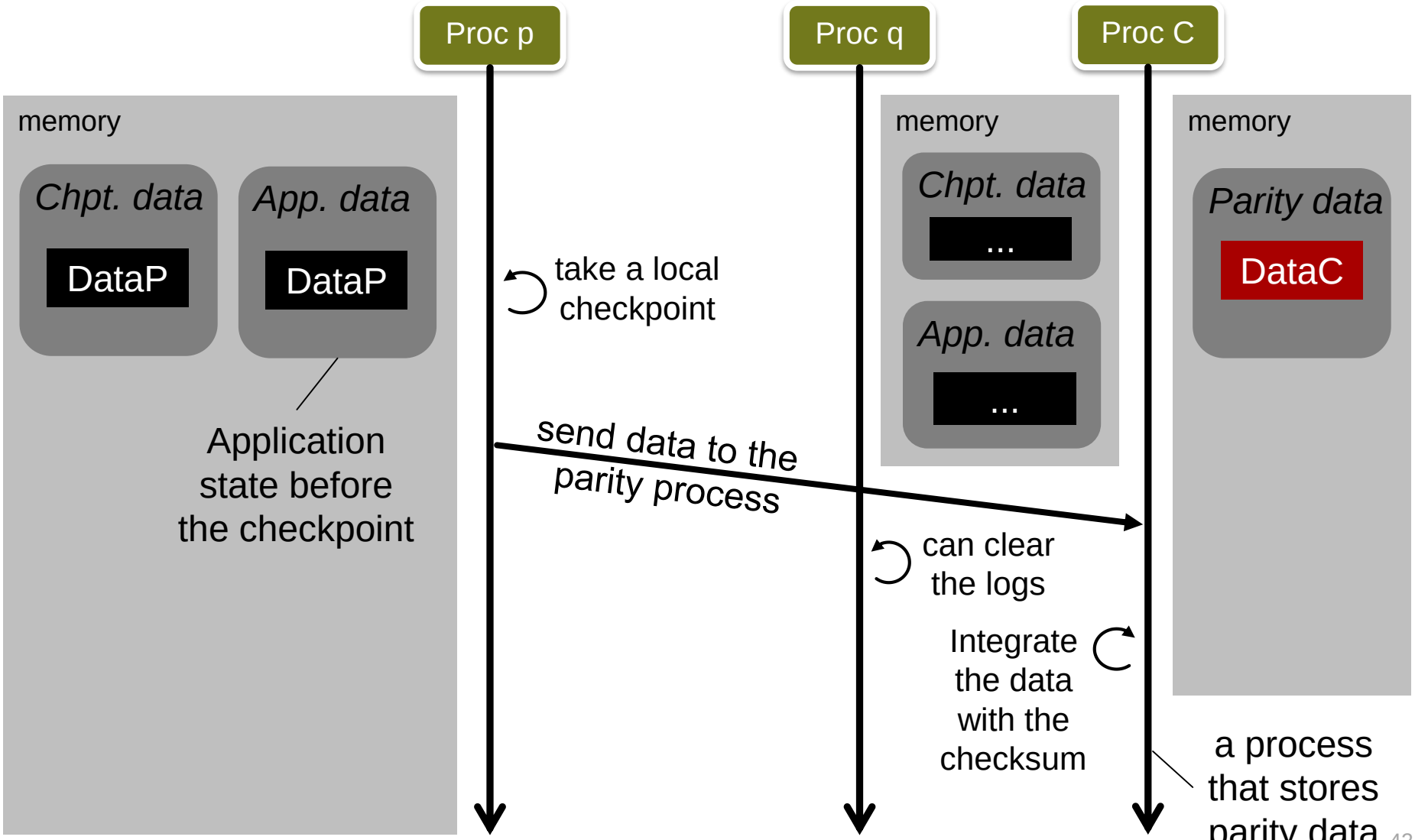


RMA: CHECKPOINTING

The Epoch Condition



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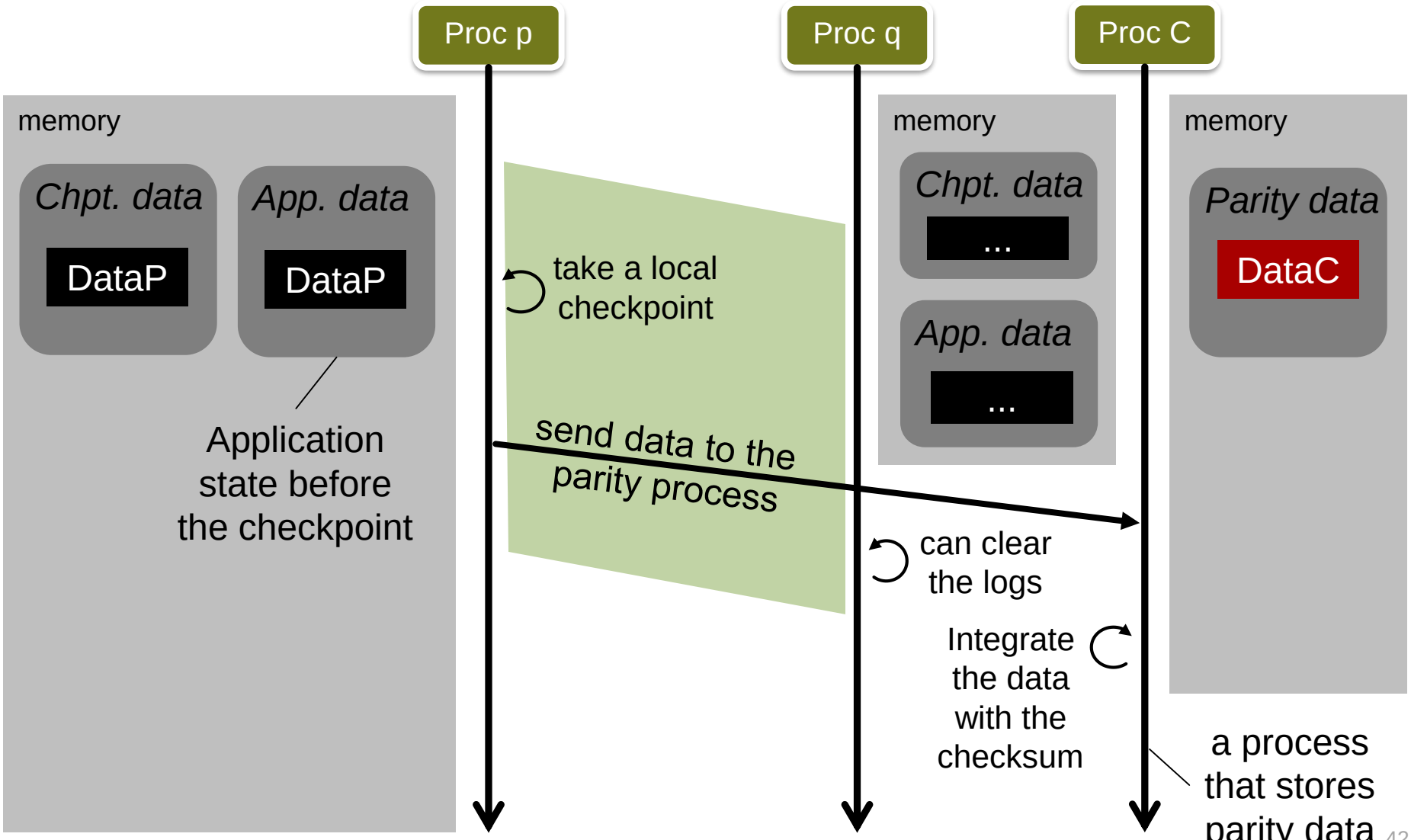

RMA: CHECKPOINTING

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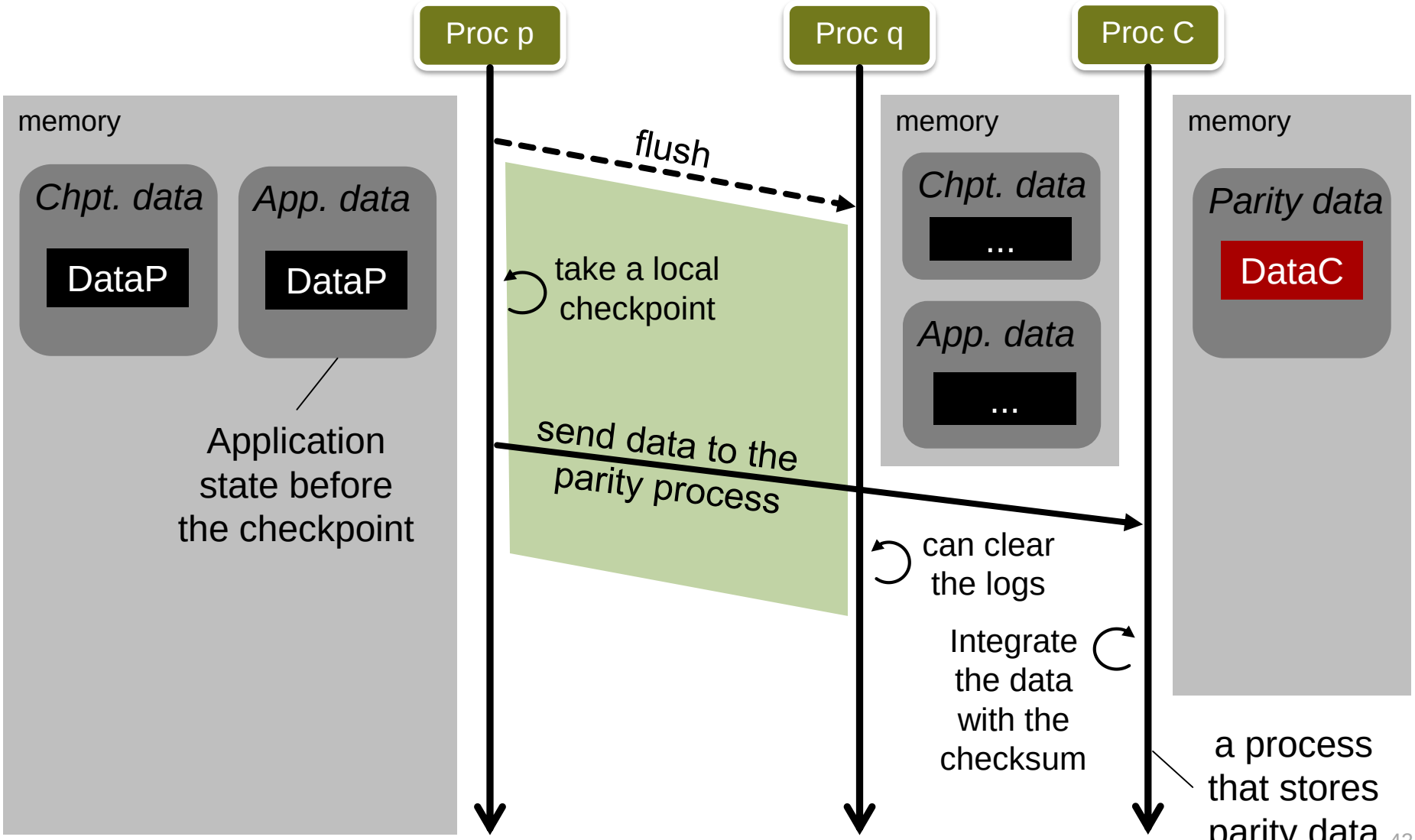

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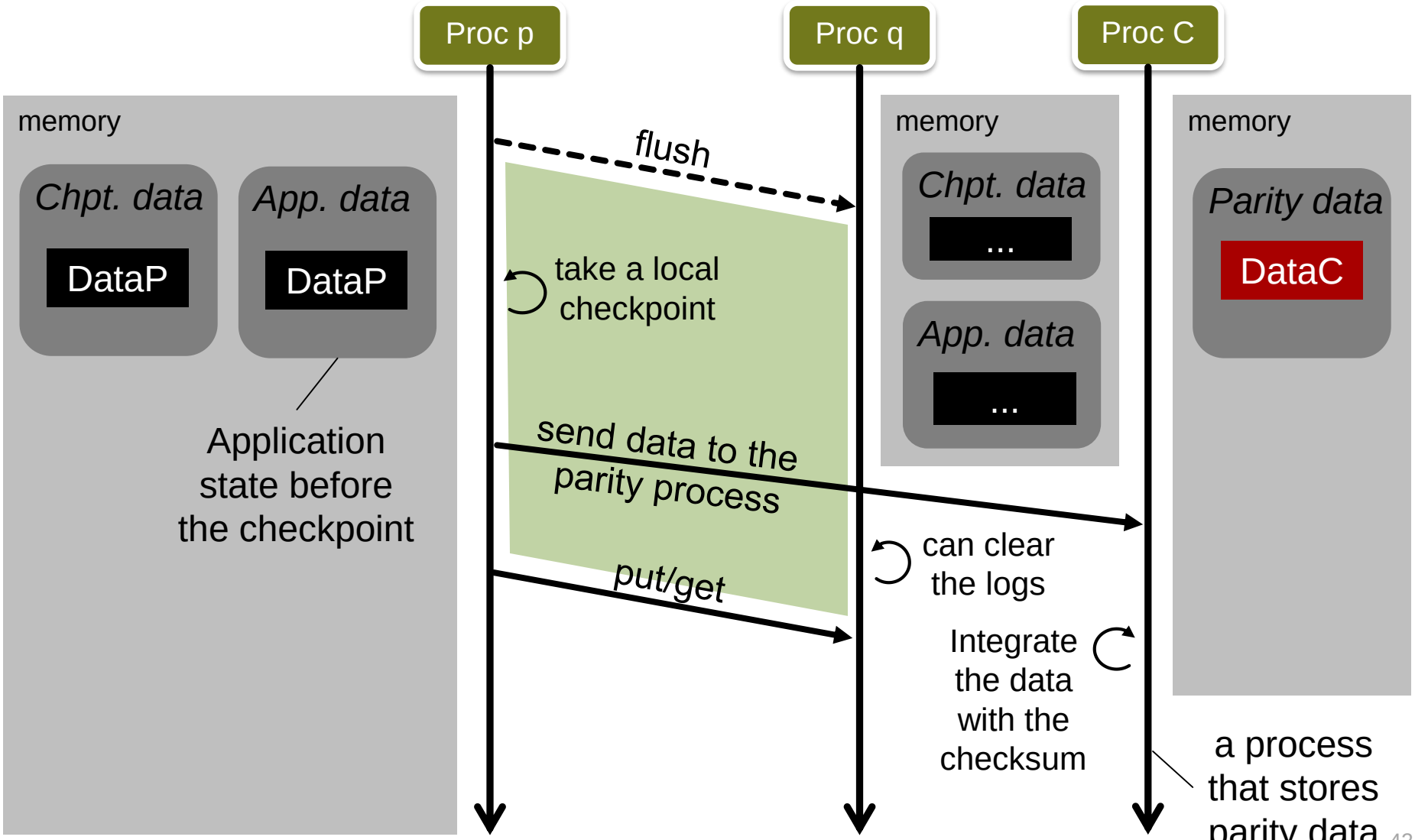
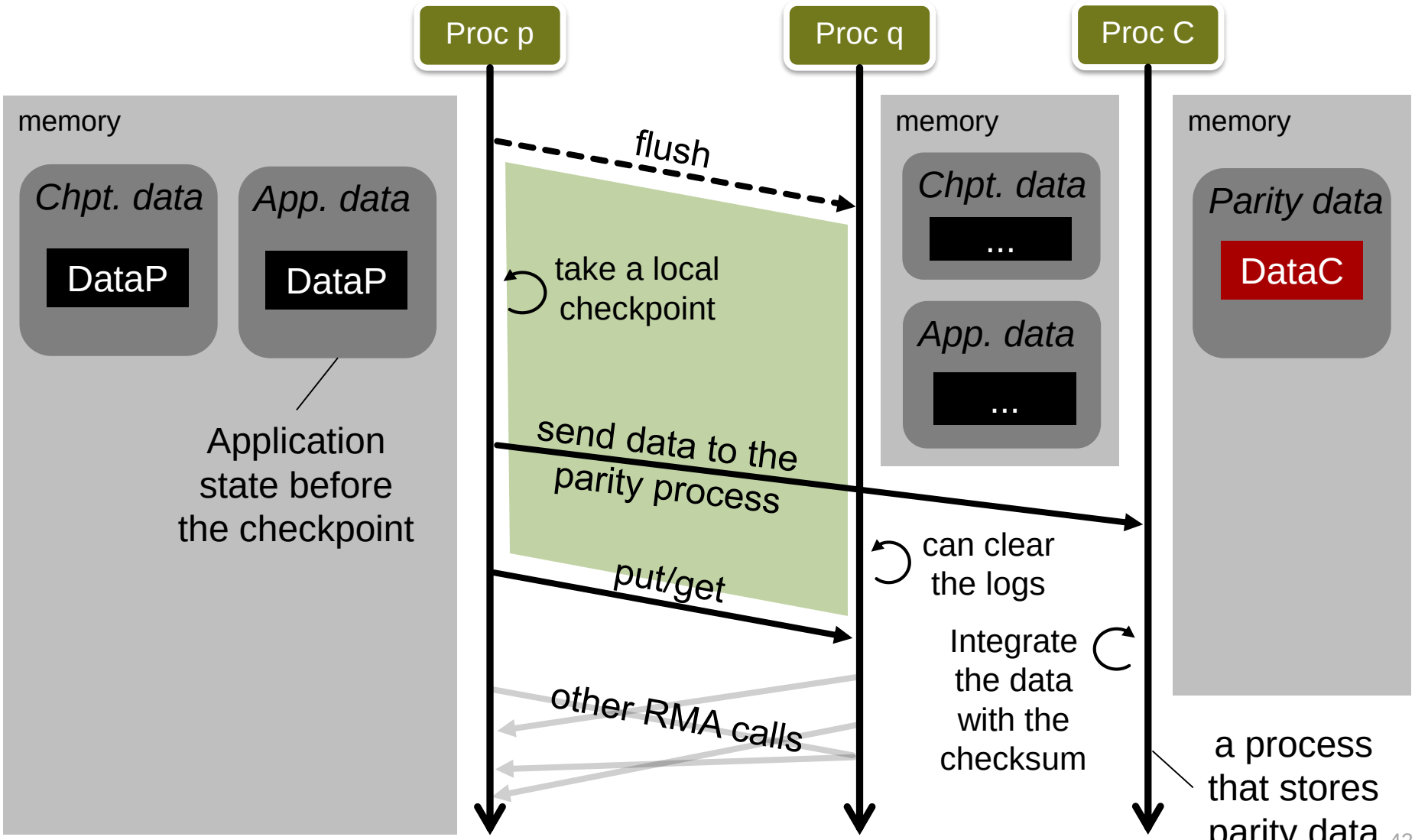


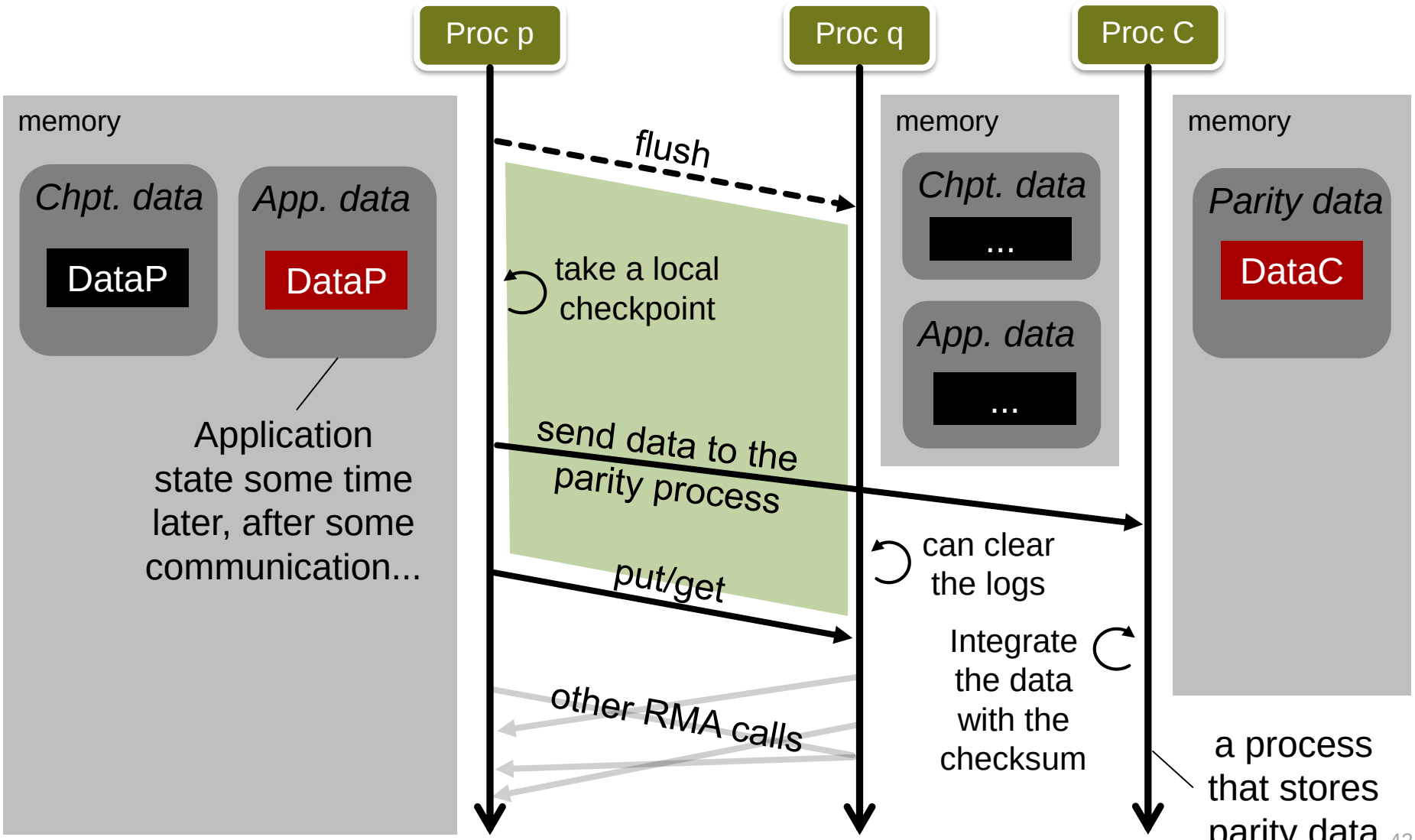
RMA: CHECKPOINTING

The Epoch Condition



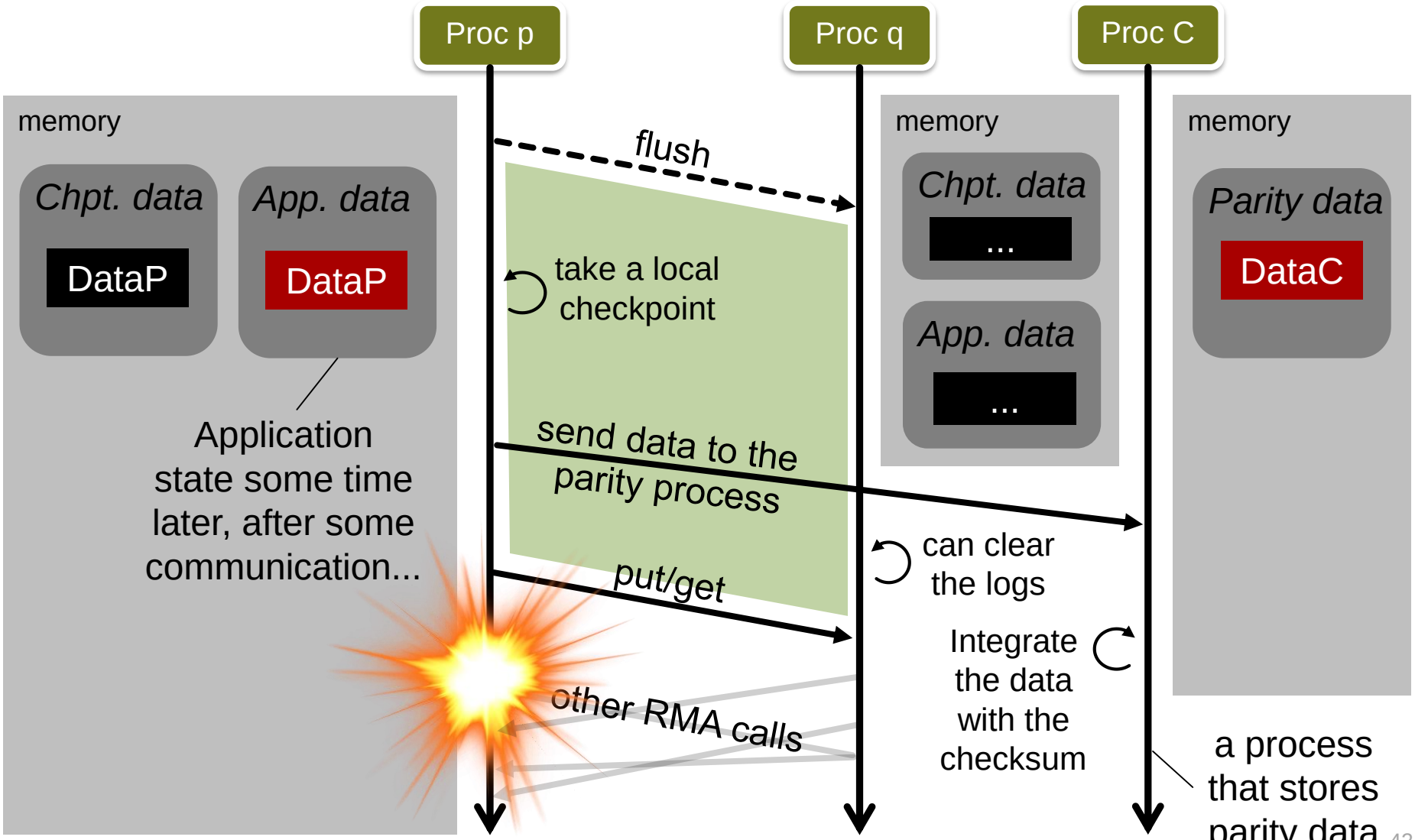
RMA: CHECKPOINTING

The Epoch Condition



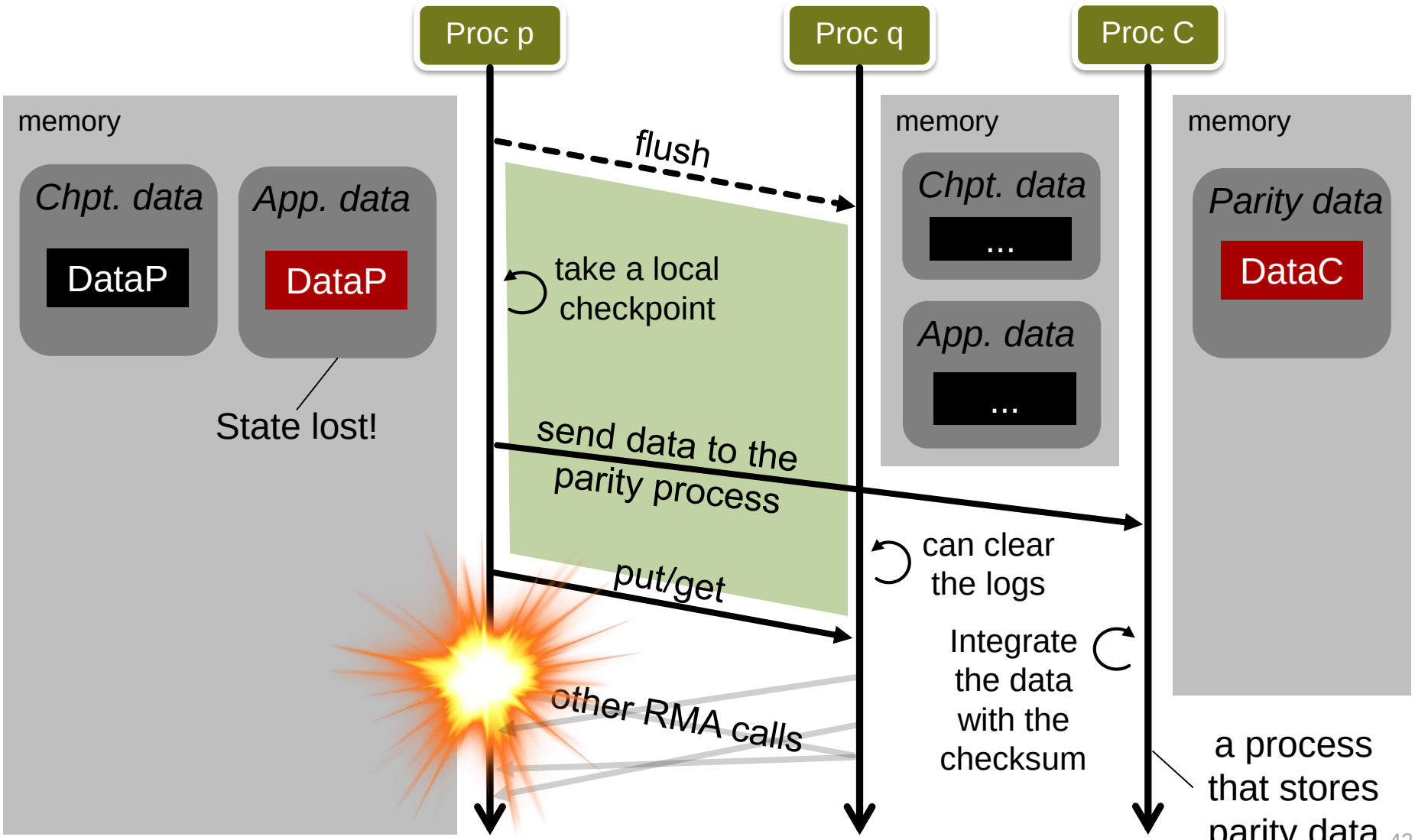
RMA: CHECKPOINTING

The Epoch Condition



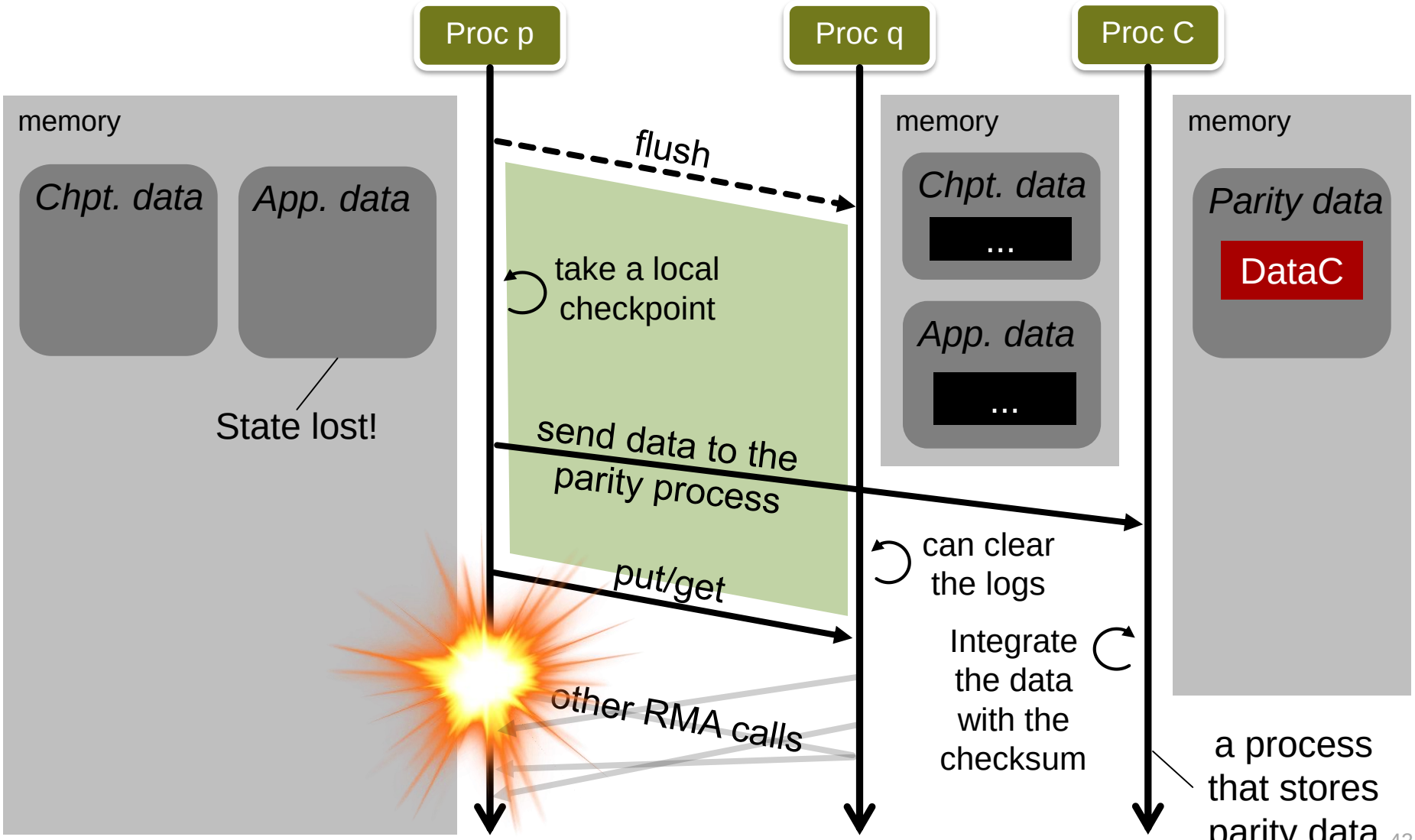
RMA: CHECKPOINTING

The Epoch Condition



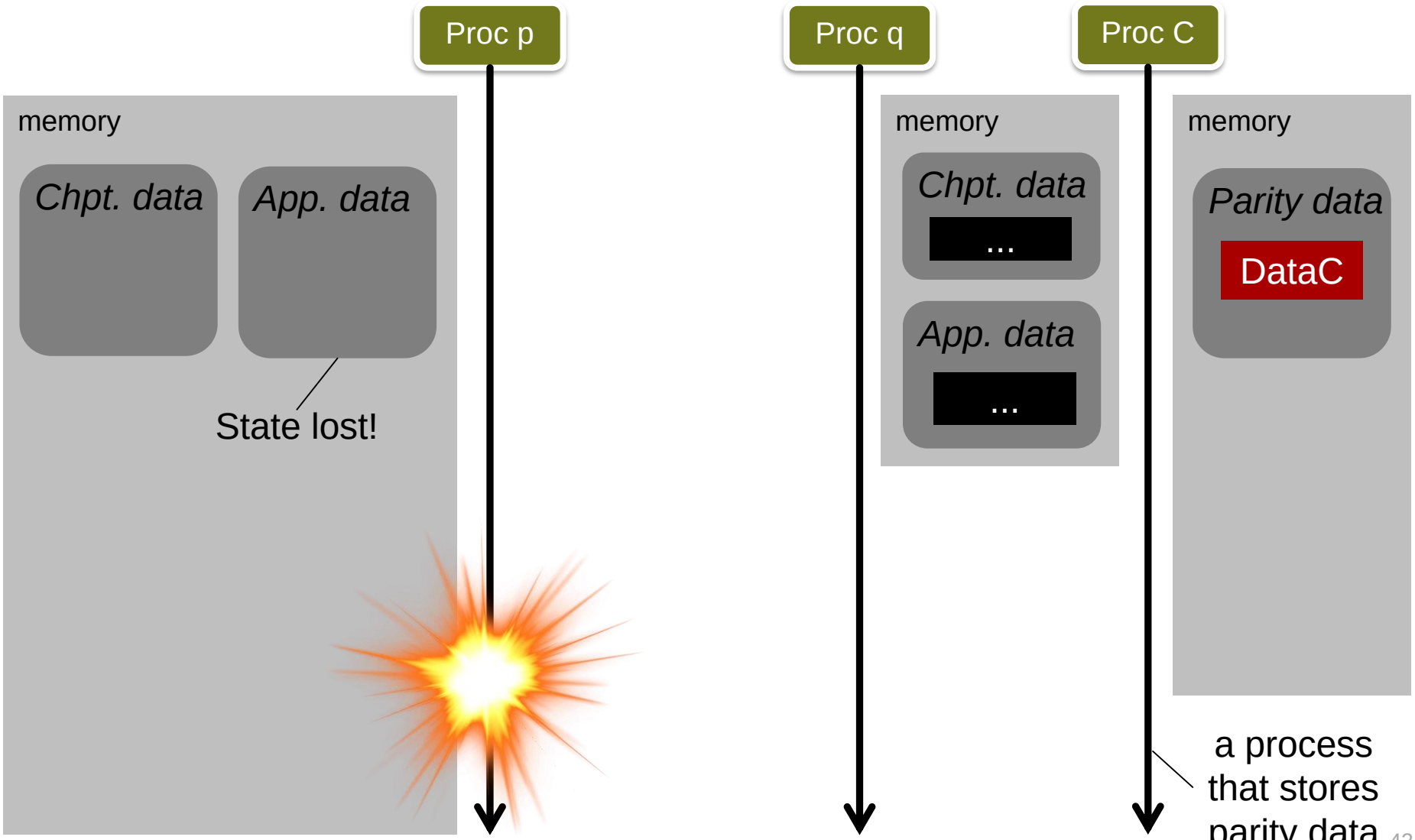
RMA: CHECKPOINTING

The Epoch Condition

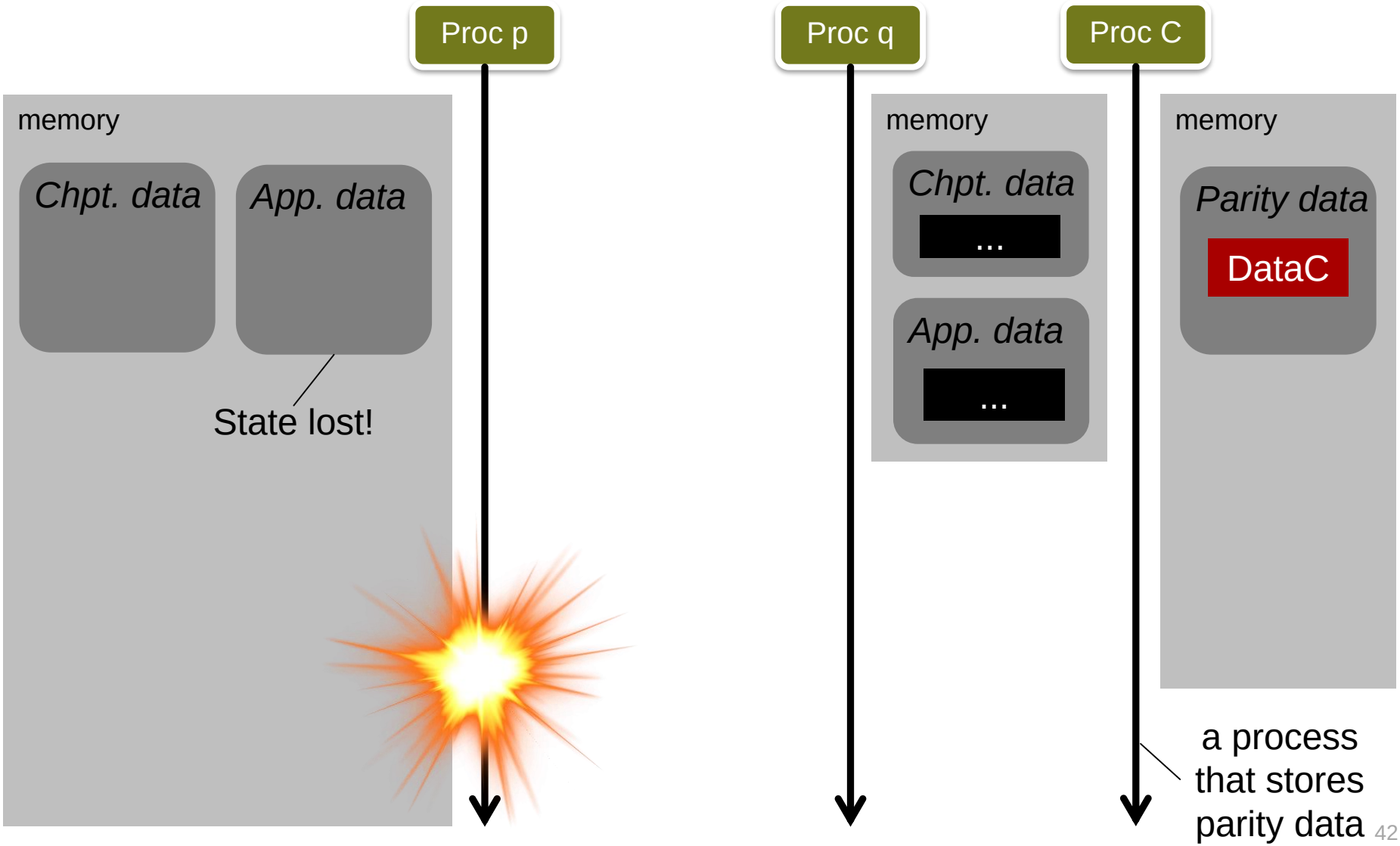


RMA: CHECKPOINTING

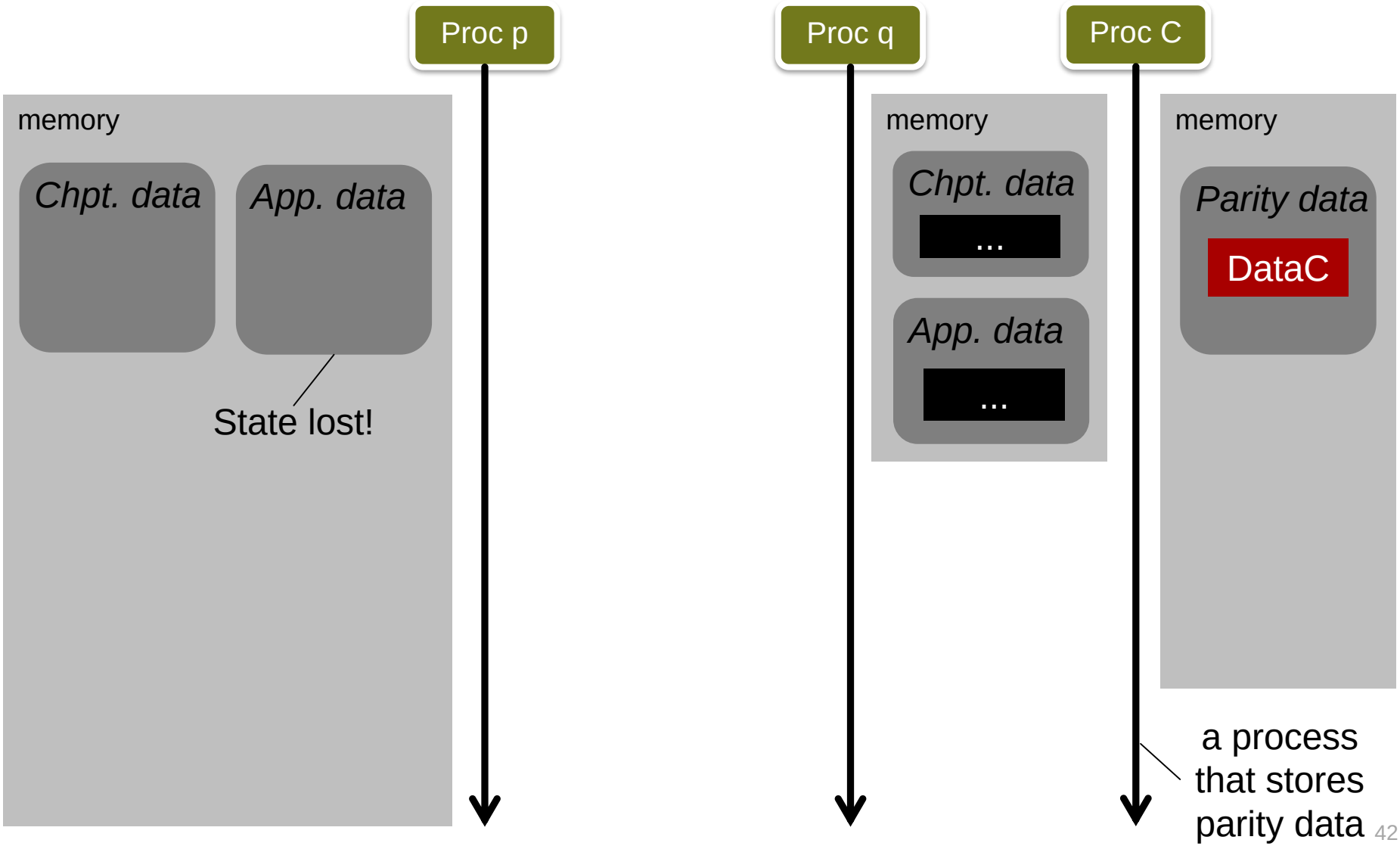
The Epoch Condition



RMA: RECOVERY

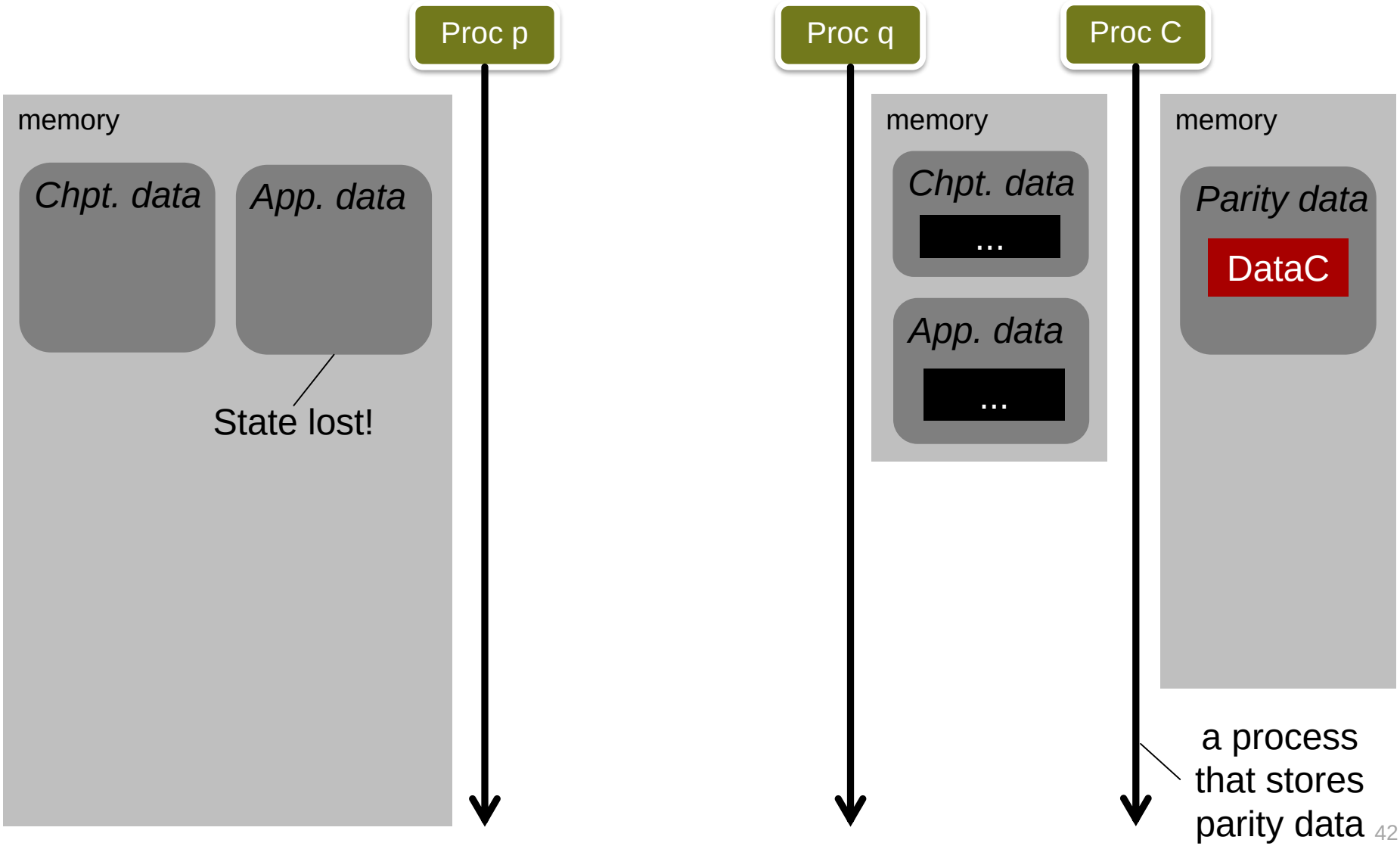


RMA: RECOVERY



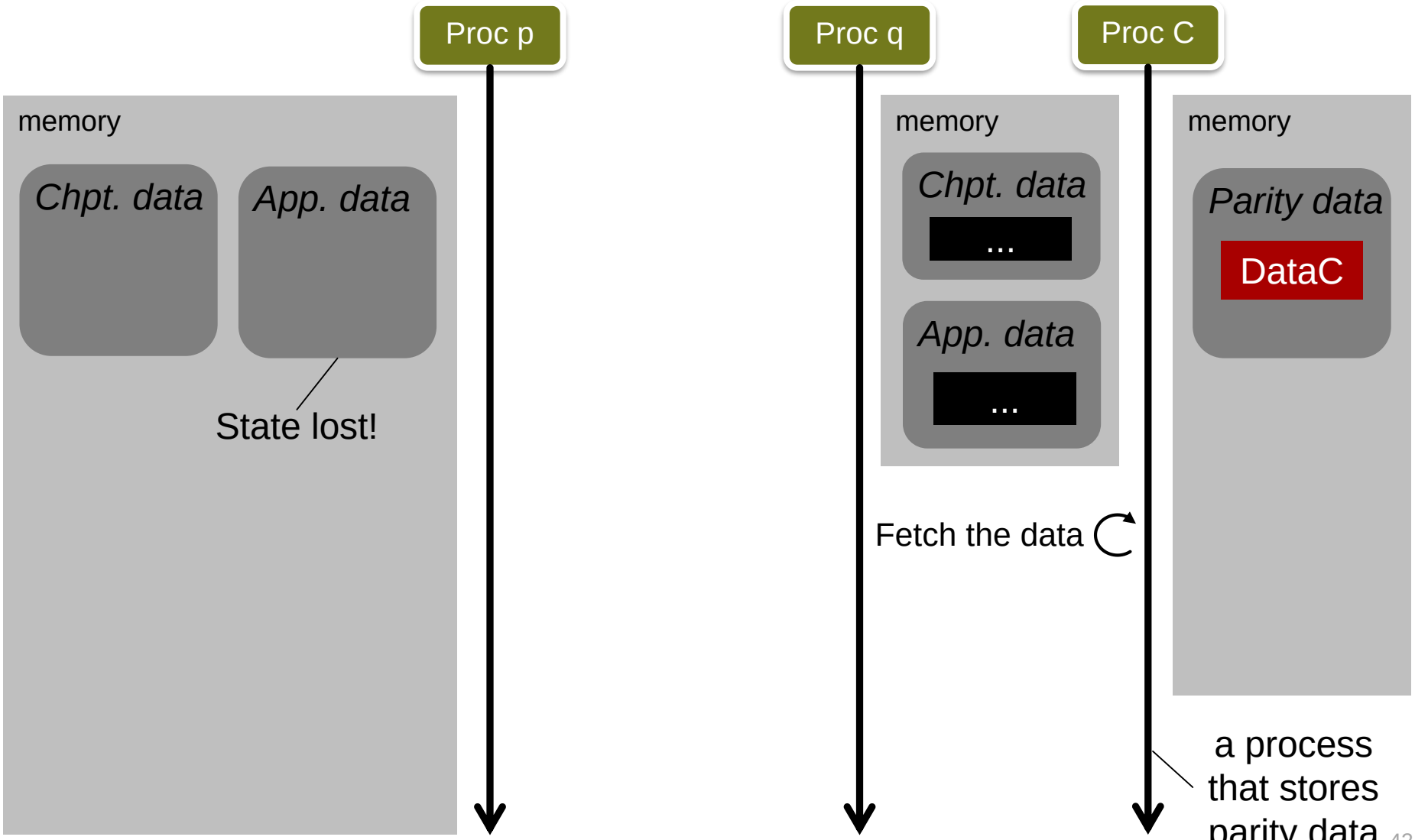
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



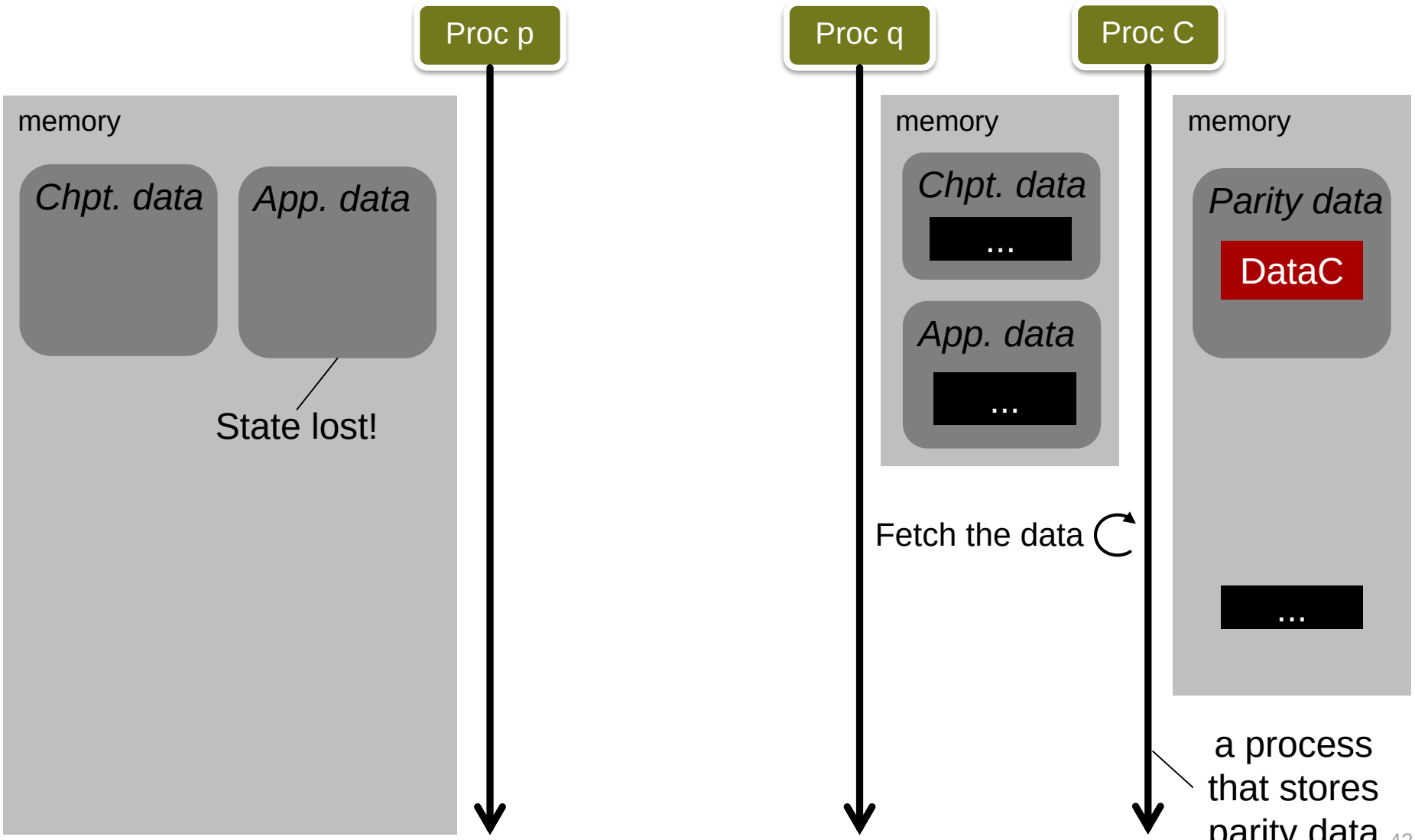
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



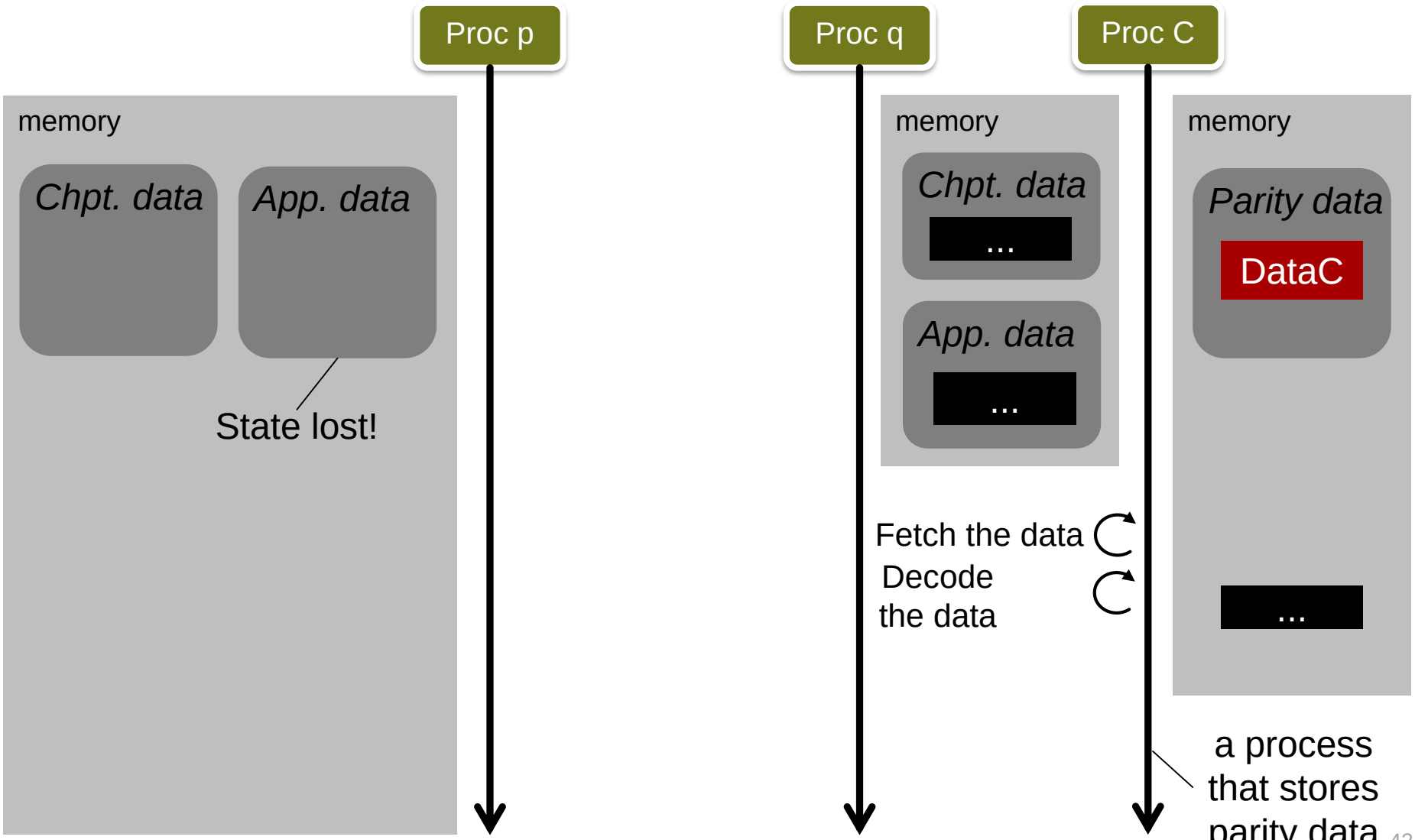
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



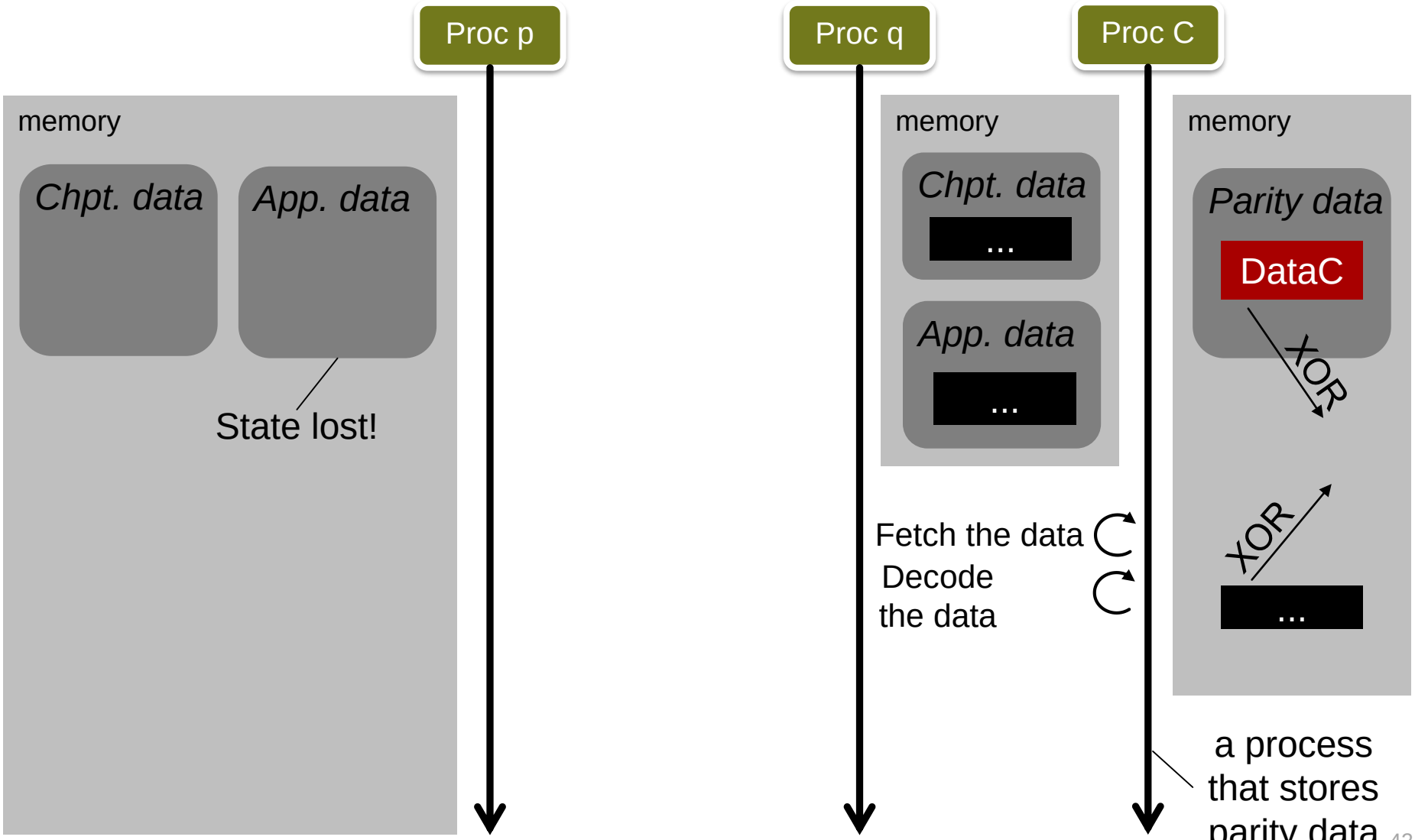
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



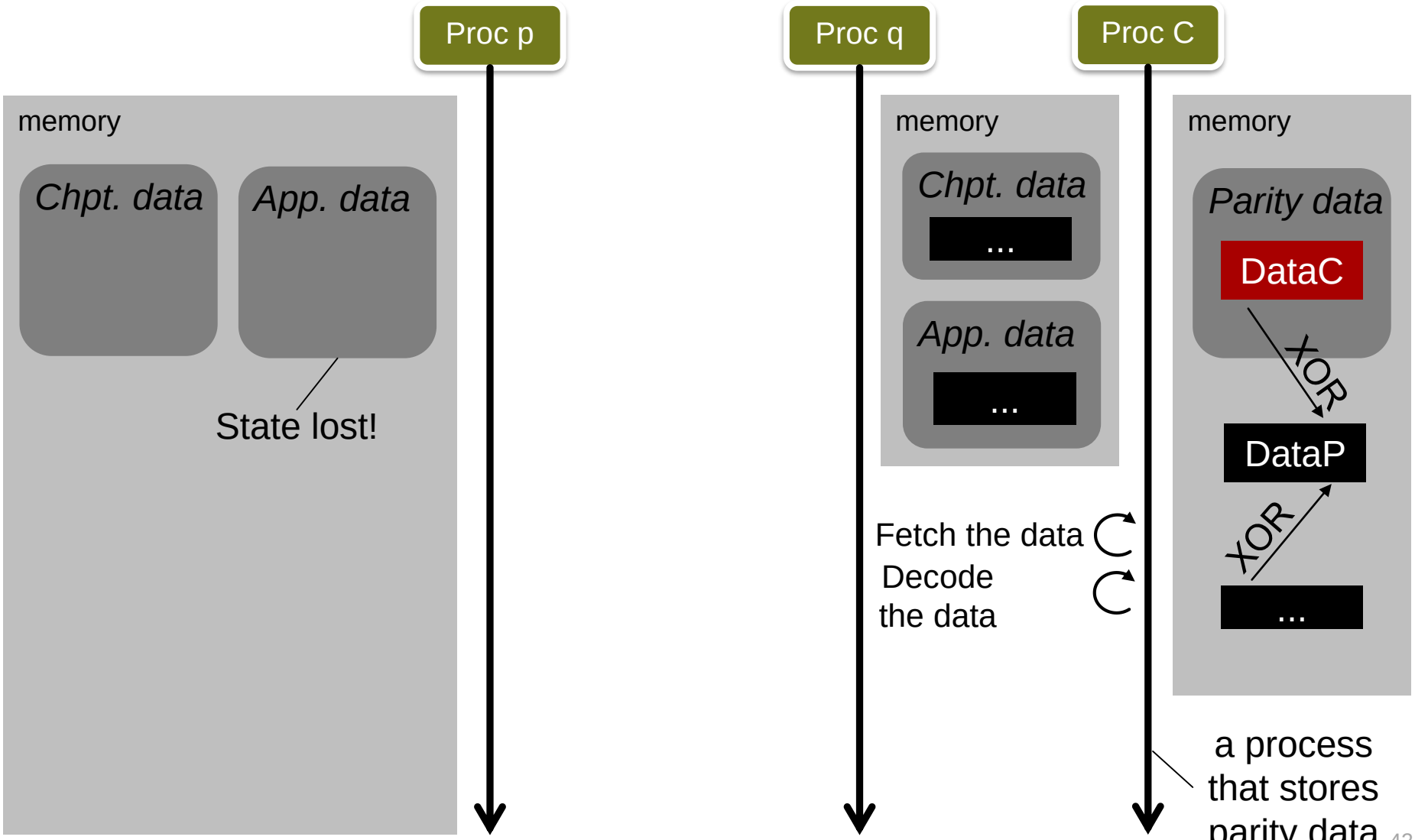
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



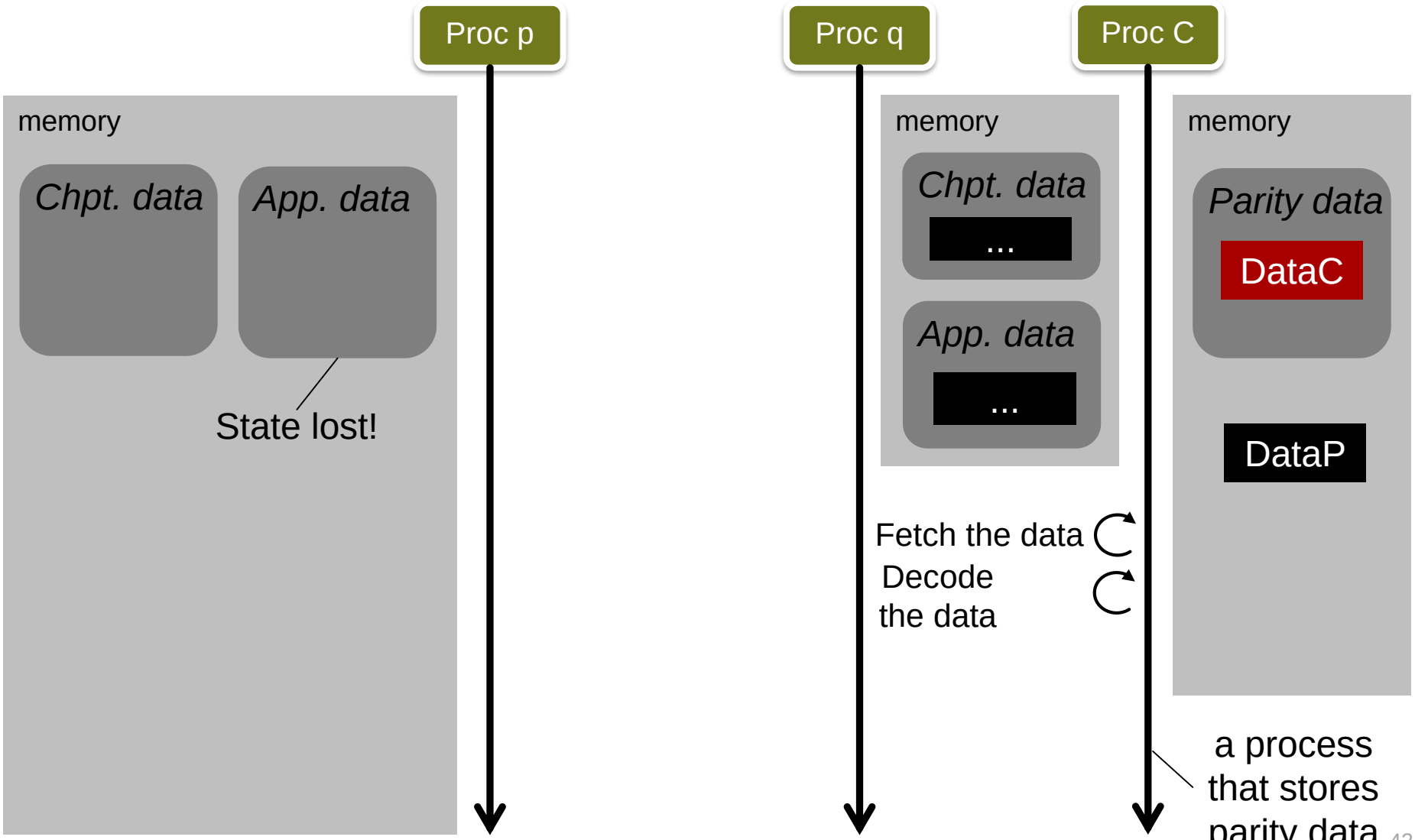
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



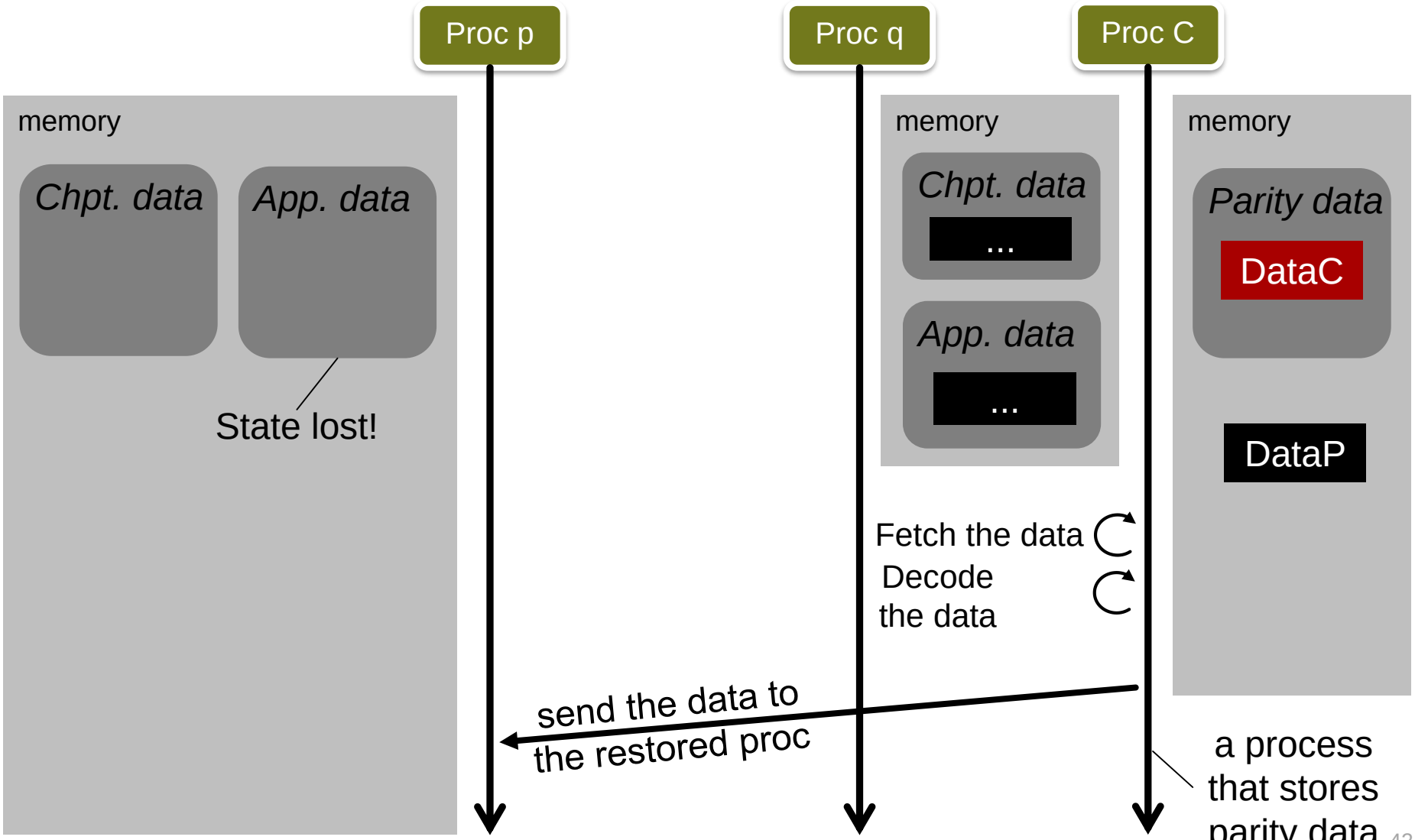
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



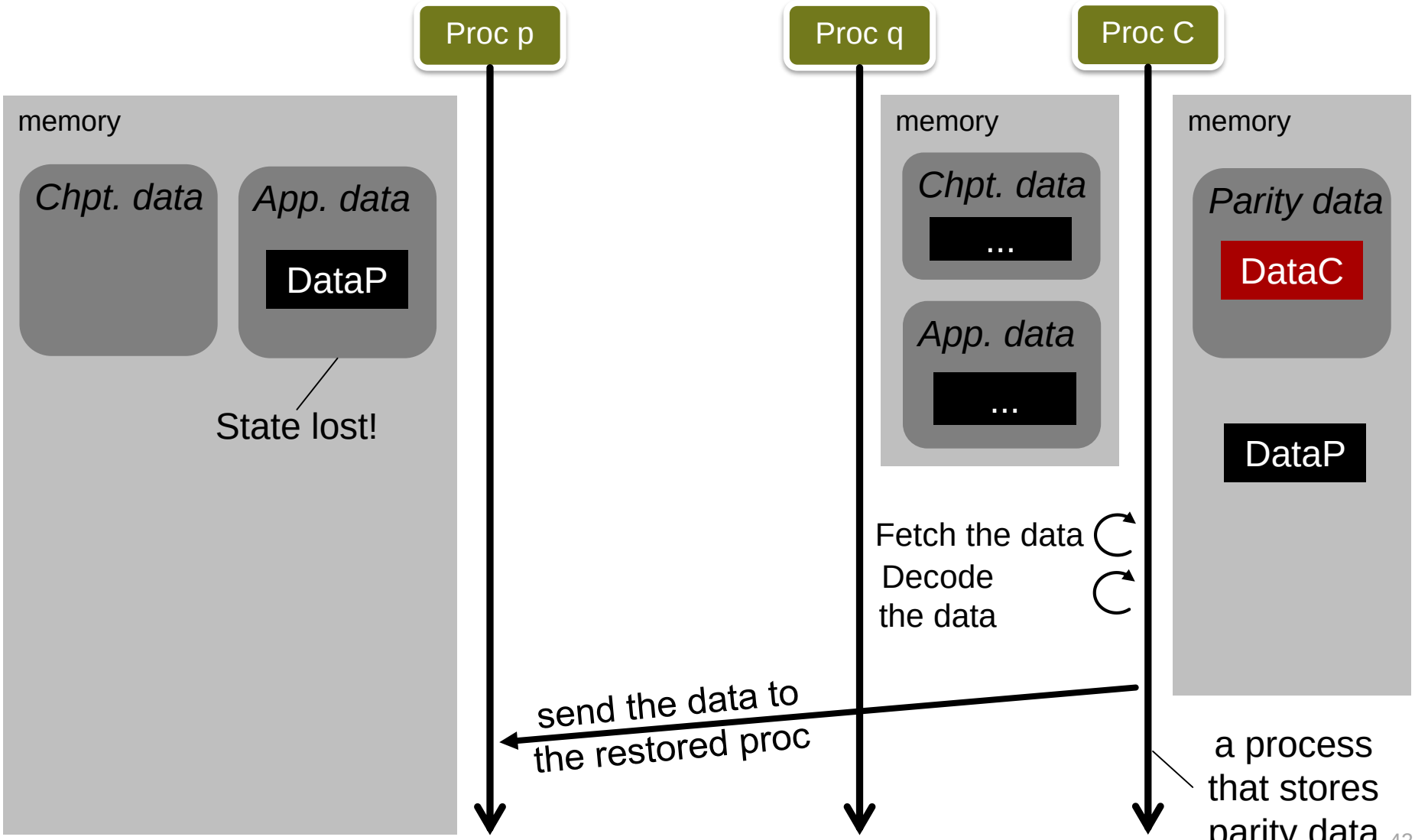
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



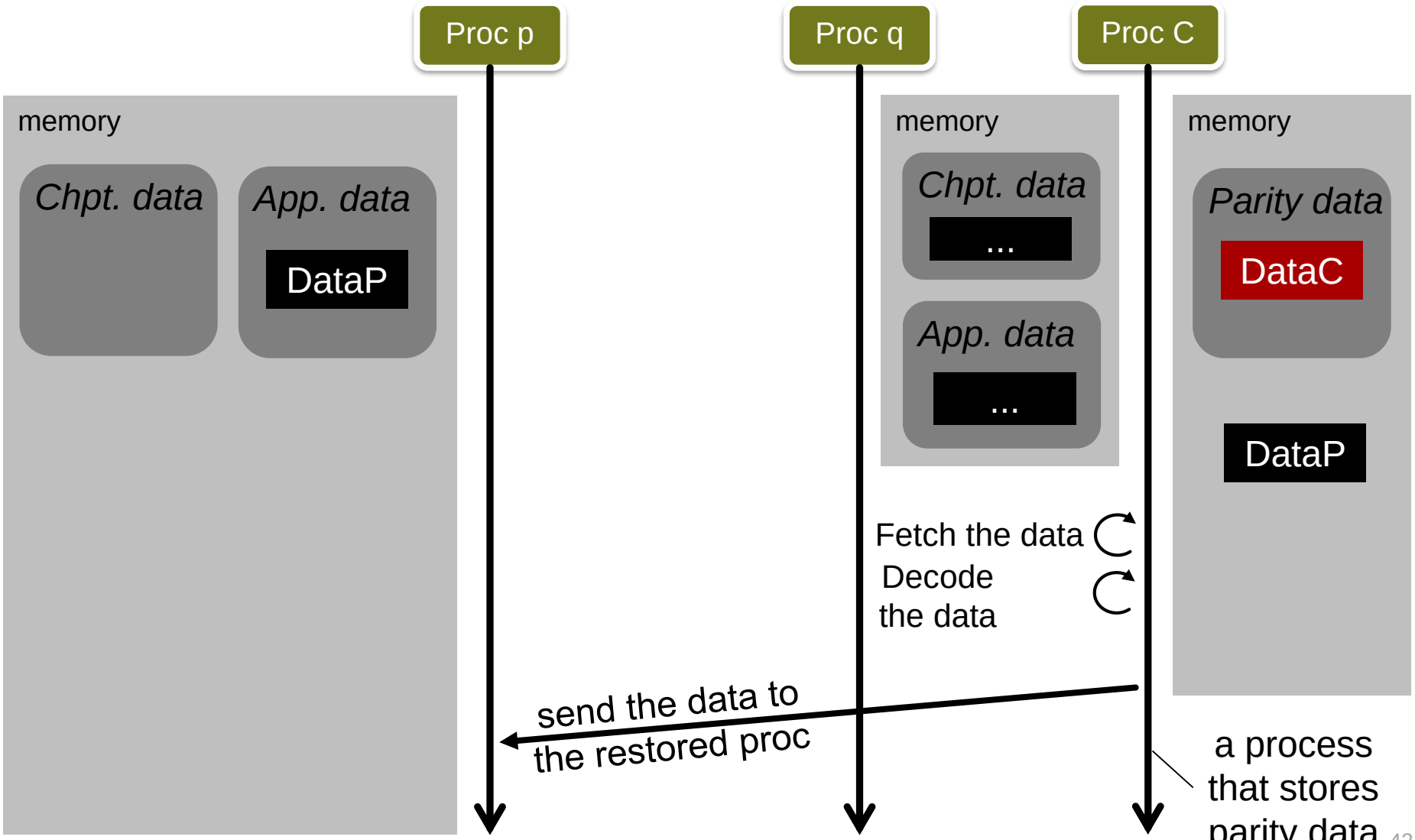
RMA: RECOVERY

Stage 1: restore the state upon checkpointing



RMA: RECOVERY

Stage 1: restore the state upon checkpointing



RMA: RECOVERY